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In this paper, we have highlighted that an on-state stress can induce a parasitic channel in AlInN/GaN HEMTs. The devices have been stressed during 216 h with a drain-to-source voltage (V_{DS}) of 20 V and a gate-to-source voltage (V_{GS}) of 0 V. A decrease in the drain current ($I_{DS\ max}$) of 43%, an increase in the access resistance (R_{ON}) of 100%, and a drop in the maximum extrinsic transconductance ($g_{m\ max}$) from 234 mS/mm down to 144 mS/mm have been observed after the ageing test. Moreover, a double peak feature is shown in the g_m (V_{GS}) characteristic 4 months after the end of the on-state stress. Consequently, we can conclude that a parasitic channel has been created by the on-state stress in the AlInN/GaN transistors. At the same time, no degradation of the Schottky contact has been highlighted after the ageing test. *Published by AIP Publishing.*
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AlGaN/GaN HEMTs (High Electron Mobility Transistors) are excellent candidates due to their potential performances in high power and high frequency for commercial and military applications.[1,2] However, few papers report that AlInN/GaN structures can have higher performances in agreement with the theoretical calculations.[3] Besides, these results were experimentally confirmed and an output current density superior to 2 A/mm has been measured for an AlInN/GaN HEMT at room temperature.[4] It is also important to note that an output power density of 10.3 W/mm at 10 GHz has been obtained with an AlInN/GaN HEMT.[5] However, the concept of AlInN/GaN HEMTs is different from that of the conventional AlGaN/GaN HEMTs. In fact, the spontaneous polarization constants of AlInN barriers are higher than those of AlGaN barriers and therefore the AlInN/GaN heterojunction is characterized by a higher two-dimensional electron gas (2DEG) compared to AlGaN/GaN devices.[3] Besides, AlInN barriers can be lattice-matched to the GaN buffer in AlInN/GaN heterojunctions, which causes no mechanical strain in the epitaxial structures. No piezoelectric polarization component exists in AlInN/GaN transistors in contrast to the piezoelectric polarization that is inherently found in the AlGaN/GaN interface as a result of tensile strain in the AlGaN barrier layer.[6] For these reasons, very little electric field driven relaxation of the material lattice (inverse piezoelectric effect) may have place in lattice matched AlInN/GaN HEMTs.[7] Moreover, the AlInN/GaN HEMTs are very interesting for the high temperature applications because of high thermal and chemical stabilities of the $In_xAl_{1-x}N$ layers which allow the device operation at 1000 °C.[7]

As these devices are intended to operate at high drain bias to deliver high output power density, it is imperative to study their reliability and to understand the physical mechanisms of their electrical performance degradation. For these reasons, we have studied the influence of the on-state stress on the electrical characteristics of AlInN/GaN HEMTs.

In this paper, the AlInN/GaN layers of the devices were obtained by Metal Organic Chemical Vapor Deposition on a sapphire substrate. It consists of a 3 μm insulating GaN, which behaves like the buffer layer, 1 nm AlN layer spacer, and 11 nm $Al_{0.82}In_{0.18}N$ non-intentionally doped layer. The room temperature channel carrier concentration, mobility, and sheet resistance are equal to $1.9 \times 10^{13}\,cm^{-2}$, $1230\,cm^2\,V^{-1}\,s^{-1}$, and 330 Ω/□, respectively. Source and drain ohmic contacts were obtained by evaporating Ti/Al/Ni/Au with annealing at 900 °C in a nitrogen atmosphere for 30 s. Ni/Au metals were used to form a Schottky contact. The gate length was defined by electron beam lithography and is 0.35 μm. The gate width is 50 μm. The studied components have a 1 μm gate-source spacing and the gate-drain distance is 3.5 μm. The isolation was made by plasma etching. The devices were passivated with an optimized SiN_X layer deposited by plasma-enhanced chemical vapor deposition. The ageing on-state stress was made with AlInN/GaN transistors biased at a drain-to-source voltage of 20 V and a gate-to-source voltage of 0 V. These electrical stresses were made with 6 AlInN/GaN devices at 30 °C in darkness in an enclosure during 216 h of accumulated stress. Then, in these bias conditions the devices were submitted to both an electrical effect and a thermal effect induced by the current. In this study, we have shown that a parasitic channel can be induced in AlInN/GaN HEMTs by an on-state stress by highlighting the presence of two humps in the g_m (V_{GS}) curves of the stressed devices.

Fig. 1 shows the electrical characteristics of AlInN/GaN HEMTs before and after 216 h of on-state stress. In order to quantify the electrical characteristics degradations induced by the ageing test, we have compared the maximum drain current ($I_{DS\ max}$) and the access resistance (R_{ON}) before and after 216 h of accumulated electrical stress. We define $I_{DS\,max}$ as the value of the drain current for a V_{DS} of 20 V and a V_{GS} of 1 V. R_{ON} is calculated from the slopes in the solid line and in the dashed line presented in Fig. 1. A decrease in $I_{DS\ max}$ from 0.75 A/mm down to 0.43 A/mm and an increase in R_{ON} from 95 Ω up to 190 Ω are highlighted after the stress. As reported in our previous study,[8] the on-state stress involves acceptor-like traps in the AlInN/GaN

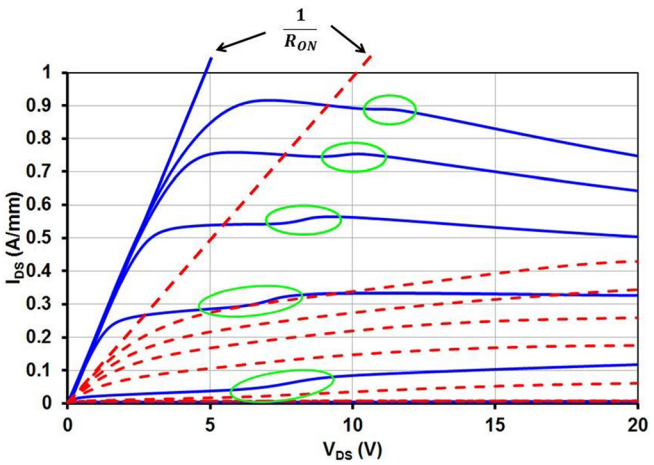

FIG. 1. I_{DS} (V_{DS}, V_{GS}) characteristics of AlInN/GaN HEMTs before (solid line) and after an on-state stress (dashed line). The drain-source voltage varies from 0 V up to 20 V and gate-source voltage increases from −6 V up to 1 V by steps of 1 V. All measurements were carried out in darkness in an enclosure. The ageing test has been done at $V_{DS} = 20$ V and $V_{GS} = 0$ V during 216 h in darkness.

components, which are responsible for the drop in $I_{DS\ max}$ and the rise in R_{ON}, which are located between the gate and the drain contacts. Moreover, the drop in I_{DS} is maximum at high V_{GS} and at low V_{DS} that it is usually induced by an electron trapping in the gate-drain access region at the device surface and/or in the layers underneath the channel.[9] In order to better understand the degradation mechanisms, we have decided to study the influence of the on-state stress on the gate current of the Schottky contact (the drain contact is not connected) and on the g_m (V_{GS}) characteristics of AlInN/GaN HEMTs. Fig. 2 presents the I_{GS} (V_{GS}) characteristics (Fig. 2(a)) and the I_{DS} (V_{GS}) characteristics (Fig. 2(b)) before and after 216 h of accumulated on-state stress and 4 months and then 1 year after the end of the stress. The ideality factor (η) and the barrier height (Φ_b) of the Schottky contact have been extracted by fitting the current-voltage curves of the Schottky contact under forward bias to a thermoionic emission model to monitor the impact of the electrical stress on the stability of the gate. So, η and Φ_b remain close to 2.3 and 0.45 eV, respectively, after the stress and 4 months and 1 year after the end of the stress. The high value of the ideality factor may be explained by a generation-recombination or Poole-Frenkel or tunneling mechanisms.[10] Consequently, the Schottky contact has not been degraded by the on-state electrical stress. However, the on-state stress induces a drop in the gate current measured in the reverse regime and a slight decrease in I_{GS} in the forward regime. Nevertheless, 4 months after the end of the ageing test, an increase in the reverse gate current and a low rise in I_{GS} in the forward regime are observed, and then the gate current remains identical when the I_{GS} (V_{GS}) is measured 1 year after the end of the stress. This phenomenon is explained by the creation of slow electron traps by the ageing test. Moreover, the extrinsic transconductance has been compared before and after the electrical stress, as shown in Fig. 3. The shape of the g_m (V_{GS}) curve measured before the on-state stress is similar to that obtained with a single heterostructure quantum well InAlN/GaN HEMT which has high electrical and radiofrequency performances, as reported in Ref. 11. The maximum extrinsic transconductance drops from 234 mS/mm down to 144 mS/mm after the ageing test. This phenomenon is in agreement with the drain current degradation observed after the electrical stress in Fig. 1. Moreover, g_m decreases gradually when V_{GS} varies between −2.8 V and 3 V before the ageing test while g_m decreases when V_{GS} increases from −2.8 V up to −1.2 V and then remains nearly unchanged when V_{GS} is higher than −1.2 V after an ageing time of 216 h. Besides, Fig. 3 shows that the transconductance degradation is more pronounced after an ageing test when V_{GS} varies between −2.8 V and 1 V than for a gate-to-source voltage close to 2 V. Zhu *et al.*[12] have already observed a strong degradation of the g_m hump after on-state-high-field stress while the g_m (V_{GS}) curves are almost the same before and after the ageing test when the values of V_{GS} are close to 0 V. In this case, they say that the g_m degradation is mainly induced by a drop of the channel conductivity (i.e., a rise in the channel resistance) and to a lesser extent to an increase in access drain resistance which is ascribed to an electron trapping in the gate–drain access region.[12] In our case, Fig. 3 highlights that the decrease in g_m is also pronounced near the g_m peak than for $V_{GS} = 0$ V, and consequently, we cannot affirm that the g_m reduction is only explained by a channel degradation. Furthermore, the difference between the values of g_m measured at $V_{GS} = 0$ V before and after the on-state stress would be lower if the drop in g_m was only related to a decrease in channel conductivity, in contrast to our results. Thus, we can suppose that the electrical stress involves not only channel degradation but also an access drain resistance deterioration.

Fig. 3 also shows that the maximum transconductance peak changes from −2.5 V down to −3 V after 216 h of on-state stress. We can suppose that the g_m peak shift is related to the electrical traps induced by the ageing test.[13] However, the g_m bump increases from −3 V up to −2.6 V when the g_m (V_{GS}) curve is measured 4 months after the end of the on-state stress. We think that some of the carriers are

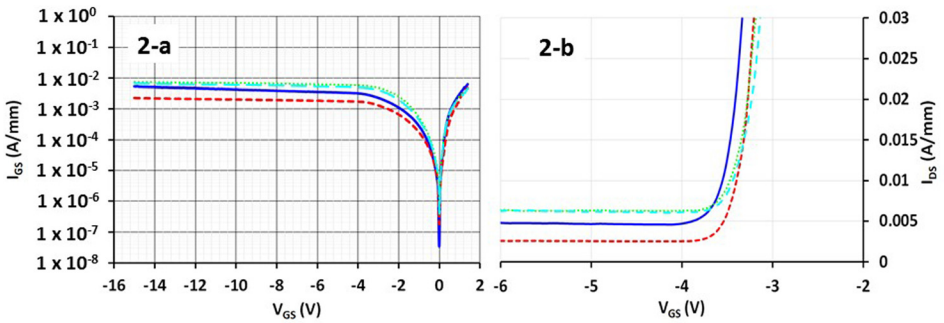

FIG. 2. I_{GS} (V_{GS}) (a) and I_{DS} (V_{GS}) (b) characteristics of AlInN/GaN HEMTs before (solid line) and after 216 h of on-state stress (small dashed line) and 4 months (dotted line) and 1 year (large dashed line) after the end of the stress. The ageing test has been done at $V_{DS} = 20$ V and $V_{GS} = 0$ V during 216 h in darkness. The I_{DS} (V_{GS}) curves (b) have been measured at $V_{DS} = 15$ V.

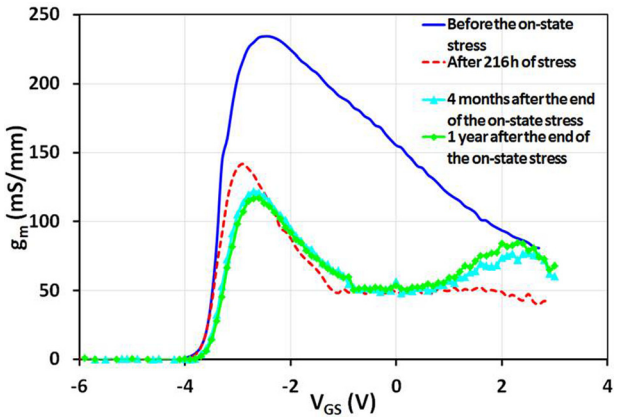

FIG. 3. g_m (V_{GS}) characteristics of AlInN/GaN HEMTs measured at $V_{DS} = 15$ V before (solid line) and after an on-state stress of 216 h (dashed line). The ageing test has been done at $V_{DS} = 20$ V and $V_{GS} = 0$ V during 216 h in darkness. The g_m (V_{GS}) characteristics of stressed AlInN/GaN HEMTs were also performed 4 months (triangle) and 1 year (diamond) after having stopped the on-state stress.

released by the slow traps induced by the ageing test and the maximum transconductance is shifted positively.

Moreover, it is also important to note that a second hump begins to appear at a V_{GS} close to 2 V when the transconductance was measured 4 months after the stress. Then, the g_m (V_{GS}) curves have been measured several times after the ageing test in order to highlight or not the irreversibility of the second g_m bump. Thus, we have shown that this second bump intensity increases slightly when the transconductance measurement has been done 1 year after the on-state stress. In these conditions, these results prove that the appearance of the second g_m hump is irreversible and we can affirm that it is induced by the on-state stress. Zhu *et al.*[12] have already reported the appearance of two humps in the g_m (V_{GS}) curves after a reverse-gate-bias stress of 25 h and they think that this phenomenon is similar to the kink effect that could be induced by hot electron trapping and field-assisted detrapping via donor-like traps in the GaN buffer layer as it has been shown for AlGaN/GaN HEMTs.[14] However, we think that the presence of two humps in the g_m (V_{GS}) curves after an ageing test is not necessarily related to the kink effect because Fig. 1 highlights the presence of kink effect on the I_{DS} (V_{DS}, V_{GS}) characteristics of unstressed AlInN/GaN HEMTs (area surrounded by a circle in Fig. 1) while a second hump is not observed in g_m (V_{GS}) measurements done before electrical stress. For these reasons, we assume that the physical mechanisms which explain the presence of two g_m humps are different from those reported by Zhu *et al.*[12] Besides, this hypothesis is consistent because they have observed two g_m humps in transconductance measurements of AlInN/AlN/GaN HEMTs after a reverse-gate-bias stress of 25 h but not after an on-state stress.[12] Moreover, this assumption is reinforced by the absence of the kink effect on the I_{DS} (V_{DS}, V_{GS}) curves measured after an ageing test of 216 h (as seen in Fig. 1).

In order to better understand the degradation mechanisms induced by the on-state stress, we analyzed carefully the g_m (V_{GS}) characterized for an AlInN/GaN HEMTs ageing during 216 h, which is presented in Fig. 3. It is important to note that the second hump clearly appears at a V_{GS} close to 2 V when the stressed AlInN/GaN HEMTs were characterized 4 months and then 1 year later and not immediately after the ageing. Moreover, no difference between the g_m values measured at gate-to-source voltages close to 2.5 V was observed with those monitored before the electrical stress. Thus, we can conclude that the g_m deterioration is mostly explained by an increase in channel resistance in place of an increase in drain access resistance induced by an electron trapping effect in the gate-drain access region. The presence of these two g_m humps in Fig. 3 can be reminiscent of the typical g_m (V_{GS}) characteristics measured for AlInN/GaN based double channel high electron mobility transistors.[15,16] However, we think that the first g_m peak is ascribed to a GaN channel of AlInN/GaN HEMTs and the second g_m peak clearly pronounced, which appears 4 months and 1 year after the end of the on-state stress, corresponds to the creation of a parasitic channel induced by the ageing test. As the drain-to-source voltage is high and that the AlInN/GaN HEMT channel is fully open during the on-state stress, a high density of hot electrons is generated in the region between the drain and the source contacts and these hot carriers can cause severe degradation in the GaN channel. It is well known that the hot electrons generated by the off-state stress ($V_{GS} = -6$ V and $V_{DS} > 32$ V) involve a creation of electron traps in GaN buffer[7] because the vertical component of the electrical field pointing to the GaN buffer promotes the injection of hot electrons in the GaN buffer, i.e., the creation of trap states in the GaN buffer. Nevertheless, no vertical electrical field exists when the component is submitted to an on-state stress and we think that the density of the defects induced by the hot electrons in the GaN buffer is lower than for an off-state stress. Nevertheless, we assume that the hot electrons can reach high energy levels during the on-state stress to be injected and generate more defects and electron traps in the AlInN/GaN interface and/or in the AlInN layer and/or in the passivation layer/AlInN interface. So, hot electrons remain trapped in the gate-drain access region. This assertion allows explaining the reduction in $I_{DS\ max}$, the increase in R_{ON} observed after 216 h of on-state stress (see Fig. 1), and the drop of $g_{m\ max}$ observed after 216 h of the ageing test, which are highlighted in Fig. 3. However, the appearance of a second hump in the g_m (V_{GS}) curves after the ageing is clearly observed 4 months and 1 year after the end of the stress but not immediately after the ageing test. Thus, we can conclude that the on-state stress allows hot electrons to have sufficient energy to pull some electrons to the semiconductor layer atoms and/or from the GaN channel and these carriers are confined and trapped in the AlInN/passivation layer interface and/or in the passivation layer. We can also claim that these electrical traps induced by the ageing test are very slow because the parasitic channel is only observed 4 months after having stopped the on-state stress. Moreover, Fig. 3 shows that the second g_m peak is higher after a rest time of 1 year than after 4 months. This means that the second g_m hump is only observed when the slow electron traps induced by the on-state stress release their carriers in the AlInN/passivation layer interface and/or in the passivation layer. We have already shown that trapped carriers can be released from electron traps after several days.[17] In fact, this phenomenon has been observed for AlGaN/GaN HEMTs after a neutron

irradiation with a fluence of 6×10^{11} neutrons/cm^2. This hypothesis is consistent with the positive g_m peak shift, which has been observed 4 months after the end of the stress and is shown in Fig. 3. Moreover, the appearance of the second g_m bump at V_{GS} value close to 2 V confirms that the parasitic channel is created in the top of the AlInN/GaN HEMTs. Besides, this parasitic channel can be correlated with the increase in the gate current measured 4 months and 1 year after the end of the stress. First, I_{GS} (V_{GS}) characteristics have been measured when the drain contact is not connected. Thus, the parasitic channel is located between the gate and the source contacts. Second, Fig. 2(a) shows a decrease in I_{GS} after 216 h of stress and no second g_m hump is observed in Fig. 3. Third, an increase in I_{GS} is highlighted (Fig. 2(a)) and a second hump is observed when the g_m (V_{GS}) curves (Fig. 3) are measured 4 months after the end of the ageing test. Besides, I_{DS} (V_{GS}) curves (Fig. 2(b)) show that it is more difficult to pinch-off the channel 4 months after the end of the stress because I_{DS} measured for V_{GS} varying between −6 and −4 V is clearly higher. Therefore, we assume that a parasitic channel between the source and gate contacts, but not under the gate, initiates this second g_m hump (Fig. 3) and this increase in gate current (Fig. 2(a)). So, these results prove that the on-state stress induces a trapping of hot electrons in GaN buffer and/or an injection of hot carriers which are expelled from the channel in the AlInN/passivation layer interface and/or in the passivation layer. Besides, the presence of this parasitic channel can explain that there is no difference between the values of g_m measured at a V_{GS} close to 2 V before the on-state stress and those obtained 1 year after the on-state stress despite the degradation of drain access resistance induced by the ageing test. Thus, the drop in access resistance is obscured by the presence of the parasitic channel in the passivation layer. We think that the mobility of the carriers which are at the origin of the parasitic channel is lower than that of the 2DEG because of the defects induced by the on-state stress. Moreover, the parasitic channel has an impact on the total drain current because an increase in the drain current is observed 4 months after the end of stress in comparison with that obtained immediately after the end of the stress. This phenomenon is amplified for higher rest time equal to 1 year (not shown here). This rise in I_{DS} is explained by the formation of the parasitic channel.

In summary, we have highlighted that an on-state stress induces a decrease in I_{DS}, a drop in g_m, and an increase in R_{ON}. Besides, we have shown that this ageing test induces the creation of a permanent parasitic channel in the top of the device structure. These degradations have been explained by the trapping of hot electrons in the gate-source access region and by a confinement of electrons extracted from the channel and/or an injection of hot electrons in the passivation layer. We think that it would be interesting to study the existence of this parasitic channel by capacitance-voltage measurements.

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