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Thermal penetration depth analysis and impact of the BEOL metals on the thermal impedance of SiGe HBTs

Rosario D'Esposito, Suresh Balanethiram, Jean-Luc Battaglia, Sébastien Frégonèse and Thomas Zimmer

Abstract—In this letter we present a detailed investigation on how dynamic thermal phenomena take place in state-of-the-art SiGe HBTs when excited by a sinusoidal power dissipation. To give a better insight into the mechanisms leading to the thermal impedance (Z_{th}) decay, we introduce the concept of thermal penetration depth; then, with the help of 3D thermal simulations, we illustrate its effect on the spatial distribution of the temperature variations within the transistor structure, according to the frequency of operation. In order to experimentally analyze the impact on a real device, dedicated HBT structures are designed; they consist of multi-finger SiGe HBTs realized in B55 technology from STMicroelectronics, for which modifications are made in the Back-End-Of-Line (BEOL) metallization or in the transistor layout, increasing its Deep Trench Isolation (DTI) enclosed area. For these transistors, Z_{th} measurements are carried out in the frequency range 10kHz–1GHz; the results show that the metal connections configuration in the BEOL or layout modifications can considerably impact the Z_{th} decay at low frequencies. An identical Z_{th} trend is instead measured above 1-2 MHz, demonstrating that at higher frequencies just the region close to the heat source is concerned by dynamic thermal phenomena.

Index Terms—SiGe HBT, thermal penetration depth, thermal impedance, BEOL metals thermal impact, thermal capacitance

I. INTRODUCTION

Thermal effects are one of the key factors limiting the performance and reliability of devices and integrated circuits realized using SiGe HBT technologies, in which the continuous trend to shrink the device dimensions leads to critically high power densities [1], [2]; in addition, the adoption of shallow and deep trench isolations, filled with low thermal conductivity materials, limits the lateral heat diffusion, and thus contributes to increase the devices R_{th} . Due to the strong relationship between electrical and temperature effects in these components [3], which is worsened by their positive feedback [4], a realistic and physics-based thermal compact modeling is mandatory; a reliable compact model must ensure accurate circuit simulations during the design phase [5], [6], which take into account the operating temperatures of the HBTs. In state-of-the-art SiGe HBTs thermal phenomena arise when a static power dissipation (P_{diss}) is applied, but also when the devices

are operated in dynamic conditions, since their thermal bandwidth is within few hundreds of MHz [7], [8]. Many works can be found in literature about DC self-heating effects [4], [9]–[11], but less attention is given to dynamic thermal modeling. It must be considered, though, that when the HBTs are driven by a signal having a bandwidth within their thermal constant, due to the intrinsic transistor nonlinearities, third-order intermodulation products (IMD3) arise and can trigger low frequency (LF) variations of the junction temperature, which can significantly affect the electrical behavior of the component [12], [13]. A deep understanding of the thermal mechanisms taking place in sinusoidal operation and a precise characterization of the Z_{th} are therefore necessary to obtain a realistic thermal model, which can result very helpful in certain applications, like the design of pre-distortion linearizers for power amplifiers [14]–[16].

In this letter we present a detailed investigation on how dynamic thermal phenomena take place in state-of-the-art SiGe HBTs, by introducing the concept of thermal penetration depth. 3D thermal simulations are reported in section II, which gives an alternative insight into these physical mechanisms; in section III different sets of dedicated transistor structures are presented and their $Z_{th}(f)$ are compared; to our knowledge no previous study on the BEOL has been supported by Z_{th} measurements.

II. THERMAL PENETRATION DEPTH SIMULATIONS IN 3D TCAD

To have an alternative insight into the dynamic spreading of the heat within the transistor structure, we can consider a very simplified case of study: let us assume a semi-infinite silicon block having an initial uniform temperature T_0 . When a uniformly distributed P_{diss} is applied at one side, eventually the whole block of material will tend to reach a higher temperature T_1 . But before this happens, a thermal gradient can be observed within a certain distance from the heat source, while beyond this boundary the temperature of the block is still T_0 . The thermal penetration depth (δ) is defined as the distance that the heat diffuses through the material (under a sinusoidal stimulus) during a time $1/f$ and is approximated with the expression [17]:

$$\delta = \sqrt{\frac{k}{c \rho \pi f}} \quad (1)$$

where f is the P_{diss} frequency, whereas k , c and ρ are, respectively, the thermal conductivity, specific heat and density of the material. Note that (1) is only valid in 1D heat transfer by conduction; moreover it must be considered that a state-of-the-art SiGe HBT has a complex structure, made of multiple material layers, having very different thermal properties.

Nevertheless, (1) indicates the general trend that should be

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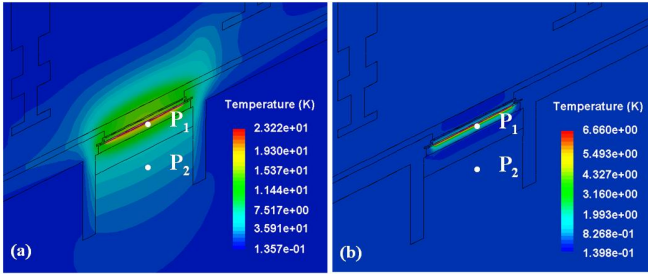


Fig. 1. Simulated 3D structure of the B11HFC HBT (zoom on the transistor), showing the thermal penetration depth (δ) profile. A sinusoidal power having a frequency of 50kHz (a) and 100MHz (b) are applied at the BC junction.

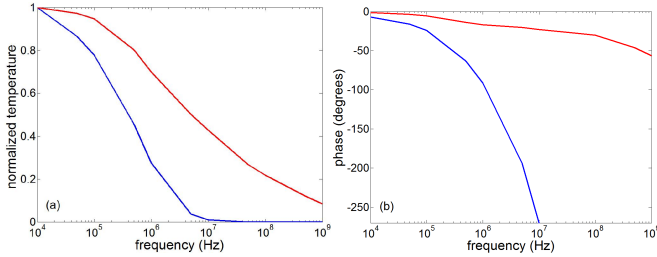


Fig. 2. Normalized amplitude (a) and phase (b) of the temperature oscillations in P_1 (red) and P_2 (blue) versus P_{diss} frequency ($P_{DC}=40mW$, $P_{AC}=2mW$).

expected; in particular, since δ is inversely proportional to \sqrt{f} , the volume of the silicon that effectively contributes to Z_{th} reduces if the frequency increases. To show this behavior and understand how the induced temperature variations will penetrate in the transistor, 3D thermal simulations using Sentaurus TCAD have been performed on the transistor structure in Fig. 1 representing an HBT from the Infineon B11HFC technology ($A_E=5 \times 0.2 \mu m^2$). In these simulations the thermal conductivity degradation due to high doping is taken into account, according to experimental data in [18] and [19]. A planar heat source (HS) is placed at the base-collector (BC) junction and isothermal conditions are applied at the back surface of the wafer and at the top, above a $15 \mu m$ thin air layer acting as a laminar sub-layer, in which just conduction can be considered [20]; due to the very low k of air ($0.024 W/mK$) this boundary condition is very close to be adiabatic. Sinusoidal power stimuli are applied to the HS, at frequencies ranging from 10kHz to 1GHz.

In Fig.2 are plotted the normalized amplitude and the phase of the simulated temperature oscillations, for two different positions P_1 and P_2 (respectively 80nm and $6.38 \mu m$ below HS). It can be observed that their amplitude will tend to reduce if the frequency is increased, due to the intrinsic thermal capacitance (C_{th}) of the structure. Moreover if the distance from the HS is higher, oscillations will tend to disappear; in fact in P_1 significant oscillations (20% of the temperature variations simulated at DC) are visible till a frequency of 100MHz, whereas the same relative amplitude is already reached at 1MHz in point P_2 . The absolute value of the thermal oscillations is $20^\circ C$ in P_1 and $0.9^\circ C$ in P_2 at a frequency of 10kHz.

It can be also noticed that the phase shift will increase if the frequency of the P_{diss} increases; furthermore in P_2 the phase shift becomes more evident, since the distance from the heat source is higher than in P_1 and thus a longer time is needed for the thermal variations induced from the HS to travel through the

HBT structure. If instead we fix a frequency and have a look at the distribution of the amplitude of the thermal oscillations within the transistor, we will have a direct image of the spatial distribution of δ . As reported in Fig. 1, at 100MHz the thermal variations are only visible in a small volume around the BC.

III. THERMAL PENETRATION DEPTH EXPERIMENTAL STUDY

To investigate how the thermal oscillations induced by a sinusoidal power dissipation affect the behavior of a real transistor and to estimate the penetration depth inside the component, dedicated test structures need to be designed. If a sinusoidal P_{diss} is applied, as shown in the previous section, temperature oscillations are induced in the lower part of the HBT, but, of course, they are also present in the BEOL. It is therefore possible to study these thermal penetration phenomena by characterizing and comparing the thermal behavior of transistor structures in which the lower part of the device is kept unaltered, whereas modifications are made in the BEOL region (during the design there is in fact a certain degree of freedom on the geometry of the different metal layers).

The HBTs under study in this work consist of five-fingers SiGe HBTs realized in STMicroelectronics B55 technology, of which a complete thermo-electrical characterization has been reported in [21]; in this section we will further extend our study, showing the thermal impedance extracted from LF S-parameter measurements in the range 10kHz-1GHz. In particular, we will now focus on the set of test structures named VM, for which copper metal dummies, acting as heat spreaders, are present upon the emitter contacts till metal-3 (VM3), metal-6 (VM6) and metal-8 (VM8); in a reference transistor named VM1 the metallization on the emitter contacts stops instead at metal-1 level (refer to Fig.3). It must be pointed out that the R_{th} value of these transistors is lowered as higher levels are reached for the metallization in the BEOL [22]–[24], since the heat flux can find an alternative path in the copper of the BEOL (the results for the R_{th} of these HBTs are detailed and reported in [21]).

An accurate design of the metal connections can thus lead to improved SOA specifications [21] and better RF performances [22]. Moreover, as it is suggested by equation (1), δ is inversely proportional to the square root of the P_{diss} frequency, which means that, at low frequencies, the thermal oscillations can significantly penetrate the structure, both downwards (towards the back of the wafer) and upwards, till eventually reaching the higher levels of the metal in the BEOL. In this scenario, the different Z_{th} trend observed at LF among the HBTs under study (Fig. 4), is due to the fact that δ has reached a distance within the abscissas of the metal dummies, and so transistors having heat spreaders till higher levels of metal will exhibit a lower Z_{th} . In the high frequency range, instead, all the VM transistors show an identical Z_{th} decay, in fact the thermal oscillations will tend to be confined in close proximity to the heat source as the frequency increases; since within this region all the transistor structures are identical (Fig.3), their Z_{th} will be the same.

From a physical modelling point of view, at low frequencies, temperature oscillations will interest a considerable volume of silicon around the HS, so it can be considered that high valued C_{th} are thermally charged and discharged. It is in fact possible

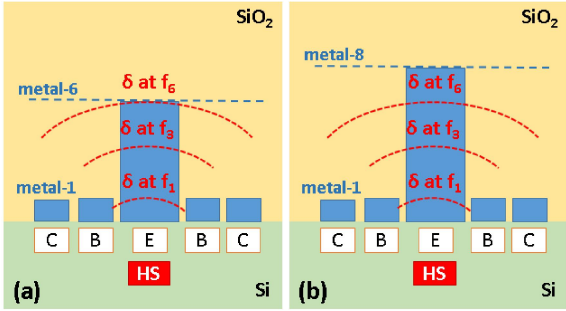


Fig. 3. Representation of the VM6 (a) and VM8 (b) transistors, showing the different levels of metal dummies and the δ at different frequencies

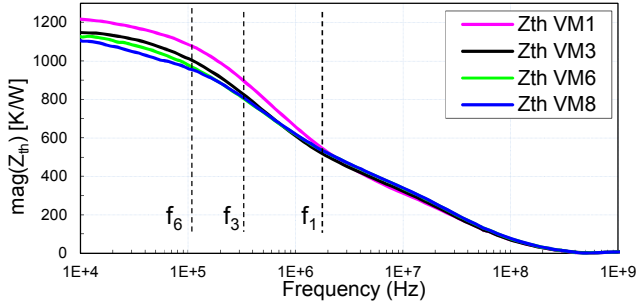


Fig. 4. Extracted Z_{th} versus frequency for the VM test structures.

to take into account the presence of the copper dummies in the VM transistors by adding big thermal capacitances in parallel to the thermal network of the lower part of the transistor [25]. These added C_{th} determine the thermal behavior at LF, but, as the frequency increases, the overall big volume of copper in the BEOL cannot participate to the temperature oscillations, due to its intrinsic thermal inertia; the AC dynamic phenomena can be rather approximated to happen in a small portion of silicon surrounding the BC junction.

It is interesting to notice, observing Fig. 4, that going from the highest frequencies (where all the VM transistors exhibit an identical Z_{th} trend) towards the lowest, we can identify a frequency f_1 (around 2MHz) starting from which the Z_{th} of VM1 starts to deviate from the others. This means that, at f_1 the thermal penetration depth has reached the abscissa corresponding to metal-1; the same assumption can be made as the frequency decreases, and it is also possible to identify f_3 and f_6 , where δ reaches respectively the levels 3 and 6 of metallization. The set of test structures under study in [21] also allows an investigation of the penetration depth in the horizontal plane: the thermal diffusion phenomena under study have in fact an isotropic nature. Among the structures presented in [21], the transistor named HL1 contains metal connections reaching the same level as VM3, but has an increased Deep Trench Isolation (DTI) enclosed area. HL1 thus allows a wider angle for the lateral heat spreading, which in turn ensures a better evacuation of the heat generated from the HS towards the silicon substrate, yielding a lower R_{th} [21].

Comparing the Z_{th} of the HL1 and VM3 transistors shown in Fig. 5, it is again noticed that increasing the DTI enclosed area yields a decrease in the Z_{th} at low frequency. At higher frequencies, though, it is just the volume in close proximity of the HS that determines Z_{th} , and it can be supposed that, in this situation, the thermal variations do not reach the DTI, which

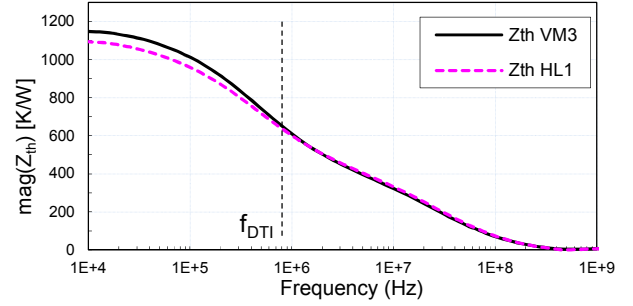


Fig. 5. Extracted Z_{th} versus frequency for the HL1 and VM3 transistors.

restricts the heat flux. The condition that thermally favors HL1 does not hold any more, and the two structures tend to behave the same way for frequencies higher than around 1MHz (f_{DTI} in Fig. 5), where we can assume that δ has reached, in the horizontal plane, the adiabatic wall represented by the DTI.

IV. CONCLUSIONS

In this letter we have shown, by means of thermal 3D simulations and reporting Z_{th} measurements on specially designed transistor structures, how dynamic thermal mechanisms take place in SiGe HBTs from state-of-the-art technology nodes; in principle, though, similar thermal phenomena also take place in devices implemented in other technologies.

We demonstrated how, at different operating frequencies, the thermal impedance influences the spatial distribution of the temperature fluctuations within the transistor structure: at high frequencies, sinusoidal temperature variations are still present, even if they tend to be confined in the region close to the HS.

In the experimental part it has been shown how a specially conceived set of DUTs can allow to identify the frequencies at which the temperature oscillations imposed by a sinusoidal P_{diss} reach a certain distance from the HS. This can be of interest in the development of physical thermal models for the Z_{th} ; the measured $Z_{th}(f)$ decays reported, in fact, clearly show a distributed nature. It is therefore strongly recommended to use at least a three poles network (instead of a single pole normally used in compact models) to accurately take into account dynamic thermal effects in the low frequency range. This is particularly important in circuit designs where IMD3 products arise within the thermal bandwidth of the HBTs.

Besides it is experimentally demonstrated that the configuration of materials in the BEOL, although far from the HS, has a non-negligible thermal impact: in particular the presence of metal connections can considerably affect the Z_{th} decay at LF. In the same way, if the transistor layout is altered, (e.g. enlarging the DTI enclosed area) Z_{th} variations should be rather present in the LF range, but it must be pointed out that instead at frequencies starting from around 1-2 MHz the same Z_{th} trend has to be expected, regardless of any modifications of the HBT structure in the vertical or horizontal plane.

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