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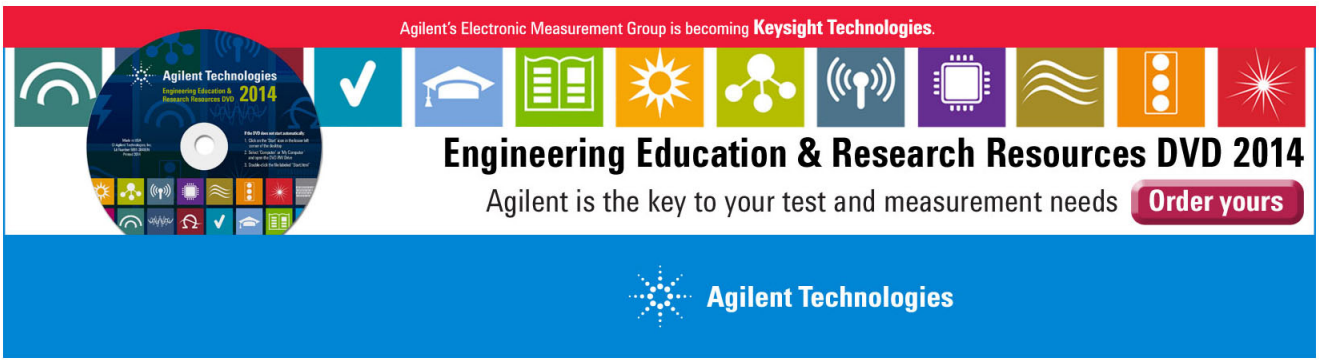

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HTML ABSTRACT + LINKS

Origin and repartition of the oxide fixed charges generated by electrical stress in memory tunnel oxide

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A method is proposed to determine the origin and the spatial oxide fixed charge repartition in memory tunnel oxide from Fowler–Nordheim current measurements after electrical stress. The Poisson equation resolution in the dielectric layer is required to account for the nonsymmetric tunneling barrier deformation, resulting from charges generated within the dielectric layer. From current–voltage characteristics measurements and simulations, we have determined the spatial distribution of the oxide fixed charges within the dielectric layer of metal/SiO_2/metal structures. In addition, the kinetics of the oxide charge generation can be explained by a dispersive hydrogen transport model. © *2004 American Institute of Physics.* [DOI: 10.1063/1.1756681]

Usually, the tunneling current flowing through the gate insulator in metal–oxide–semiconductor (MOS) structures is calculated without considering the influence of dielectric bulk charges on the shape of the tunneling barrier.[1–3] However, it is well known that the electrical properties of MOS structures depend much on electrically active defects. In this work, we describe a method to determine the nonuniform dielectric fixed charge distribution induced by electrical stress of metal/SiO_2/metal structures, based on the analysis of tunneling currents after electrical stress. Our approach lies in the continuity of the work of Ku *et al.*[4] which have performed an analytical resolution of Poisson equation in the case of a uniform fixed charge repartition. It is also shown that the kinetics for the oxide fixed charge buildup can be explained by a dispersive hydrogen transport model.

In this study, the tunneling oxide capacitor, with area $W\times L=1000\times 75\ \mu m^2$, is assumed to be equivalent to three series capacitances:[5] a highly doped silicon electrode (n type) with $N_{Sub}=1.5\times 10^{25}\ m^{-3}$, an oxide layer with $t_{ox}=8.3$ nm, and a highly doped n-type polysilicon electrode (gate electrode) with $N_G=1.2\times 10^{26}\ m^{-3}$. The relationship between the two surface potentials, Ψ_S and Ψ_G (for the substrate and the gate, respectively), and the gate voltage, V_{GB}, is given by

$$V_{GB}=\Phi_{MS}-\frac{Q_{ox\,eff}}{C_{ox}}+\Psi_S-\Psi_G-\frac{Q_{SC}(\Psi_S)}{C_{ox}}, \tag{1}$$

where C_{ox} is the oxide capacitance, Φ_{MS} is the gate–semiconductor work function difference, Q_{SC} is the total bulk charge, and $Q_{ox\,eff}$ is the effective charge density seen from the bulk interface. For a given gate voltage and a given dielectric charge density, the spatial distribution of the dielectric potential, V, is calculated from Poisson resolution within the dielectric layer using a three-point finite difference method and the following boundary limits:

$$\begin{cases} V_{(y=0)}=0 \\ V_{(y=t_{ox})}=-\dfrac{Q_{SC}+Q_{ox\,eff}}{C_{ox}}, \end{cases} \tag{2}$$

where y is the distance from the bulk (silicon electrode).

Then, using Wentzel–Kramer–Brillouin approximation,[6] we express the current, due to the tunneling of electrons from the substrate to the gate (I_{si}) and from the gate to the substrate (I_{poly}), respectively,

$$I_{si,poly}=A_{eff}Q_{n\,si,poly}\times F_{imp}\left[\exp\left(-2\sqrt{\frac{2qm_{nox}}{\hbar^2}}\int_0^{t_{ox}}\sqrt{\Phi_{b\,si,poly}}dy\right)\right], \tag{3}$$

where A_{eff} is the effective area of the capacitor, Q_n is the inversion charge in the substrate (Q_{nsi}) and in the gate (Q_{npoly}), F_{imp} is the impact frequency, Φ_b, is the barrier height between the silicon, Φ_{bsi} (or polysilicon, Φ_{bpoly}) conduction band and the dielectric conduction band, and m_{nox} is the electron mass in oxide. Figures 1 and 2 illustrate the current–voltage ($I-V$) characteristics of two different capacitors measured after cumulative times of negative (−9.5 V) and positive (8 V) gate voltage stress, respectively.

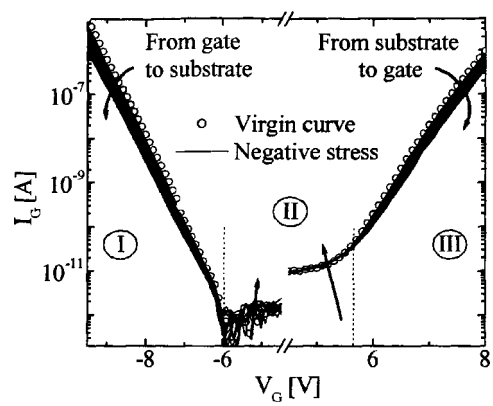

FIG. 1. $I-V$ characteristics of the capacitor recorded after cumulative times of negative gate voltage stress (−9.5 V).

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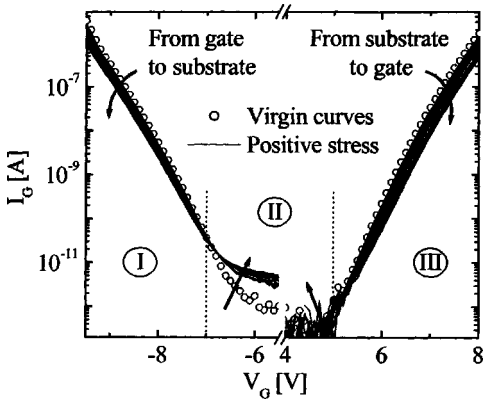

FIG. 2. $I-V$ characteristics of the capacitor recorded after cumulative times of positive gate voltage stress (8 V).

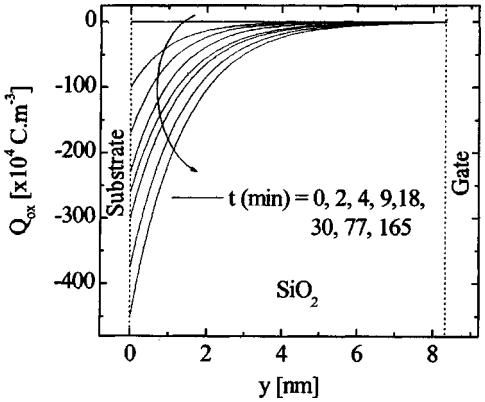

FIG. 4. Decreasing exponential distribution of the trapped oxide charges used to fit the measurements shown in Fig. 3.

In Figs. 1 and 2, we will only discuss parts I and III which correspond to a decrease in the Fowler–Nordheim tunneling current. This phenomenon is well known as the closure of the programmable window observed after numerous write–erase operations in EEPROM cells.[7] We observe, in Figs. 1 and 2, a more pronounced current decrease for the injection of electrons from gate to substrate for a negative stress, and from the substrate to the gate for a positive stress. Based on this dissymmetric behavior of the tunneling current, we have compared three different negative oxide fixed charge distributions: Constant, Gaussian, and exponential. The constant oxide fixed charge distribution did not allow us to fit the experimental data for both positive and negative voltages. This result shows that the distribution of the fixed charge, generated by electrical stress within the dielectric layer, is nonuniform. In the following, we detail only our results for positive stress.

Considering a Gaussian oxide charge repartition, the maximum of charge density must be located close to the substrate/oxide interface. However, the best fits to the data (shown as solid lines in Fig. 3) have been obtained by considering a decreasing exponential charge distribution (cf. Fig. 4):

$$Q_{ox} = Q_{max} \exp\left(\frac{-y}{\lambda}\right) + Q_{min}, \tag{4}$$

where Q_{min} is the oxide charge in the virgin sample, Q_{max} is the maximum value of the oxide trapped charges during the stress, and λ is the decay length. The increases in the $|Q_{max}|$ and λ values (from 0 to 450×10^4 C m^{-3} and from 0 to 16.25 Å, respectively) correspond to a trapped oxide charge moving away from the interface during the electrical stress. Let us remark that the determination of the oxide charge distribution using the two-level charge pumping technique on MOS transistors after electrical stress shows the same kind of spatial distribution for the oxide traps.[8]

Figure 5 shows the impact of a negative fixed charge in the dielectric layer close to the silicon electrode, which induces a band diagram deformation on this area. This result can only be obtained by Poisson resolution within the dielectric layer. It clearly appears that after positive stress, electron tunneling current is more degraded for a positive voltage than for a negative voltage (cf. Fig. 2). Symmetrically, in case of negative stress (cf. Fig. 1), the induced fixed charges would be located close to the polysilicon electrode. Let us remark, that for EEPROM cells, the write–erase operations would lead to two decreasing exponential distributions of the oxide fixed charges (one on the silicon side and the other on the polysilicon side) which form one U-shaped curve.

A possible origin for the exponential negative fixed charge distribution in the oxide can be the release of hydrogen species at the Si/SiO_2 interface by an impacting electron during the stress. Then, the hydrogen species transport throughout the gate oxide and their subsequent trapping into

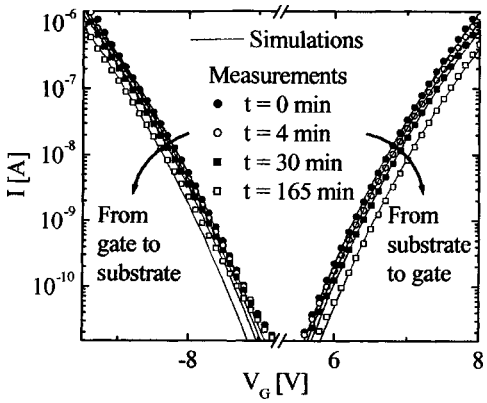

FIG. 3. Comparison of simulated and measured $I-V$ characteristics of the capacitor after cumulative positive stress, under gate injection and substrate injection.

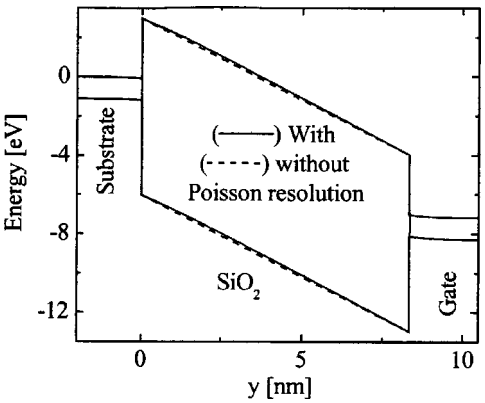

FIG. 5. Band diagram obtained with and without Poisson resolution within the SiO_2 layer for the exponential negative fixed charge distribution at $VG = 8$ V after 165 min.

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the oxide network lead to the generation of Si—O—H defects close to the interface. These defects are efficient electron trapping centers,[9] forming SiO^- defects which could correspond to the negative oxide charge generated during the stress. From these assumptions, the kinetics of Si—O—H precursor sites generation has been calculated within a dispersive transport model,[10,11] where the charge generation is assumed to be limited by the random hopping of H^+ and its trapping in the SiO_2 layer.

Within this model,[10] the kinetics of charge density variation ΔN_{ox} is given by

$$\Delta N_{ox} = N_H^+ \left(1 - \int_0^1 SiO_2 G_{SiO_2}(y) dy \right), \quad (5)$$

where N_{H+} is the density of protons close to the Si/SiO_2 interface and $G(y)$ is a function related to the probability $P(x,t)$ for finding a proton at a distance x at time t; the "improved trial function" described by McLean and Ausman[12] is used here for approximating $G(y)$. In Eq. (5), $\ell_{SiO2} = x_c / \ell_h t^\alpha$, where x_c is the position of the hydrogen-induced defect centroid, ℓ_h is the average proton hopping distance, and α is a parameter characterizing the dispersiveness of the proton transport in the material. We fixed here $\ell_h = 2.5$ Å and $\alpha = 0.3$, consistently with values reported in SiO_2.[10,11] The kinetics of oxide charge generation derived from the data in Fig. 3 are compared to the model in Fig. 6. A very good agreement is obtained, with realistic values for $N_{H+} = 4 \times 10^{13}$ cm^{-2} and $x_c = 3$ nm, suggesting that the defect precursors for the negative charge generation could be Si—O—H centers.

To summarize, we have presented a method to determine the spatial oxide fixed charge repartition in memory tunnel oxide. This method is based on the Poisson equation resolution in the dielectric layer and presents the advantage to consider an arbitrary spatial distribution of oxide fixed charges. From $I-V$ measurements after positive (or negative) stress and Poisson resolution within the dielectric layer, we have found a decreasing exponential distribution of the fixed dielectric charge with a maximum value at the substrate/SiO_2 (or SiO_2/gate) interface. A possible explanation for this decreasing exponential distribution has been given from the generation of Si—O—H precursor defects close to the substrate/oxide interface, most probably leading to the creation of SiO^- charges upon subsequent electron trapping.

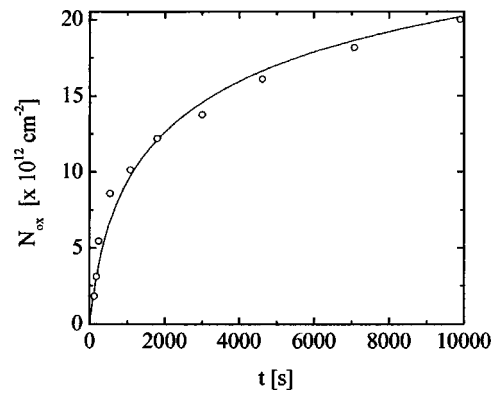

FIG. 6. Oxide charge kinetics comparison between the charge distribution used to fit the measurements shown in Fig. 3 (open circles) and the simulations obtained from a dispersive transport model (solid line).

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