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Influence of PE-ALD of GaP on the Silicon Wafers Quality

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An attractive method of low-temperature plasma-enhanced atomic layer deposition (PE-ALD) of GaP on silicon wafer was recently proposed. In the present paper, the influence of the growth process on the quality of silicon wafers is explored by space charge capacitance techniques, *C–V* profiling and deep level transient spectroscopy (DLTS). No DLTS peak is observed for PE-ALD GaP deposited onto n-type wafer, meaning that the defect concentration is very low (less than $1 \times 10^{12}\,cm^{-3}$) and that the growth process does not affect the properties of the n-Si wafer. For boron-doped p-type silicon, *C–V* profiling shows that there is no deactivation of boron doping after the PE-ALD process, as could have been expected from the presence of hydrogen in the plasma. Measurements on the reference Schottky diodes formed on the p-type Si wafer reveal the presence of the well-known Fe interstitial defects at the position $E_V + 0.38\,eV$ with a concentration of $3 \times 10^{13}\,cm^{-3}$. PE-ALD of GaP leads to a modification of the response of this defect and to the appearance of another response in the low temperature range, possibly related to changes in the Fe interstitial defect environment or configuration. However, deep-levels were not detected in p-Si after PE-ALD, meaning that the quality of p-Si does not degrade.

1. Introduction

High-efficiency and low-cost of solar cells are the driving forces for the success of photovoltaics in terrestrial applications. The highest efficiencies are obtained for multi-junction solar cells based on III–V compounds (GaAs, GaInP, GaNAs, etc.). In 2015 multi-junction solar cell based on III–V semiconductors have achieved record efficiency of 46% (concentrator).[1] For space applications, where the key factors are the efficiency and resistance to radiation triple-junction solar cells based on the GaInP (1.85 eV)/GaAs (1.42 eV)/Ge (0.7 eV) system are industrially used. However, cost of wafers (Ge, GaAs, InP, etc.) and expensive growth methods (molecular-beam (MBE) and vapor-phase epitaxy (VPE)) are major drawbacks to the extension of low-cost solar cells based on III–V compounds to terrestrial usage. On the other hand, silicon industry is much more developed than that of III–V semiconductors and silicon is one of the most abundant element in the Earth, so the cost of growth and processing for silicon solar cells is much lower. Thus, majority of terrestrial solar cells (90%) are fabricated from silicon. However, record efficiency solar cell based on silicon is slightly above 26%[2] and it almost reaches the theoretical limit for single-junction silicon solar cell.

PV requires new approaches for high-efficiency and low-cost solar cells, which can combine the advantages of III–V multi-junction and silicon solar cells. Therefore, fabrication of multi-junction solar cells with active layers of III–V compounds on silicon wafers is a very promising approach for the photovoltaic industry. Growth of III–V semiconductors on silicon wafers is a real challenge for scientists, because such a technology can open the way to the fabrication of optoelectronic integrated circuits. Gallium phosphide is one of the most perspective candidates for fabrication of multi-junction solar cells on silicon wafers. Firstly, lattice mismatch between Si and GaP is only 0.4% so GaP can be grown on silicon for the fabrication of the bottom subcell based on GaP/Si heterojunction by different epitaxial methods (MBE and VPE).[3,4] Further, novel materials (In)GaP(NAs) with small nitrogen content (called dilute nitrides) can be lattice-matched to GaP. These materials can be grown as active layers for top subcells with a wide range of bandgap values, 1.5–2.1 eV.[5]

Previous efforts on the growth of dilute nitrides GaPNAs on Si wafers have not allowed one to reach high efficiencies due to the low quality of layers in solar cells.[6] Temperature of 800–900 °C required during growth process is a possible reason for the low performance of solar cells for MBE and VPE epitaxial methods.

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Firstly, the GaP/Si heterojunction can be deteriorated due to inter-diffusion of atoms at the III–V/Si interface and different values of thermal expansion coefficient. Secondly, such high temperatures lead to degradation of bulk properties of silicon wafer due to activation of centers of non-radiative recombination.[7,8]

Recently, a new growth approach was proposed[9] which can allow one to avoid these negative impacts during growth of GaP on silicon wafers. The technology is based on plasma-enhanced atomic-layer deposition (PE-ALD) with alternation of P and Ga sources at low temperature (below 400 °C). In our previous work, we explored GaP/n-Si heterojunctions and showed differences between amorphous (a-GaP) and microcrystalline (μc-GaP) GaP grown by PE-ALD using deep-level transient spectroscopy (DLTS). We detected two responses with activation energy of 0.30 and 0.80 eV in μc-GaP/n-Si heterojunction and no response in a-GaP/n-Si.[10] In the present study we describe the influence of PE-ALD growth on the properties of silicon wafers by space charge capacitance measurements, because the wafer quality is a very crucial issue for the performance of solar cells based on GaP/Si heterojunction.

2. Results and Discussion

2.1. Samples and Methods

Firstly, thin films of GaP with thickness of 50–75 nm were grown at 380 °C on p-type (boron-doped, 0.8–1.2 Ω cm) and n-type (phosphorus-doped, 2–7 Ω cm) (100) silicon wafers by PE-ALD using an Oxford PlasmaLab System 100 PECVD (13.56 MHz) setup. Phosphine (PH_3) and trimethylgallium (TMG) were alternatively changed with continuous plasma discharge due to constant hydrogen (H_2) flow during the growth and purge steps. The total flow and pressure were kept constant and equal to 100 sccm and 350 mTorr, respectively. Detailed description of technological process is given elsewhere.[9] We obtained two different types of structures with either amorphous (a-GaP) or microcrystalline (μc-GaP) layers of gallium phosphide, as detailed in Ref. [10]. Structural properties strongly depend on RF plasma power applied during deposition steps. Thus a-GaP and μc-GaP layers were obtained at RF power of 20 and 100 W, respectively. Then, mesa-structures were created for measurements of the silicon wafers properties by space charge capacitance techniques. For this purpose, Schottky barrier structures were fabricated onto the silicon wafers with the processing steps described below.

In the first step, the GaP layers were selectively removed by wet etching. For n-type silicon, a layer of 50 nm of n-type hydrogenated amorphous silicon ((n)a-Si:H) was deposited on the bottom of the wafer in the PECVD chamber. Silver was vacuum evaporated onto (n)a-Si:H for creation of the contact which became ohmic after thermal annealing at 170 °C during 20 min in the air atmosphere. Then, gold dots with diameters of 0.5 and 1 mm were evaporated on the top of the n-type silicon wafer to form Schottky diodes to n-Si (Au/n-Si). For p-type silicon, indium was used as an ohmic back contact instead of silver/(n)a-Si:H in the case of n-Si. Also, Schottky barrier to p-Si were fabricated by evaporation of a titanium layer which was covered by a gold layer to protect the contact (Au/Ti/p-Si) during dry etching. Finally, mesa structures were formed by dry etching of 2 μm of silicon using an Oxford PlasmaLab System 100 ICP 380. Furthermore, reference samples were fabricated with the same top Schottky diode and back ohmic contact to the initial p-type silicon wafer (i.e., without the GaP deposition and etching sequence). The schematic view of both Schottky barrier structures is shown in **Figure 1**.

Space charge capacitance techniques are very common for characterization of properties of semiconductor materials. In the present work, we used capacitance–voltage (C–V) measurements and deep-level transient spectroscopy (DLTS). Measurements of C–V and DLTS were performed using a liquid nitrogen cryostat in the temperature range of 80–400 K. Using C–V measurements at high frequency (100 kHz), profiles of effective concentration of free carriers (N_{CV}–W) were estimated in the depletion layer approximation by:

$$N_{CV} = \frac{2}{q\varepsilon_r\varepsilon_0}\left(\frac{dC^{-2}}{dV}\right)^{-1} \quad (1)$$

where C is the capacitance per unit area, ε_0 is the permittivity of vacuum, ε_r is the relative permittivity, and q is the elementary charge. The obtained value of N_{CV} corresponds to the free carrier concentration at the edge of the space charge region, W, that is simply obtained from the capacitance as $W = \varepsilon_0\varepsilon_r/C$. DLTS is an attractive method for the exploration of defect levels in semiconductors,[11] which allows one to estimate their important properties: activation energy (E_a), namely the energy position of the defect with respect to the band edge, capture cross-section (σ_a) and concentration (n_a). An automated setup based on a Boonton-7200B capacitance bridge was used for measurements by the classical DLTS method in our experiments.

2.2. Schottky Barrier Diode of Au/n-Si

According to Ref. [10] two defect levels were detected in μc-GaP/n-Si heterojunctions and no one in a-GaP/n-Si. Therefore, we spend more attention to n-type silicon wafer after PE-ALD process when μc-GaP was grown. N_{CV}–W profiling (see inset of **Figure 2**) shows constant concentration of charge carriers in silicon with estimated value of 1×10^{15} cm^{-3} which corresponds to the n-type doping level in the wafer. DLTS spectra $S(T)$ of Au/n-Si are shown in Figure 2 for the following experimental

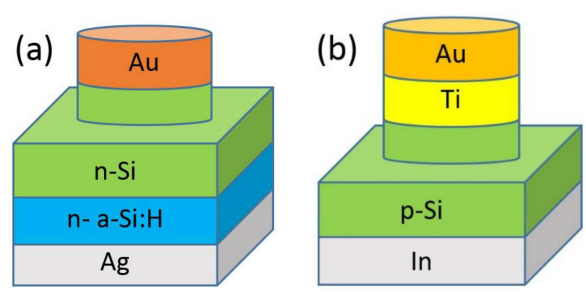

Figure 1. Schematic view of Au/n-Si (a) and Au/Ti/p-Si (b) structures.

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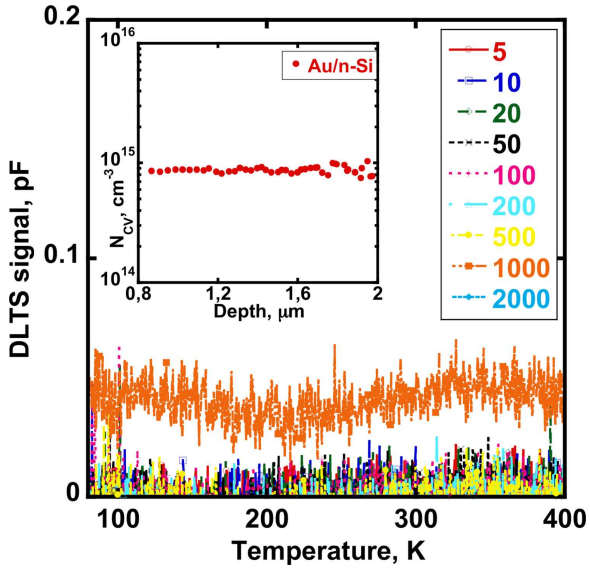

Figure 2. DLTS spectra $S(T)$ measured on Au/n-Si for different emission rates (in s^{-1}) obtained by changing the DLTS gate window. Inset shows the N_{CV}–W profile.

conditions: reverse bias of 2 V, amplitude and duration of filling pulse of 2 V and 50 ms, respectively. There are no peaks in the $S(T)$ curves whatever the emission rates in the explored temperature range, meaning that the concentration of defects is below the detection limit (estimated at 10^{12} cm^{-3}) in bulk n-Si after PE-ALD growth process. Therefore, earlier detected defects in the μc-GaP/n-Si structure originate from the μc-GaP layer. Furthermore, it shows that our low temperature PE-ALD growth of GaP does not lead to the deterioration of wafer quality in n-type silicon wafers. The latter conclusion is very important for future research on GaP/n-Si heterostructures grown by PE-ALD. Indeed if responses would detected by DLTS in such heterojunction structures they would be attributed to the GaP layers or to the GaP/n-Si interface.

2.3. Schottky Barrier Diode of Au/Ti/p-Si

Recently, it was theoretically simulated and experimentally confirmed that the n-GaP/p-Si heterojunction has advantages over the p-GaP/n-Si one for photoelectrical structures grown by MBE.[12] Thus, influence of PE-ALD growth process of GaP on p-type silicon quality is a crucial issue for future performance of high efficiency multi-junction solar cells. Here we present measurements of three samples which were fabricated using p-type silicon wafer as described above in Section 2.1: Au/Ti/(p) Si the reference (ref) sample (i.e., no PE-ALD of GaP), a-PE-ALD is a Schottky barrier form on p-Si after etching of amorphous GaP, μc-PE-ALD is a Schottky barrier to p-Si after etching of microcrystalline GaP. For these samples $1/C^2(V)$ curves and N_{CV}–W profiles (**Figure 3**) were plotted from capacitance–voltage measurements (not shown here) at 80 K.

For all samples $1/C^2(V)$ curves have linear behavior so the charge carrier concentration is uniform in p-type silicon. N_{CV}–W

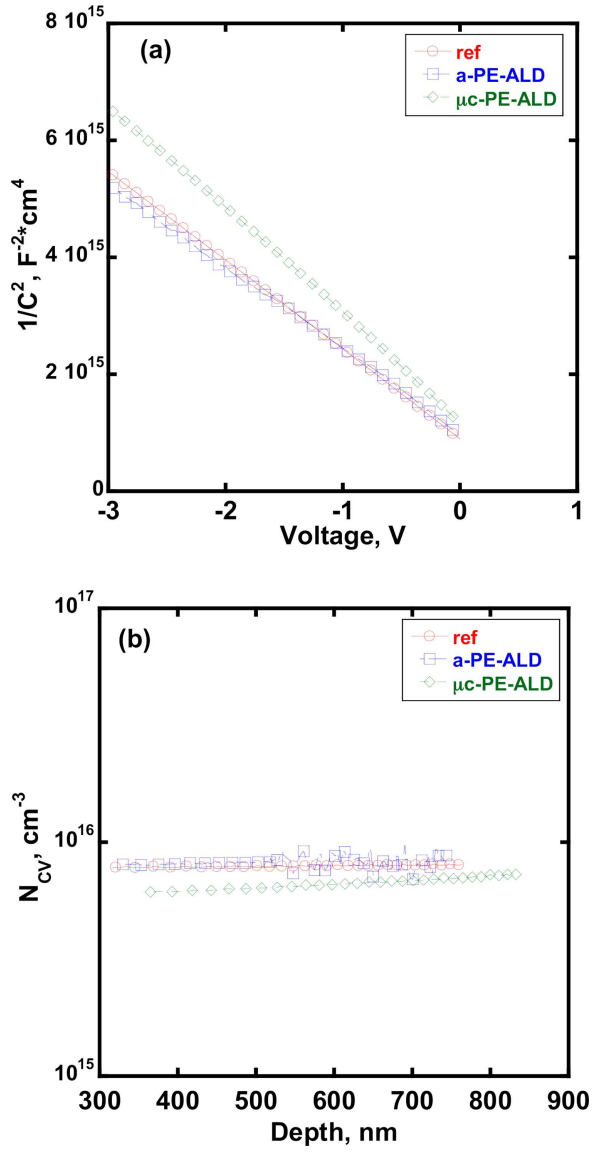

Figure 3. Analysis of the bias dependence of the measured capacitance of the three structures: $1/C^2$–V (a) and N_{CV}–W (b).

profiles show a constant concentration value of 1×10^{16} cm^{-3} which corresponds to the boron concentration in silicon. This means that we do not observe passivation of boron doping after PE-ALD growth process, which is an encouraging result since it is a typical problem for solar cells based on a-Si:H/p-Si heterostructures due to interaction between hydrogen atoms from the plasma and boron atoms in the silicon wafer during the growth process. It leads to non-linear behavior of $1/C^2(V)$ as a sharp drop when the space charge region approaches the heterointerface.[13–15] In our case, hydrogen plasma is also used during low-temperature PE-ALD growth of GaP, but it does not lead to boron passivation in p-Si. The estimated intercept voltage for $1/C^2(V)$ curves are close for the three samples: 0.60 eV for reference, 0.73 eV for a-PE-ALD, and 0.70 eV for μc-PE-ALD. It means similar value of Schottky barrier height 0.65–0.75 eV for

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Ti/p-Si at 80 K, but it is slightly higher than 0.61 eV obtained at room temperature.[16] However, the value of Schottky barrier height should increase with decreasing temperature, so characteristics of explored samples are in good correlation with literature data.

Further, DLTS spectra $S(T)$ of reference wafer of p-type silicon was measured under the following experimental conditions: reverse bias of 0.2 V, amplitude and duration of filling pulse of 0.2 V and 50 ms, respectively. Results are shown in **Figure 4**.

DLTS spectra exhibit peaks, which are characteristic for the response from defect levels. Indeed a peak is observed when the characteristic time fixed by the DLTS gate window corresponds to the emission rate from the defect level, e, given by:

$$e = AT^2 e^{-E_a/k_B T}, \tag{2}$$

where A is a pre-exponential factor, E_a is the activation energy of the defect level, and k_B is Boltzmann's constant. Experimental peaks are narrow and have almost the same amplitude for different emission rates. It means that the response comes from point defects in silicon. The activation energy and the pre-exponential factor can be estimated directly from a linear fit of e/T^2 in an Arrhenius plot, and the capture cross section is then deduced from A. Activation energy and capture-cross section for detected defects in reference p-Si are 0.38 eV and 1.8×10^{15} cm^{-2}, respectively. Defect concentration was estimated from the peak amplitude at 3×10^{13} cm^{-3}. DLTS peaks have a positive value so the detected responses correspond to traps for majority charge carriers in p-Si. Therefore, the energy position of the defect level is $E_V + 0.38$ eV and the capture cross section is that for holes. This defect is common for boron-doped p-type silicon and can be attributed to interstitial iron in Si (Fe_i).[17,18]

The existence of Fe_i in our initial silicon wafer is a drawback if we want to properly study the effect of the PE-ALD process on the silicon wafer, so we will use better quality silicon wafers in the future to exclude the influence of initial defects on the detection of potential defects after the PE-ALD process.

DLTS spectra $S(T)$ were obtained for Schottky diodes on silicon wafers, where a-GaP and μc-GaP were wet etched (**Figure 5**a and b, respectively). Measurements were done for reverse bias of 0.2 V, amplitude and duration of filling pulse were equal to 0.2 V and 50 ms, respectively. Both DLTS spectra show a similar shape of DLTS peaks that is different from that in the reference sample. All peaks in the reference sample are narrow and symmetric: it means that the response is from point defects. However, peaks in both samples in Figure 5 have broadened asymmetric shape with blurred low-temperature

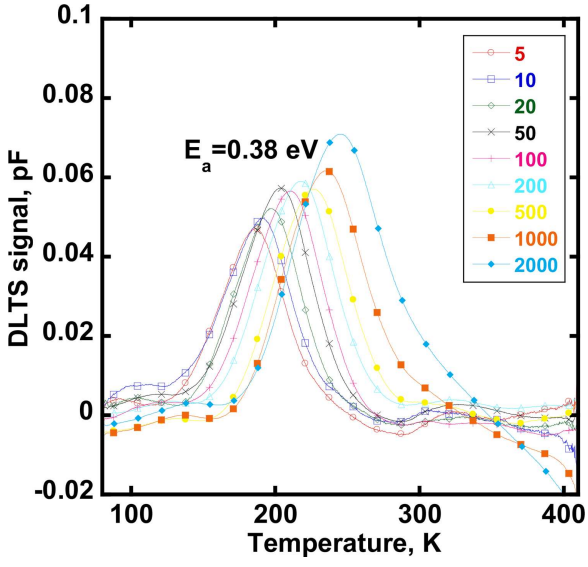

Figure 4. DLTS spectra $S(T)$ of reference Au/Ti/p-Si for different emission rates (in s^{-1}) obtained by changing the DLTS gate window.

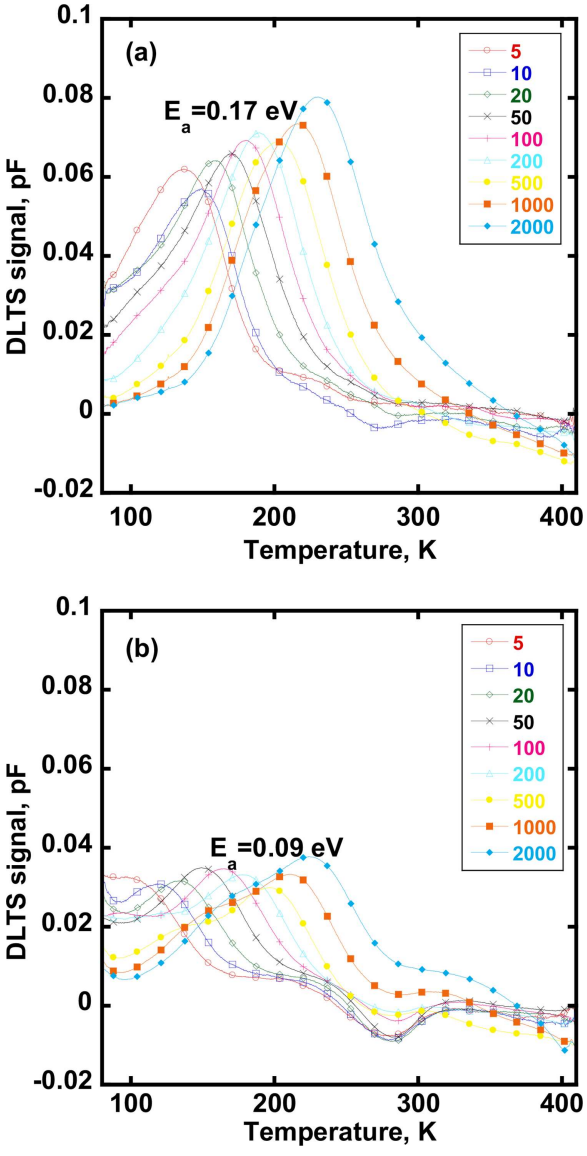

Figure 5. DLTS spectra $S(T)$ of Au/Ti/p-Si after etching of a-GaP (a), and μc-GaP (b) for different emission rates (in s^{-1}) obtained by changing the DLTS gate window.

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side. There are dominant peaks in the temperature range 150–220 K, but estimated values of activation energy are different for a-PE-ALD (0.17 eV) and μc-PE-ALD (0.09 eV) samples. Nevertheless, peak positions suggest that the defects may have the same nature as those detected in the reference sample above. Discrepancy of activation energies comes from overlapping of responses from few defect levels in these structures. Responses from another defect in the low temperature range are the main differences between the reference sample and that after PE-ALD process. Detailed observation of $S(T)$ spectra allows us to propose the existence of a second defect in the temperature range 80–150 K. However the estimation of its parameters is complicated, because the peak is wide and its amplitude is lower than that of the high-temperature peak. The latter became wider after growth process and his amplitude decreased for μc-GaP sample. This suggests that the initial Fe_i configuration could be modified after the PE-ALD process. Temperature of growth of the GaP layers is 380 °C which could lead to migration of irons and change of its surroundings due to high diffusion coefficients. Additionally, the plasma treatment of the Si surface takes place, which could lead to local heating. Indeed for μc-GaP grown with significantly higher RF power DLTS spectra are strongly modified. Therefore, future experiments will be focused on research of influence of plasma power on defect modification in silicon wafer.

Nevertheless, we do not detect responses which can be associated with defect levels at temperatures above 250 K. Therefore, it can be concluded that the PE-ALD growth process does not lead to the formation of deep-levels with high activation energy, suggesting that the quality of boron-doped p-type silicon would not be hardly deteriorated during growth of GaP by PE-ALD. This assumption is valid for studied samples grown at RF power of 20 and 100 W and at low temperature 380 °C not leading to deep level formation. Future experiments will be focused on improvement of crystal quality of GaP by increasing plasma power rather than the temperature. However, it can lead to degradation of wafer properties so it will be controlled by DLTS measurements for each sample to define optimal growth parameters for future application in photovoltaics.

3. Conclusion

The quality of silicon wafers was explored after PE-ALD growth of GaP at temperatures below 400 °C by space charge capacitance methods (C–V and DLTS). The absence of response on DLTS spectra for n-type wafer means that the defect concentration is very low (less than $1 \times 10^{12}\,cm^{-3}$). N_{CV}–W profiles do not indicate passivation of boron-doping in p-Si after PE-ALD. In the reference p-type Si samples defects were detected at a concentration of $3 \times 10^{13}\,cm^{-3}$ and an energy position of $E_V + 0.38$ eV, suggesting the presence of interstitial iron in the wafers. PE-ALD of GaP leads to some modification of this defect and to the appearance of another response in the low temperature range. However, levels with larger activation energies were not detected in p-Si after PE-ALD, suggesting that the quality of p-Si does not deteriorate. This should be confirmed by measurements on better quality wafers.

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Conflict of Interest

The authors declare no conflict of interest.

Keywords

deep-level transient spectroscopy, defects, GaP, heterojunctions, plasma-enhanced atomic layer epitaxy, silicon

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