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Abstract: In power electronics, in order to minimize the dimension and increase the performance of the converters, passive component integration is needed. One strategy is to replace the surface-mounted, discrete capacitors with embedded capacitive layers to achieve a variety of functions such as: resonant, filter, decoupling and bypassing capacitors. The main strategy used by designers is to use larger value capacitors for more efficient decoupling or filtering purposes. In order to increase the capacitance of an embedded capacitor, higher dielectric constant material can be used, also electrodes can have a larger surface and new technologies can be applied to reduce the thickness of the dielectric. This paper focuses on studying high capacitance embedded capacitors for power electronics applications, fabricated by screen-printing technique. Thick film ferroelectric ceramic was printed on Ag/Al_2O_3 substrates and dried at 120^0C, then a pre-treatment was applied by cold isostatic pressing (CIP) to improve the quality of the thick films. A comparison between the non-CIP and CIP samples are made from a physico-chemical and dielectric characteristics point of view. The results show that the microstructure of thick films were treated by CIP and have better dielectric properties. The embedded capacitor samples with CIP exhibit higher capacitance, lower parasitic ESL and smaller ESR. The overall process for obtaining the embedded capacitors, allows for high capacitance values for decoupling and filtering applications in power electronics.

I. INTRODUCTION

Advanced power electronic circuits have been continuously innovated and integrated according to three main driving parameters: increase in electrical performance, decrease in dimension and cost reduction. Among the various technologies, the embedded passive components technologies have been increasingly studied (Ostmann et al., 2002) because of their high integration ability for both active and passive components to build 3D standardized compacts (Lee et al., 2002).

This technology replaces discrete passive components into a multilayered substrate. This substrate not only reduces the component volume, but it also reduces total board and increases electrical performance and reliability due to a miniaturization in interconnection length and a decrease on the number of solder joints and vias. Of the embedded passive components, planar embedded capacitors account for the greatest interest because they often occupy large volumes and quantity with many difference functions. The most important factors that limit the application of capacitors are capacitance value, wide range of operated frequency, voltage rating, low parasitic and effective production cost. Integrated capacitors devoted for decoupling or filtering functions often require large capacitance values. To achieve a compromise between these factors, embedded capacitors based on ferroelectric materials are a reasonable option because they present high capacitance density, low parasitic ESL, low ESR high permittivity and the physic-chemical stability of the ceramic materials (Guillemet et al., 2001). In addition, when applying a screen-printing technique, they have a great potential in reduction of cost thanks to a simple, high throughput and reproducible process. One simple way to obtain high capacitance could be to reduce the thickness of the dielectric layer thanks to the use of cold isostatic pressing (CIP) (Hindrichsen et al., 2010). CIP allows producing compacts with effective uniform grain structure and density (Peng et al., 2011)due to applying the high pressure in multiple directions (James, 1971). In this paper, several processes are presented to fabricate a planar ferroelectric capacitor on an alumina substrate, High isostatic pressure is applied to study its impact on the properties of screen-printed ferroelectric thick film. Different CIP processes have been investigated and discussed in both physico-chemical analysis and electrical properties.

II. SAMPLE PREPARATION

A simple MIM (metal – insulator – metal) capacitors were realized by screen-printed technology according to four different processes summarized in Table 1.The chosen insulator paste is based on a lead titanate . The dielectric commercial material (ElectroScience ESL 4212) presents a dielectric permittivity ranging from 2000 to 12000 according to the manufacturer information. The metal selected for completing the MIM structure needs to be compatible with the sinterint temperature of the dielectric, in this case a silver-based paste was the appropriate one.. The layers are deposited on top of a 50.8 x 50.8 mm, 635µm thick alumina substrate. MIM capacitors are fabricated based on a first optimized process named *P1* described in the following. In a first step, the alumina substrate is cleaned using a basic solution of RBS 25MD (Sigma-Aldrich) at a concentration of 2%vol in an ultrasonic bath for 30 minutes, rinsed with deionized water and then dried at 120°C during 10 minutes. In the next step, the first (silver-based) electrode is printed on the surface of the alumina substrate, dried at 120°C during 10 minutes and then sintered at 900°C during 10 minutes. A first

dielectric layer (DL) is deposited on the first electrode, and then dried and sintered at the same temperature and dwell time that mentioned before. Instead of a silver electrode deposition, a second dielectric layer is screen printed to decrease the probability of direct failure or shortcut due to holes and other defects of the first DL. Finally, after this second DL has been dried, the second silver layer is printed, dried and co-sintered with the second DL. Using this simple method, screen-printing technology can successfully fabricate thin integrated capacitors with thickness only a few tens of micrometers.

In order to reduce the thickness of dielectric layer, the samples in processes P2, P3, P4 were fabricated according to the main process as in P1 but the dielectric layers were pressed isostatically at different pressures, with a holding time of 5 minutes. For example, process P2, CIP was applied for only one the first dielectric layer (DL), process P3 CIP applied for first DL then applied for both 2^{nd} DL and 2^{nd} Ag whereas process P4 applied CIP for 1^{st} DL and 2^{nd} DL separately.

III. RESULTS AND DISCUSSIONS

A, Physico-chemical analysis:

Microstructure of Grains

Samples without applied CIP and with applied CIP (only at 300 MPa) were cut into individual elements using a diamond saw. Then, they were encapsulated in epoxy resin and polished to a mirror finish to observe the sintered layers morphology and microstructure, and to perform a chemical analysis by energy dispersive spectroscopy (EDS, Oxford INCAEnergy) coupled to the SEM. The cross-section morphology in Fig.1 demonstrates a clear impact of the applied CIP pressure in the pore size and its distribution across de dielectric layer.

SEM images in Fig. 2 show that although the two dielectric layers are fabricated in different ways, the final grain morphology of samples with CIP and without CIP are close in grain size distribution.

Chemical analysis by EDS of two samples with and without CIP application in Figure 4 and Figure 5 accounts for a lead diffusion from the dielectric layer into the alumina substrate, though the silver electrode. The small diffusion of lead into the alumina could have an impact on the dielectric breakdown due to local field reinforcement. This has to be confirmed later studies

B, Electrical characteristics

Capacitance and permittivity values

In order to compare the permittivity of the samples which have applied CIP to others which have not the CIP, thickness measured of dielectric layer by the observation of a section by scanning electron microscopy (SEM) in backscattered electrons mode (JEOL JSM-6700F) and the capacitance of different capacitors was measured by gain-phase analyzer in the 100 to 10^7 Hz range (Hewlett Packard 4194A). The results in Table 2 present that the thickness of dielectric layer is reduced remarkably when CIP is applied. The comparison of relative permittivity between sample with CIP and without CIP can be calculated thanks to formula:

$$n = \frac{\varepsilon_{CIP}}{\varepsilon_{no\_CIP}} = \frac{C_{CIP} d_{CIP}}{C_{no\_CIP} d_{no\_CIP}}$$

Where n is the change of permittivity of the samples with CIP compared to the sample without CIP process P1, C is capacitance, ε is dielectric material's permittivity.

It is obvious seen that most cases the capacitance of the samples with CIP increases (n>1) for the two following reasons:

i. The thickness of the dielectric layer reduces thanks to CIP pretreatment. (In Table 2 the thickness of each sample was calculated average from three measured points).

ii. The permittivity of dielectric material increases due to improvement of thick film's dielectric properties when they were compacted. The **Erreur ! Source du renvoi introuvable.** shows that the permittivity of the dielectric material after CIP treatment can obtain much higher value (nearly 18000) compared to the one without CIP (around 10000).

Due to pretreatment of isostatic pressing the dielectric properties of the thick films improve, because the pores with low relative permittivity are progressively eliminated (Liu and Wang, 2012). The increase of permittivity could be also caused by a combined contribution of a decrease of domain size and stress effects related to the increase in density (Arlt et al., 1985).

Impedance and capacitance versus frequency

The Fig. 6 presents the relative change of capacitance and impedance with frequency and pressure level applied to the samples for process P4 compared to sample without the CIP. Capacitance values increase - proportionally with the applied pressure to the screen printed

dielectric layer. The samples are capacitive in the frequency range from 100Hz to 900kHz. Around 1MHz the parasitic equivalent series resistor ESR can be observed, whereas the inductive behavior dominates at higher frequencies.

Figure 7 presents the results of capacitance values for all the processes for the maximum applied pressure of 300 MPa, the results are compared with the process with no CIP. It is important to note that the process P3 and P4 can obtain higher capacitance than process P2 because CIP was applied to both dielectric layers, while in process P2 only the first dielectric layer was treated with CIP. This once again confirms the impact of CIP pretreatment in the shrinkage and properties modification of the ferroelectric thick film.

Temperature dependence of the electrical properties:

The temperature dependence of the dielectric properties is one of factors limiting the application of ferroelectric capacitors. The dielectric properties of MIM capacitors were therefore measured as a function of temperature. The dielectric used for the fabrication of the MIM structures, exhibits the maximum capacitance value at 25°C. The capacitance changes with the temperature limits the material performance, and probably is not a good candidate for severe environment applications. The Figure 8 presents that the Curie temperature is not modified by process P3; regardless of the applied pressure. In Figure 9, the phase transition temperature of the dielectric of samples with and without CIP exhibit a similar value for the applied pressure of 200 MPa. The Curie temperature is around room temperature for all cases. The dielectric losses ($\tan\delta$) of the ferroelectric phase are very low as function of both the frequency and the temperature range, remaining in all cases below 0.1.

Withstand voltage test:

All capacitors are designed for a particular rated voltage. In power electronics applications, this is going to be one of the mayor limiting factors to be taken in account for circuit design considerations. Therefore we measured the maximum voltage that could be applied to the MIM structures. To achieve this we applied dc voltage until breakdown of the ceramic occurs. When breakdown occurs a surge in current is detected and two possible things could occur. One is the self-healing of the dielectric, when the breakdown creates a full delamination of the metallic electrode, creating a small surface where the voltage is no longer applied. If this event occurs in a first place (one, or several times), then it is possible to continue to apply a higher voltage until a full short circuit is created by one last breakdown event. Table 4 shows the voltage (V) that can be applied to the samples before a first breakdown event between the electrodes. The measured voltage

was limited to 300 V, since targeted applications (Doan et al., 2013) do not require larger field application.

In summary, the different properties of the material under study and of the manufacturing processes used to realize the capacitors are in good agreement with PE demands and these properties may be taken into account when designing a capacitor for PE applications.

IV. CONCLUSIONS

The ferroelectric capacitors were successfully fabricated with four various processes. Cold isostatic pressing was investigated to improve dielectric properties of screen-printed thick films. A higher capacitance densification was reached due to different CIP application modes The high capacitance values and their low losses could allow the development of an integrated capacitor as a mayor component of filtering applications in power electronics. CIP could be a useful technology for forming thinner and higher capacitive integrated capacitors thus providing more flexibility to power electronics designers.. In future works, we propose further investigations for building multilayer capacitor construction to reach much higher capacitance. These capacitors can integrate into planar capacitive substrate with semiconductor dies placed on their surface. With great potential in size and cost reduction they are good selection to replace traditional bulky printed circuit board (PCB).

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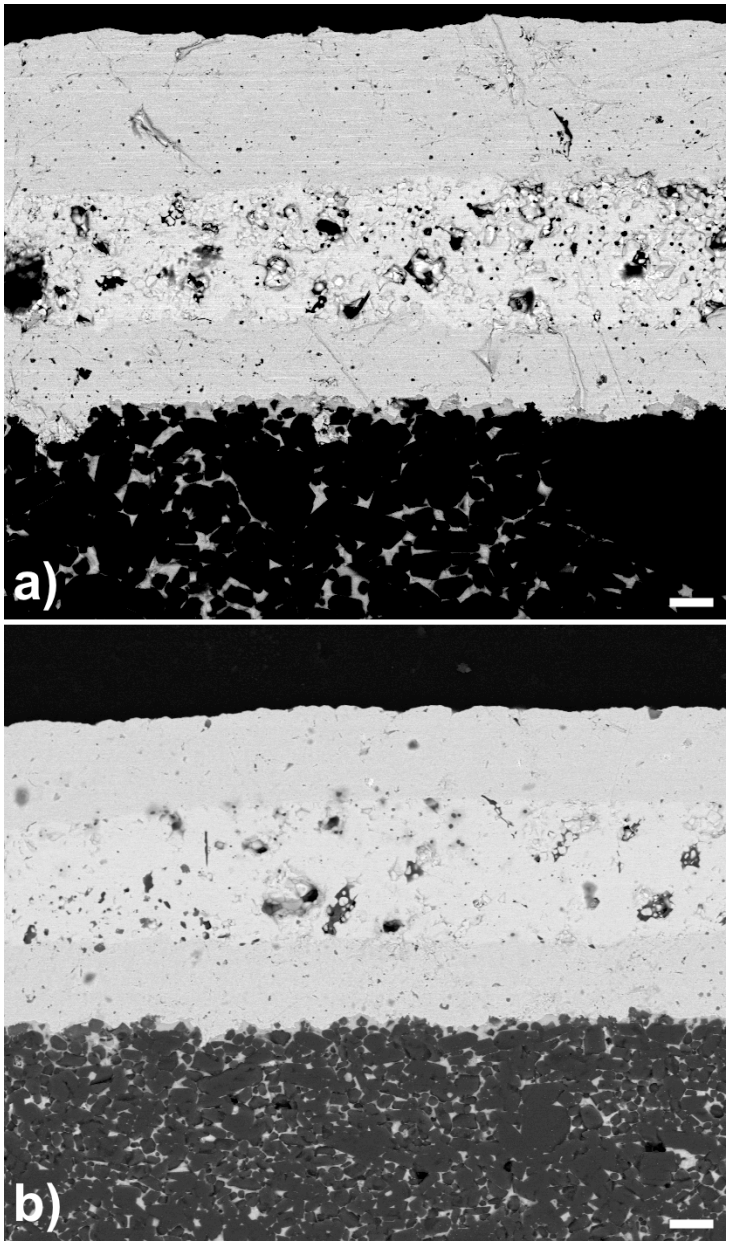

Figure 1. Cross-section of the Metal-Insulator-Metal sample a) without CIP S2P1 and b) sample with CIP S4P3 (pressed at 300 MPa). The maximum pore size is reduced by the application of the CIP. Bar=10µm.

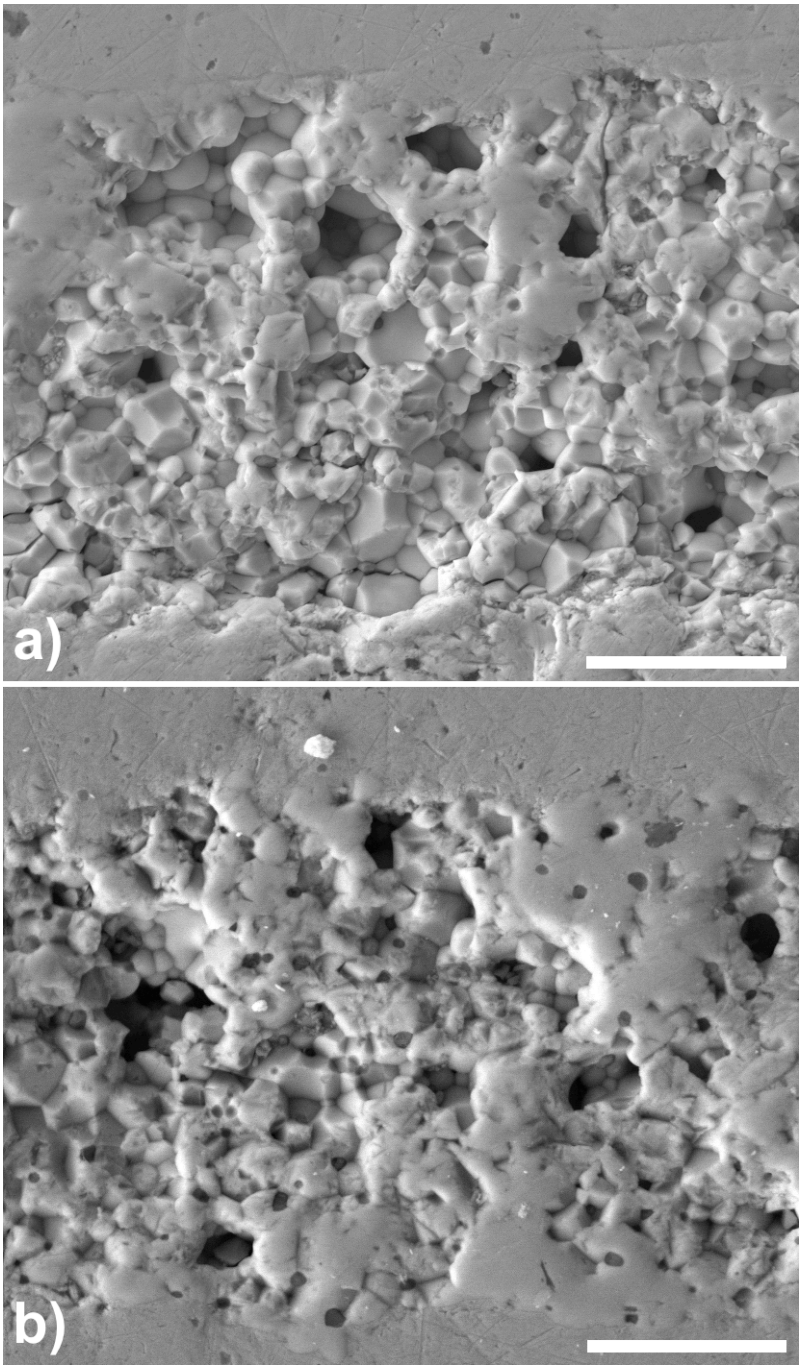

Figure 2. The SEM scan photos of samples without CIP and with CIP .Bar=10 μm.

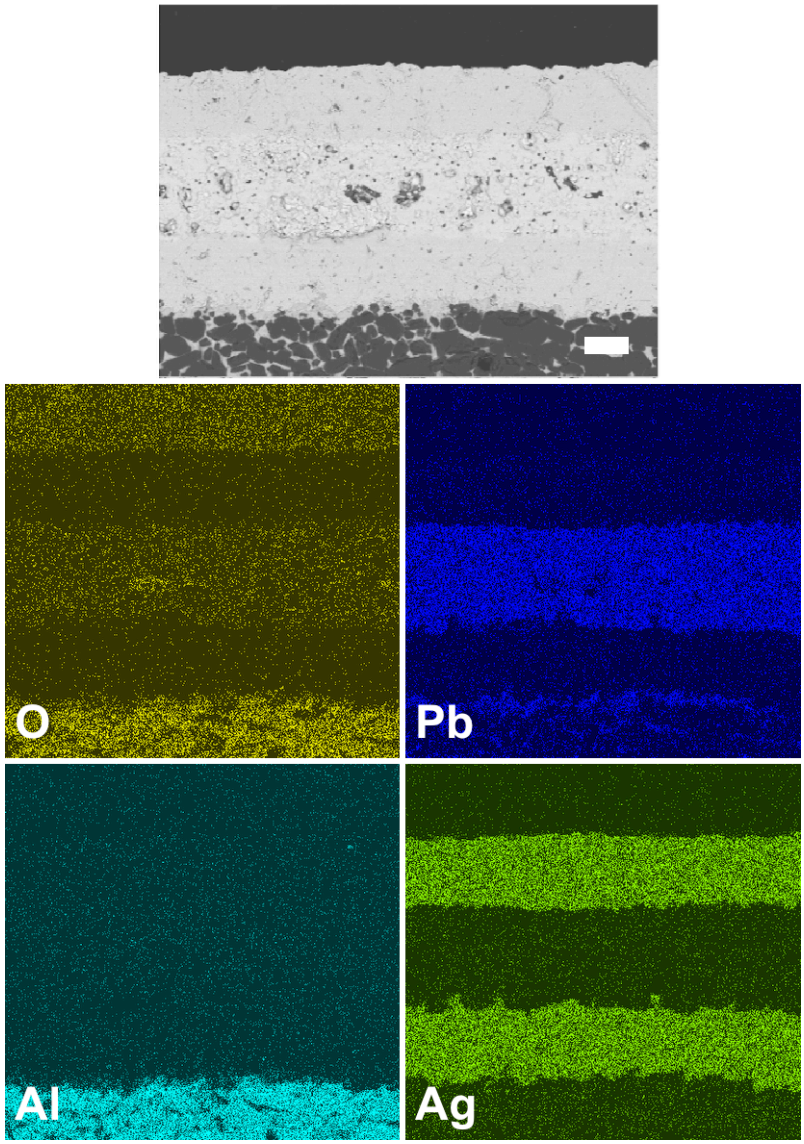

Figure 3. Chemical analysis of sample without CIP. Bar=10 µm.

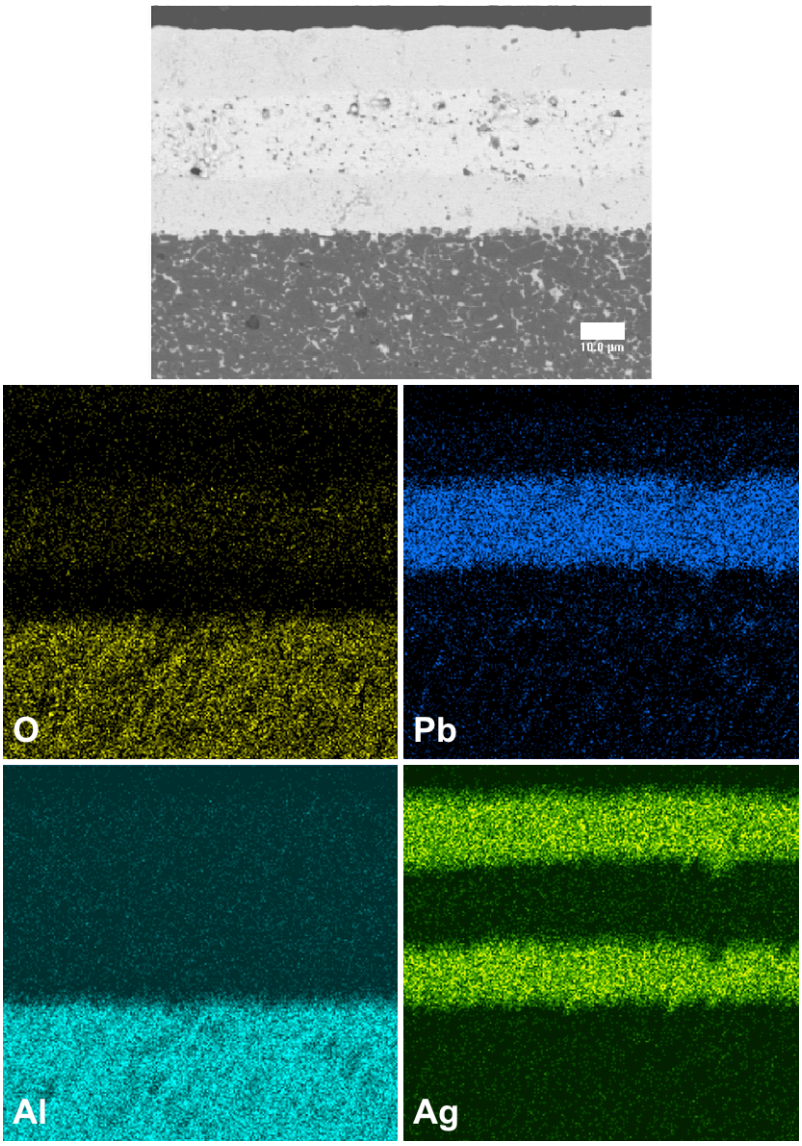

Figure 4. Chemical analysis of sample with CIP. Bar=10 µm.

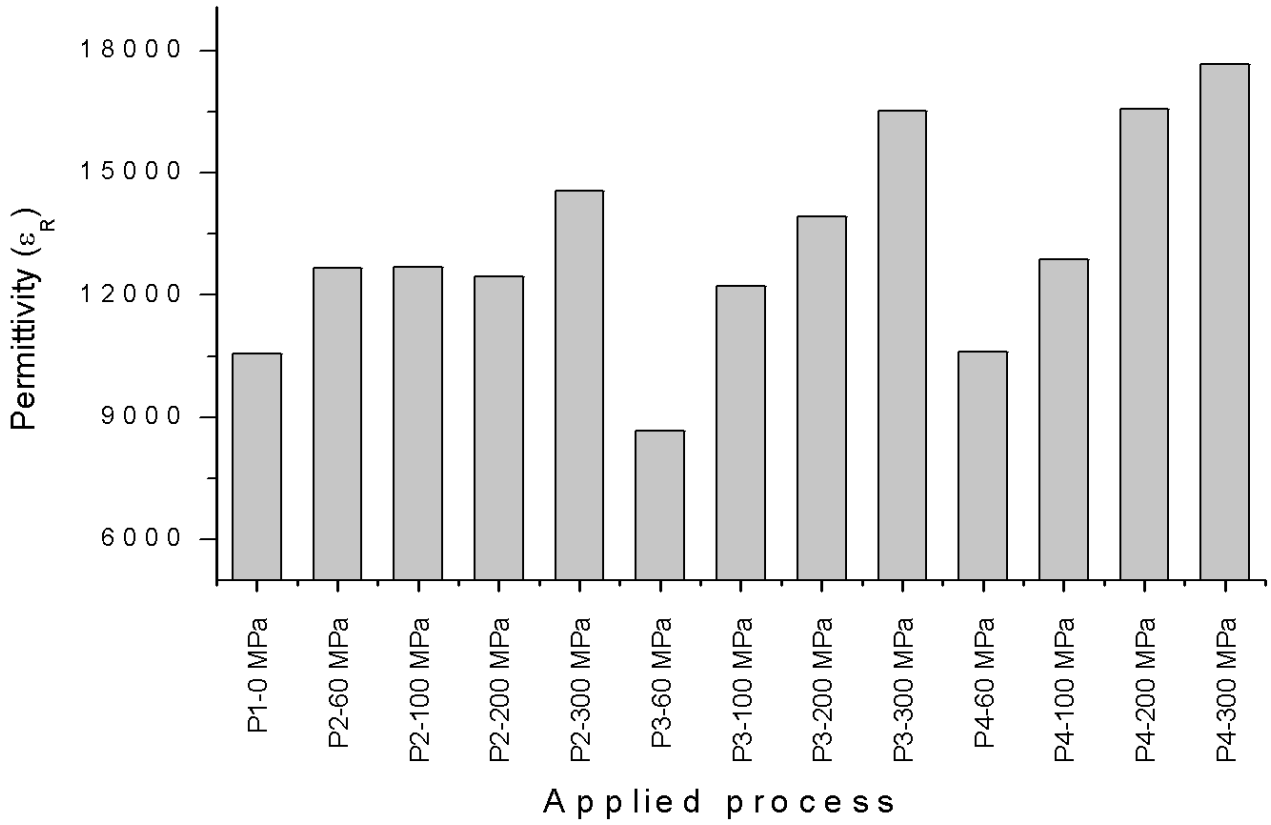

Figure 5. The change of permittivity versus frequency and pressure level

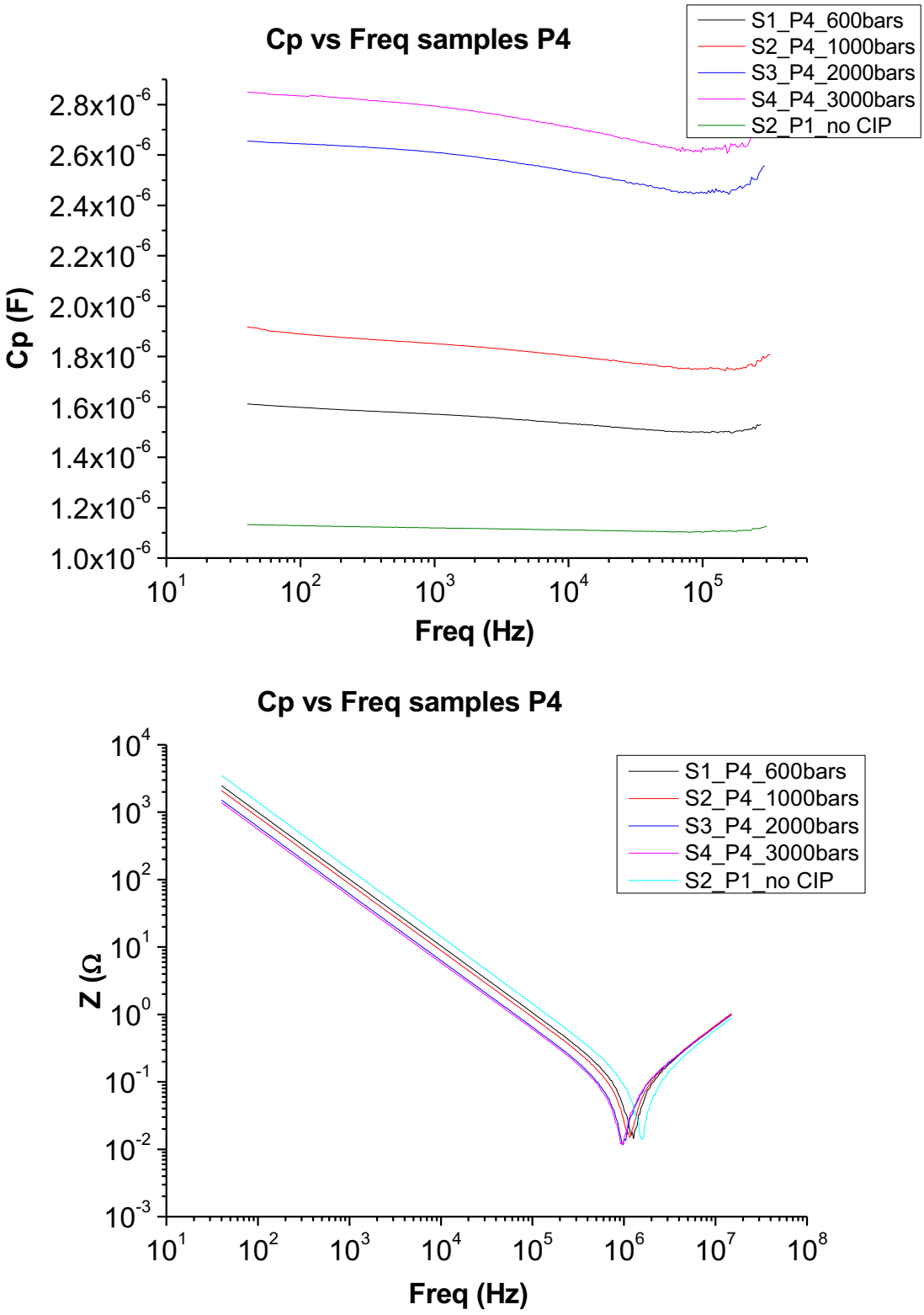

Figure 6: Capacitance and impedance behavior of sample without CIP (S2P1) and samples with CIP for the different pressure levels applied for process P4 samples.

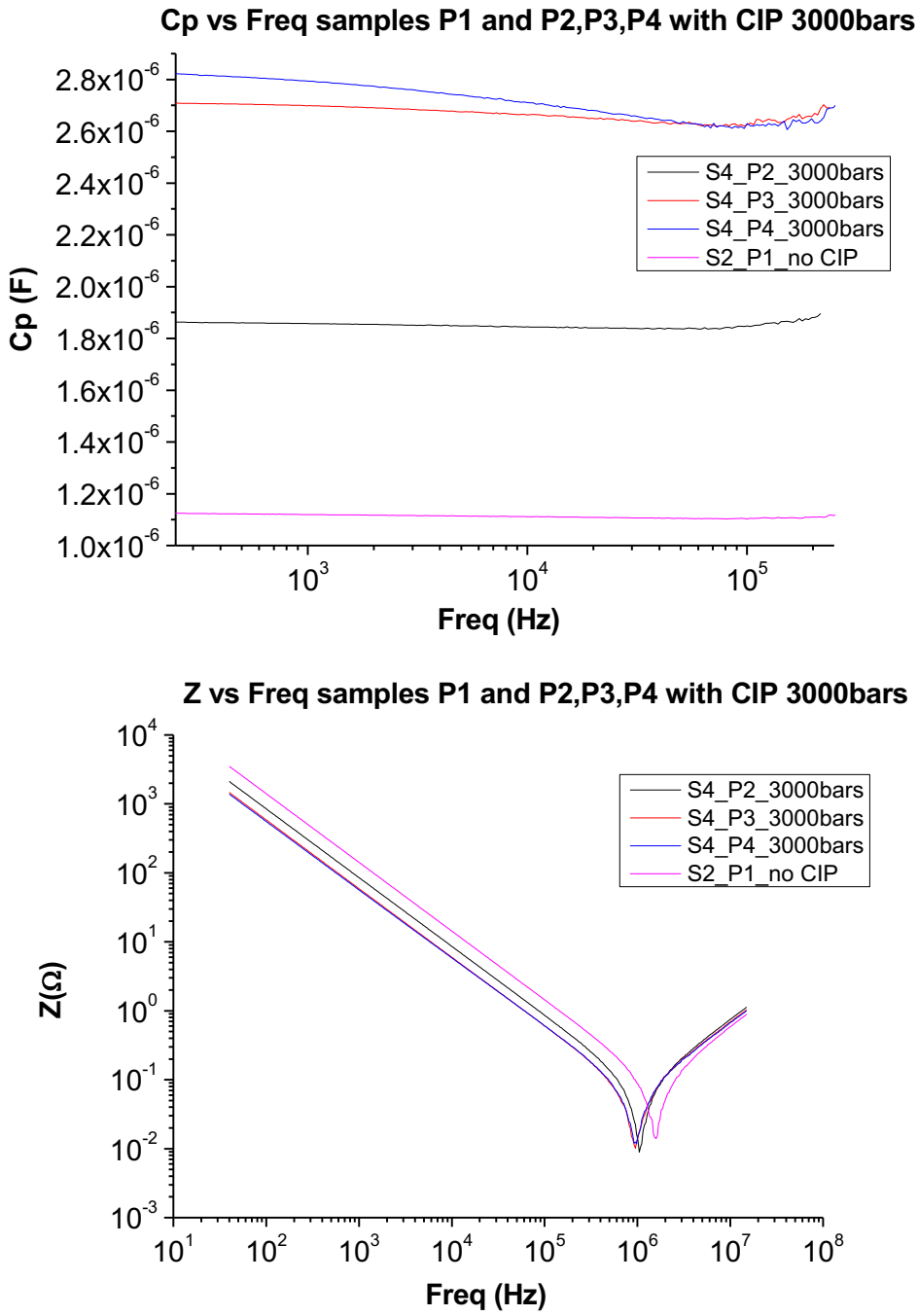

Figure 7. Capacitance and impedance behavior of sample without CIP S2P1 and samples with same CIP level (300 MPa) for all processes.

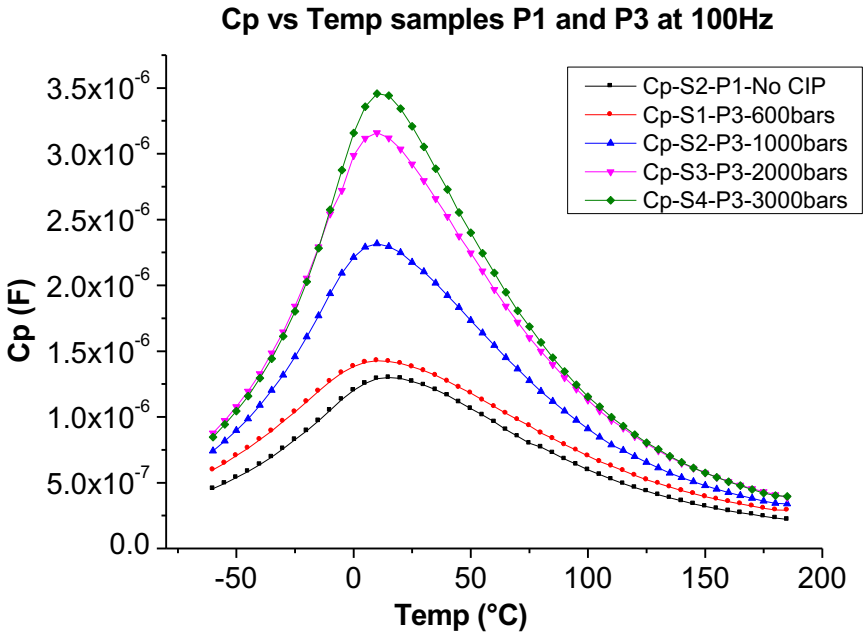

Figure 8. Capacitance dependence with temperature for samples with and without CIP application at different pressure levels (only process P3 is shown)s.

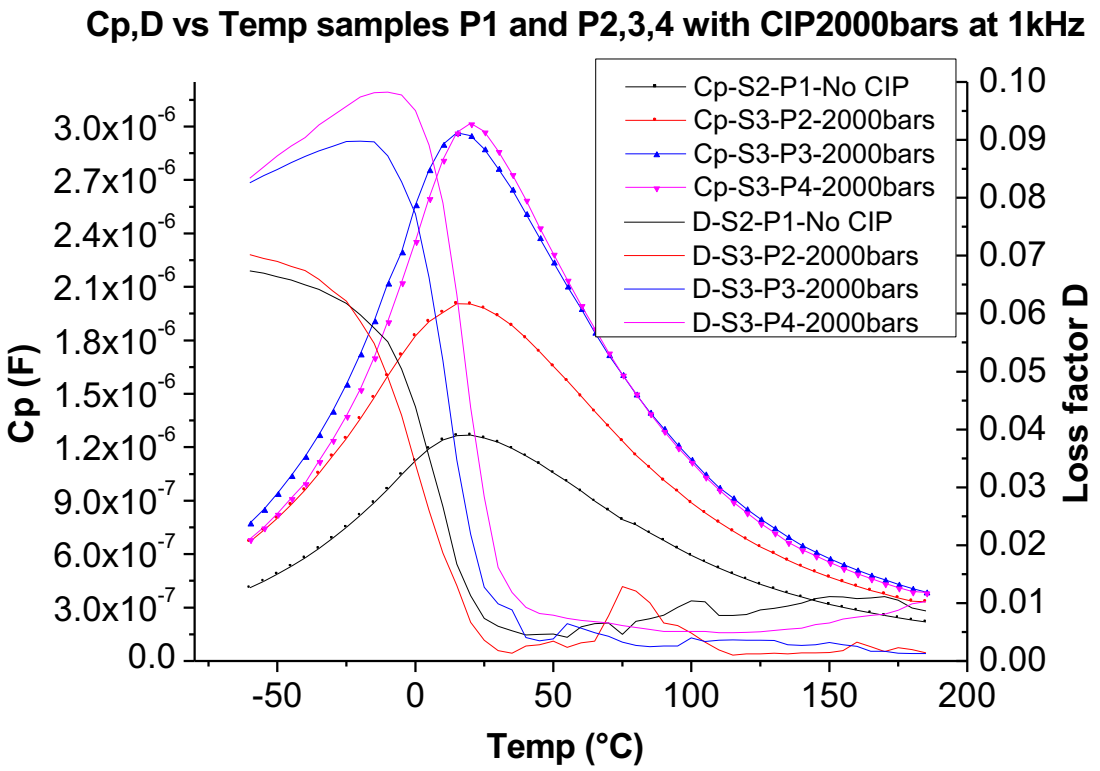

Figure 9. Dielectric loss factor (tanδ) as a function of temperature of samples with and without CIP for the same pressure level (200 MPa) for the different processes.

Table 1. Sample preparation steps for fabricating MIM capacitors.
(Abbreviations: DL: Dielectric; De/D/S stand for: Deposit/Drying/Sintering; CS: co-sintering, C-CIP: co- cold isostatic pressing)

Process	Layer	Flow	Dwell time (day)	Notes
P1	1st Ag	De/D/S	1	No CIP applied
	1st DL	De/D/S	1	
	2nd DL	De/D	1	
	2nd Ag	De/D/CS		
P2	1st Ag	De/D/S	1	CIP applied only on the 1st DL
	1st DL	De/D/CIP/S	1	
	2nd DL	De/D	1	
	2nd Ag	De/D/S		
P3	1st Ag	De/D/S	1	CIP applied on the 1st DL and then CIP applied for both 2nd DL and 2nd Ag
	1st DL	De/D/CIP/S	1	
	2nd DL	De/D	1	
	2nd Ag	De/D/C-CIP/CS		
P4	1st Ag	De/D/S	1	CIP applied for the 1st DL and 2nd DL separately.
	1st DL	De/D/ CIP/S	1	
	2nd DL	De/D/CIP/S	1	
	2nd Ag	De/D/S	1	

Table 2. Thickness of samples measured by SEM

Name	Pressure (MPa)	Point 1 (μm)	Point 2 (μm)	Point 3 (μm)	Average thickness d (μm)
S4 P2	300	26	28	27	27
S4 P3	300	23	20	21	21
S4 P4	300	23	22	21	22

Table 3. The comparison of dielectric layer's thickness and relative permittivity change of sample (n) with and without CIP application.

Name	Pressure (MPa)	Point 1 (μm)	Point 2 (μm)	Point 3 (μm)	Average thickness d (μm)	Cp at 1kHz, room temp.	n
S2 P1	0	57	52	58	56	1.12	1
S1 P2	60	49	52	52	51	1.18	1.2
S2 P2	100	27	35	31	31	1.94	1.2
S3 P2	200	30	35	33	33	1.79	1.18
S4 P2	300	35	40	36	37	1.86	1.38
S1 P3	60	26	36	33	32	1.28	0.82
S2 P3	100	30	30	29	30	1.93	1.16
S3 P3	200	22	28	28	26	2.53	1.32
S4 P3	300	26	32	29	29	2.70	1.57
S1 P4	60	33	32	30	32	1.57	1.005
S2 P4	100	36	32	32	33	1.85	1.22
S3 P4	200	25	33	31	30	2.61	1.57
S4 P4	300	30	31	30	30	2.79	1.67

Table 4. DC voltage that can be applied to the MIM capacitors.

Name	Pressure (MPa)	Average thickness d (μm)	Cp at 1kHz, room temp	V_{br}
S2 P1	0	56	1.12	300*
S1 P2	600	51	1.18	195
S2 P2	1000	31	1.94	300*
S3 P2	2000	33	1.79	150
S4 P2	3000	37	1.86	300*
S1 P3	600	32	1.28	230
S2 P3	1000	30	1.93	300*
S3 P3	2000	26	2.53	200
S4 P3	3000	29	2.70	70
S1 P4	600	32	1.57	120
S2 P4	1000	33	1.85	140
S3 P4	2000	30	2.61	150
S4 P4	3000	30	2.79	300*

* Up to this voltage level there is no breakdown.