# Design and Characterization of an Eight-Phase-137-kW Intercell Transformer Dedicated to Multicell DC–DC Stages in a Modular UPS

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# Design and Characterization of an Eight Phase-137kW Intercell Transformer Dedicated to Multi-cell DC-DC Stages in a Modular UPS

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Recent Uninterruptible Power Supply systems, in the medium power range (a few 100 kW), are based on a three-power stage topology including a rectifier, an inverter, and a DC-DC converter. The DC-DC converter ensures the charger / discharger function necessary for battery management. The Monolithic InterCell Transformer (ICT) described in this paper is dedicated to such a charger/discharger, of which the nominal power is 137kW. This DC-DC converter is comprised of eight interleaved cells that are interconnected by the ICT.

The first part of the paper briefly presents the full UPS system and the topology of the eight-cell charger/discharger arranged around the eight-phase monolithic ICT.

The second part suggests a model and emphasizes the design specificities of the monolithic ICT. The final design is provided by an optimization routine, checked in the end by different 2D and 3D Finite Element (FE) simulations, both electromagnetic and thermal.

The third part describes the construction of the ICT prototype. It is then placed in a test-bench that reproduces the conditions of future operations and provides current balance conditions. Lastly, the experimental results obtained for the 137kW nominal power validate design parameters and confirm the interest of the ICT solution.

Keywords—Interleaved converters, ICT, UPS

## I. Introduction

The hardware used in critical infrastructures, such as digital networks and data centers, must include Uninterruptible Power Supplies (UPS) [1] to ensure availability in case of failure in the AC supply network. The electrical power of these UPS units is increasing continuously and can now reach up to one Megawatt. In this context, manufacturers are developing modular UPS systems that are able to cover a broad power range by associating a variable number of modules.

The magnetic device described in the present paper is dedicated to a DC-DC converter that constitutes a part of a future “on-line” and modular UPS system, currently under development. This DC-DC converter provides the charger/discharger function of the UPS. It controls the battery charge under normal operation and supplies the DC bus from batteries in case of AC grid failure. In the case considered here, the maximal power of that charger/discharger is 137kW. It is the basic DC-DC module for the future range and several units can be parallelized to build a more powerful stage.

As the on-line UPS system is always in operation, the efficiency of the AC/DC/AC part is a very important feature: the higher its value, the lower is the operating cost. In the same manner, increasing the efficiency of the charger/discharger increases battery autonomy in backup mode.

To improve efficiency, the converter topology and the power semi-conductor devices must be carefully evaluated, compared, and selected [2]-[9]. We do not address this part of the design in the present paper, but the conclusion was reached that series-parallel multi-cell converter topologies using interleaving, such as that presented Figure 2, were an interesting option for obtaining very low semiconductor losses. This paper is focused on the design, construction, and testing of the eight-phase InterCell Transformer (ICT, [10][13]) that has been chosen to interconnect the different cells, in an effort to increase the efficiency and decrease the weight of the battery-side filter (it must be possible for a maintenance operator to be able to handle the DC-DC rack). The main originality lies in the high number of cells and the monolithic shape of the ICT, two points that make it possible to obtain good characteristics for the magnetic part of the filter.

The first part of the paper briefly presents the general arrangement of the full UPS system and the topology of the charger/discharger, including the eight-phase monolithic ICT.

The second part describes the design process that was developed explicitly for this very specialized magnetic device. The final design is provided by an optimization routine that is checked in the end by different 2D and 3D Finite Element (FE) simulations to evaluate both electromagnetic and thermal parameters.

In the third part, we present the construction of the ICT prototype, essentially composed of eight specific U cores. Then the ICT prototype is placed in a test converter that reproduces the conditions of future operations. The monolithic ICT requires a very good current balance between the different phases and therefore, the control part includes an original circuit using differential current sensors. Lastly, we present the results of experiments using 137kW nominal power. These results validate the design parameters and confirm the interest of the ICT solution.

## II. General Structure of the UPS System

### A. Global design

The general arrangement of the full UPS system is given in Figure 1. It is obtained by adding the three stages: the rectifier that generates the DC bus from the AC network (normal operation); the inverter that generates output voltages (normal operations and backup mode); and the charger/discharger (normal operations and backup mode).

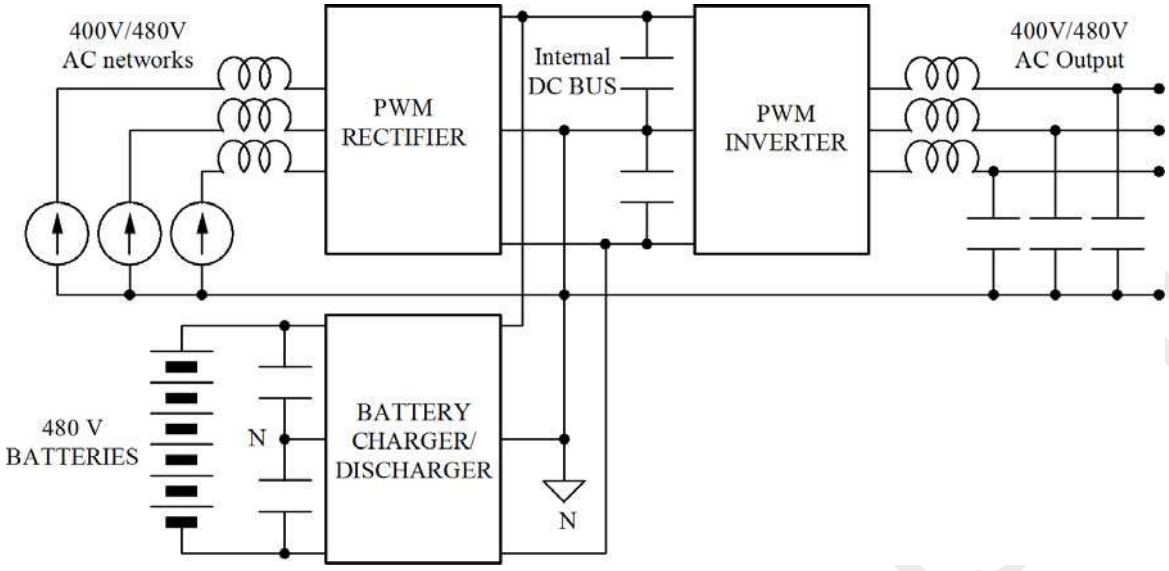



Figure 1: UPS arrangement

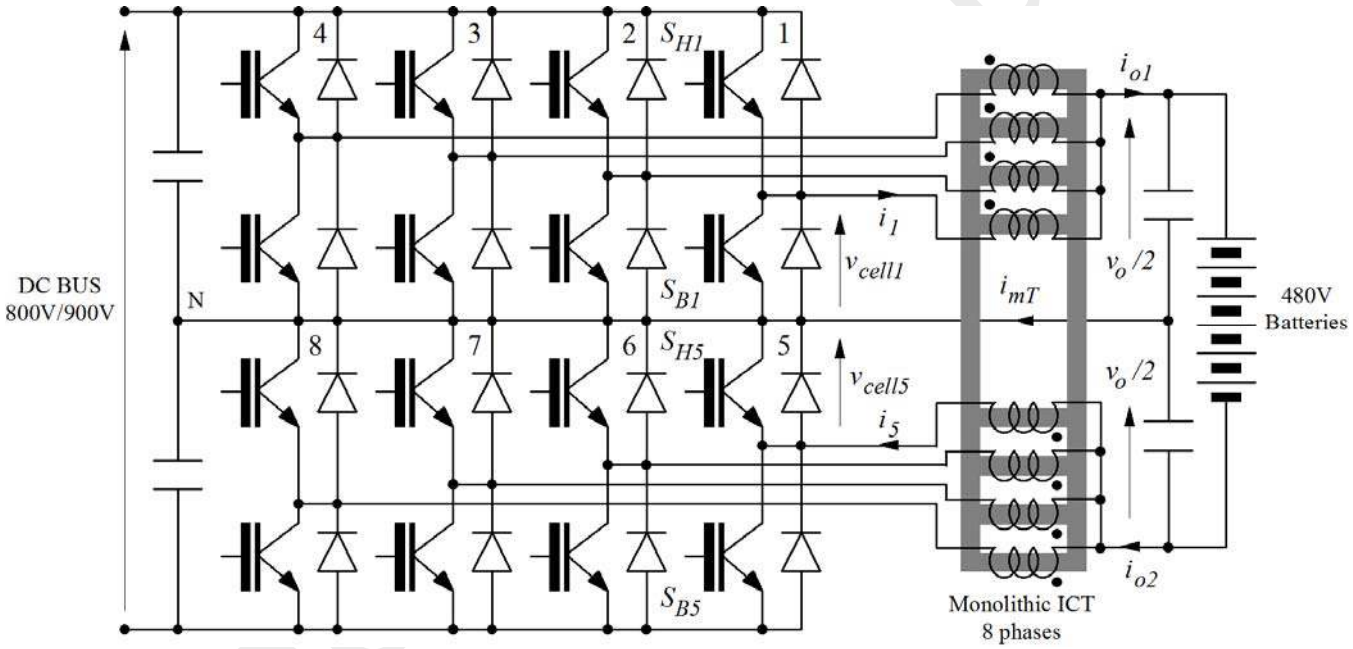



Figure 2: Multi-cell ICT DC-DC converter

This scheme shows a particular specificity of UPS system, that is, organization around a neutral point that makes the three output phases independent, while facilitating operations with unbalanced loads.

In addition, the UPS system must be able to operate both on 400V and 480V AC networks. Therefore, the DC-DC bus voltage is regulated between 800V (400V AC) and 900V (480V AC).

### *B. Multi-cell ICT DC-DC converter*

The DC-DC converter is the charger/discharger component in the system. In discharge mode, it must provide nominal power of 137kW to the inverter stage from the batteries (nominal voltage 480V). In that mode, battery voltage can vary between 550V under full charge and 380V closer to the discharged state. In the most critical case, i.e. 380V, the total current on the battery side can reach 360A. It is the main location of current stress in the system. Therefore, in order to use the same power semiconductor devices in the different stages (for modularity), a series-parallel DC-DC converter is chosen (Figure 2). The rectifier and inverter stages are similarly arranged with, in each phase, two 600V cells connected in series on the capacitive divider. To provide the same power, the DC-DC converter theoretically needs at last three similar stages (6 cells), but in practice four stages (8 cells) are used because of the lower battery voltage and the resulting high current. This even number makes it possible to design an efficient and symmetrical monolithic ICT.

Therefore, to allow interleaving of the eight cells and to minimize the size filter, an eight-phase ICT is used, which is the topic of the present paper. The converter control sequence is defined to generate an eight-phase voltage system (frequency $F_{sw}$) composed of the four voltages of both groups (referenced with respect to the neutral point).

## III. Operation and Design of the Monolithic ICT

The monolithic ICT is the main originality of the proposed DC-DC converter. Using an ICT makes it possible to minimize the magnetic part of the battery filter, as compared to a separate inductor solution. The counterpart is the specific core required by this solution. Section IV.A shows how the problem was solved with low cost ferrite cores.

### *A. Simplified modeling and operation*

The ICT principle has been widely described in [10][13]. ICTs can be monolithic or they can be built with separate transformers. The optimal operating mode is obtained by means of particular sequences of the multi-phase supply voltage system [10][11][12]. In case of high number of cells, they can replace the separate inductors without an additional output inductor. Therefore, it is a gapless device that allows the introduction of high induction materials such as nanocrystalline.

A monolithic ICT is a k-phase magnetic device that uses a monolithic magnetic core with k winding legs (or columns) linked by 2k linking legs. The ICT must be quasi-symmetrical in order to obtain a proper electrical balancing. Assembly of the magnetic core must also be as simple as possible. The shape shown on Figure 3-a corresponds to these requirements. It imposes an even phase-number but can be achieved by associating k U cores (*see section IV.A.*). This shape was therefore chosen for the present work.

To describe ICT operation in the particular converter shown in Figure 2, and to obtain the basis for design, a simplified reluctance modeling is proposed (Figure 3-b), from which an electrical model is derived. Each column has a reluctance $R$. A column is connected with adjacent columns through linking legs that have a reluctance $2R_T$. If the leakage flux due to one cell is considered, one part noted $\Phi_{akout}$ flows through the air outside of the ICT; another part noted $\Phi_{akin}$ flows inside the window between two columns. Reluctances $R_{akout}$ and $R_{akin}$ are attributed respectively to both leakage zones. By considering the symmetry assumption, all ICT-phases have the same leakage flux $\Phi_{akin} + \Phi_{akout}$ that constitute one $k^{th}$ of the total ICT leakage flux. The complete description of the ICT is obtained by connecting k identical cells in a ring. This is used in section III.B.2) to estimate flux repartition and core losses.

To describe the principle of ICT operation, it is simpler to ignore the reluctances $R_T$ with respect to the reluctances $R_{akin}$ and also to ignore the winding resistances. With these assumptions, the reluctance network becomes that of Figure 4-a, with:

– $\Phi_p$ , flux in column p
– $\Phi_{ak} = \Phi_{akin} + \Phi_{akout}$, leakage flux between two phases
– $R$, column reluctance
– $R_{ak} = R_{akin} + R_{akout}$,
– $n$, turn number by phase,
– $L = n^2/R$ and $L_{ak} = n^2/(R_{ak} + R)$

Figure 4-b shows the arrangement and the notations that are used subsequently in this paper. It is assumed that both output voltages are balanced and equal to $v_o/2$.

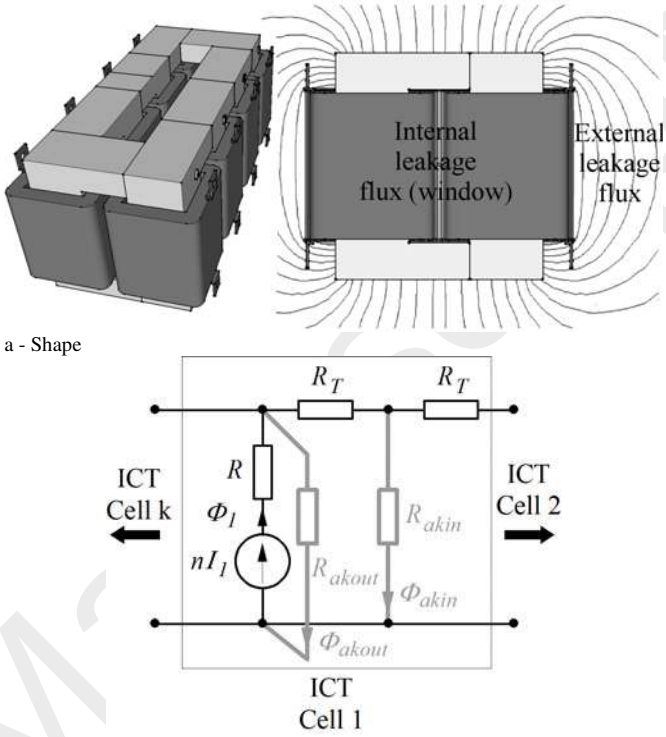



Figure 3: Shape and cell-model of the monolithic ICT

#### *1) Equations*

The flux in a column is given by:

$$v_p = v_{cellp} - \frac{v_o}{2} = n\frac{d\Phi_p}{dt} \quad (1)$$

By summing on the k phases: $\frac{v_o}{2} = \frac{\sum_{p=1}^{k} v_{cellp}}{k} - n\frac{d\,\Phi_{ak}}{dt}$ (2)

Hopkinson law for one phase: $n\,i_p - R\Phi_p = R_{ak}\,\Phi_{ak}$ (3)

By summing on the k phases: $n\,(i_{o1} + i_{o2}) = k\,(R_{ak} + R)\Phi_{ak}$ (4)

From (2) and (4) it follows: $\frac{v_o}{2} = \frac{\sum_{p=1}^{k} v_{cellp}}{k} - \frac{L_{ak}}{k}\frac{d\,(i_{o1} + i_{o2})}{dt}$ (5)

The first term of (5) corresponds to the generation of the interleaved voltage, its frequency is $k.F_{sw}$. Therefore, the frequency of the term $i_{o1} + i_{o2}$ is also $k.F_{sw}$.

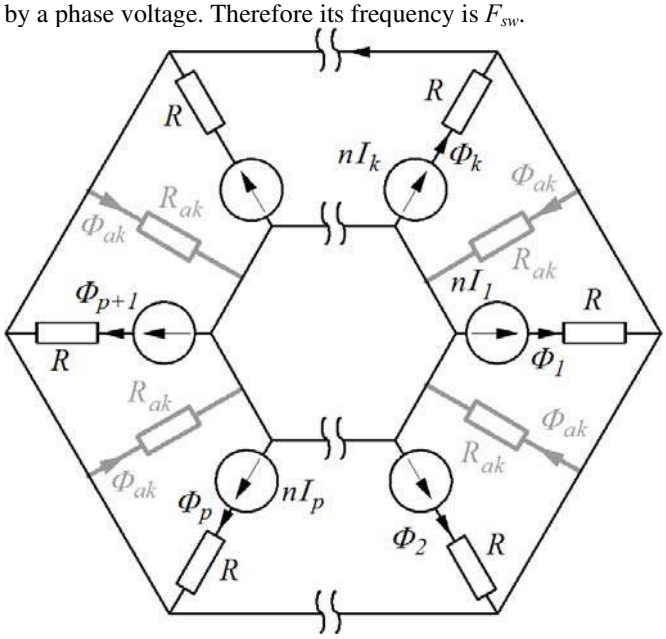
By combining (4) with the derivative of (3), it follows:

$$\frac{n^2}{R}\frac{di_p}{dt} - n\frac{d\phi_p}{dt} = \frac{n^2 R_{ak}}{k(R_{ak} + R)R}\frac{d(i_{o1} + i_{o2})}{dt}$$

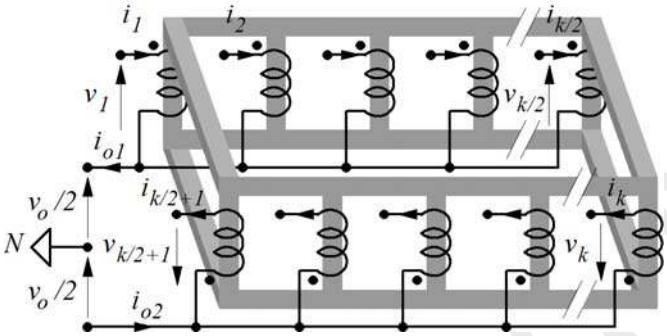
Lastly:

$$\frac{di_p}{dt} = \frac{v_{cellp} - \frac{v_o}{2}}{L} + \frac{R_{ak}}{k(R_{ak} + R)}\frac{d(i_{o1} + i_{o2})}{dt} \approx \frac{di_{mp}}{dt} + \frac{1}{k}\frac{d(i_{o1} + i_{o2})}{dt} \quad (6)$$

$i_{mp}$ is the magnetizing current of the phase p. It is generated by a phase voltage. Therefore its frequency is $F_{sw}$.




a – Complete reluctance scheme




b – Electrical arrangement and notations

Figure 4: ICT magnetic schemes

*2) Electrical model*

To use the previous analysis to derive a clear and simple model, magnetizing currents are ignored. As a consequence, all phase currents $i_p$ are identical (equation (6) with $i_{mp} = 0$) and $i_{o1} = i_{o2} = i_o$. In the real case, the magnetizing currents are summed ($i_{mT}$) in the neutral point line. Therefore, (5) and (6) become respectively:

$$\frac{v_o}{2} \approx \frac{\sum_{p=1}^{k} v_{cellp}}{k} - \frac{2L_{ak}}{k}\frac{d\,i_o}{dt} \quad (7) \qquad \frac{di_p}{dt} \approx \frac{2}{k}\frac{di_o}{dt} \quad (8)$$

Equations (7) and (8) lead to the electrical model of Figure 5. The coupled inductor of this model has a coupling ratio equal to 1 and a mutual inductance $M$ equal to $L_{ak}$. This points out the characteristic properties of ICTs:

– An output voltage resulting in the interleaving of input voltages (frequency $kF_{sw}$, amplitude $V_p/k$).

– Output voltage is applied to an output inductor that corresponds to the total leakage flux. It determines the ripple output current (frequency $kF_{sw}$) if any additional inductor is introduced.

– If magnetizing currents are ignored, phase-currents are identical.

These properties suppose an interleaving control sequence, i.e. the input voltages have the same form and are regularly phase-shifted ($2\pi/k$).

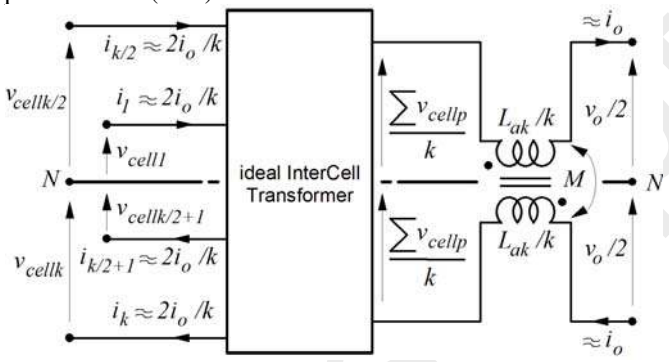
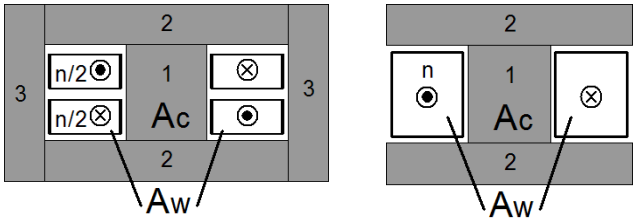



Figure 5: Electrical model of the ICT

Compared to a version that uses separate transformers, the monolithic ICT leads to a weight and volume decrease, which is why it was chosen in the present development. There is a simple way to see this decrease: to design a phase-transformer using the separate transformer option [10], the initial winding (turn number $n$) is separated into two windings (turn number $n/2$) that must be connected to two converter cells (electrical coupling). In this case, the core areas are identical in both options. As shown in Figure 6, the E-I core of the separate-transformer needs closing magnetic legs that do not exist in the monolithic ICT.

Conversely, the monolithic ICT is more difficult to build due to the need for a customized core. Section IV.A shows how this problem was solved in the present case.




a – Separate transformer (cyclic cascade) b – Monolithic ICT

Figure 6: Magnetic part reduction in monolithic ICT

## B. Design

The design of ICT basically involves the same steps as the design of other magnetic components [15]:

– Determine the current and flux densities based on circuit excitations and geometrical parameters.

– Deduce loss densities in the various parts, and then total losses by integration over the full volume.

– Estimate the temperature rise using a thermal model that takes into account the geometry and size of the ICT as well as external conditions (temperature, natural/forced convection).

Then, these steps can be included in an optimization process to make the temperature rise compliant with material limits, while minimizing an objective function (e. g. weight).

However, in the case of the ICT, these steps involve specific problems that can be summarized as follows:

– Current ripples depend on the leakage flux with a significant part flowing unguided in the air, which makes the inductances difficult to evaluate.

– This may be a high frequency current ripple, thus flowing unevenly through the conductors.

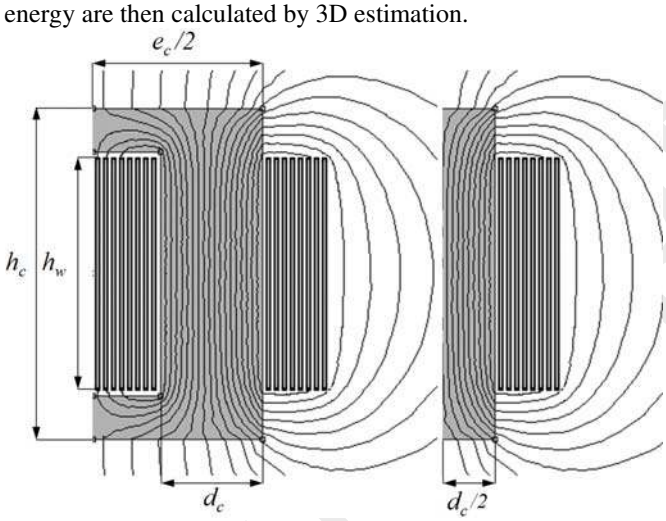
– The flux waveforms in some regions of the ICT can differ significantly from the sinusoidal waveforms used to characterize materials, and even determining the pk-pk flux is not always trivial; both of these factors make evaluating core losses a difficult task.

The following section describes how these questions were addressed to define a general design method and apply it to this component. Simplified models of the various aspects of the design were developed and included in a Matlab optimization routine. More accurate calculations are proposed outside the optimization routine to check the design before construction of the prototype.

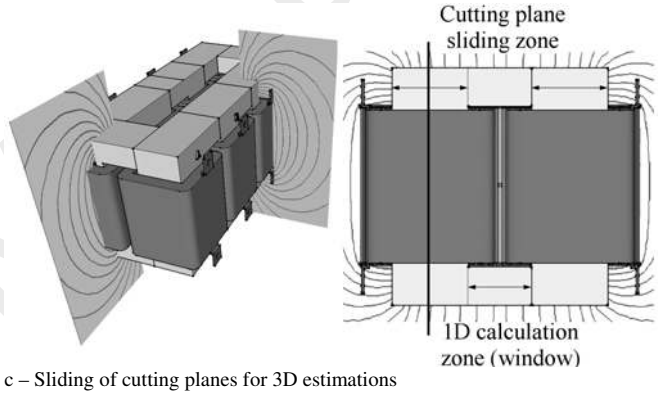
*1) Winding losses and leakage inductances*

The design of a monolithic ICT such as that in Figure 3 is, strictly-speaking, a 3D electromagnetic problem, especially when AC resistance and leakage fluxes are concerned. However, it is interesting and possible to develop a design procedure using simpler models. The proposed method is to identify cutting planes (2D) that can be slid to make an approximate 3D description of the ICT. Figure 7-b shows such a cutting plane that was be used for the present shape. It corresponds to the external parts of the columns (reference sizes on Figure 7-b). The cutting plane can be found all around the ICT, excepted in the winding windows and corners, and does not take into account the center of the ICT. In the following, it is assumed that the electromagnetic energy and current densities calculated on this plane in 2D conditions are close to those of the same plane in the real 3D configuration. 3D FE simulations (COMSOL) confirmed the validity of this assumption. The 3D estimations are thus made by sliding the cutting plane along the ICT faces (Figure 7-c) to calculate the total electromagnetic energy in the volume. In this approach, the 1D analytic model derived by Dowel [15] is used in the windows, but the electromagnetic energy in the winding corner zones and at the center of the ICT is ignored. Therefore, the leakage inductance is under-estimated and current ripple overestimated. A similar method is applied to the calculation of the AC winding losses.

To make that 2D-3D method more compliant with a design routine including optimization, i.e. avoiding 2D FE simulation on each step, a response surface using intensive *a priori* simulation was created. 2D Finite Element simulations (FEMM software) with different values for geometrical parameters (Figure 7-a) were made for different frequencies and for common mode currents ($I_{cellp}$=+$I_{cellp+1}$), as well as differential mode currents ($I_{cellp}$=-$I_{cellp+1}$). The results are the values of AC resistances/meter and leakage inductances/meter for both modes. This database file is used subsequently by the design routine to evaluate AC resistances, leakage inductances, and magnetizing inductances by means of interpolation. The total AC winding loss density of the plane is calculated by summing up the contributions of the different harmonic currents (DC, AC common mode and AC differential mode). The total winding losses and leakage energy are then calculated by 3D estimation.




a – ICT phase sizes b – Used cutting plane




c – Sliding of cutting planes for 3D estimations

Figure 7: Modeling of the k-phase ICT

*2) Core Losses*

In the monolithic ICT, the electrical circuit imposes a square AC voltage across the winding that induces a triangular flux in the vertical legs (1), of which peak amplitude can be determined easily:

$$\Phi_{pmax} = max\left[\frac{D(1-D)}{2nF_{sw}}V_{DC}\right] = \frac{V_{DC}}{8nF_{sw}} \quad (9)$$

$D$ being the duty-cycle

From the leakage inductance calculations of the previous step, the reluctance values corresponding to the network of Figure 3 can be estimated. The knowledge of this network, and of the shape of fluxes $\Phi_p$, enables us to deduce the other fluxes in the other parts of the core (Figure 8).

As a first approach, i.e. during the optimization process, core losses are evaluated using the peak-to-peak values of these fluxes that are introduced in a modified Steinmetz model [15], of which the form is:

$$Loss\ density = \left(K_1.f^{\alpha_1} + K_2.f^{\alpha_2}\right)\Delta B^{(\beta - a_\beta.f)} \quad (10)$$

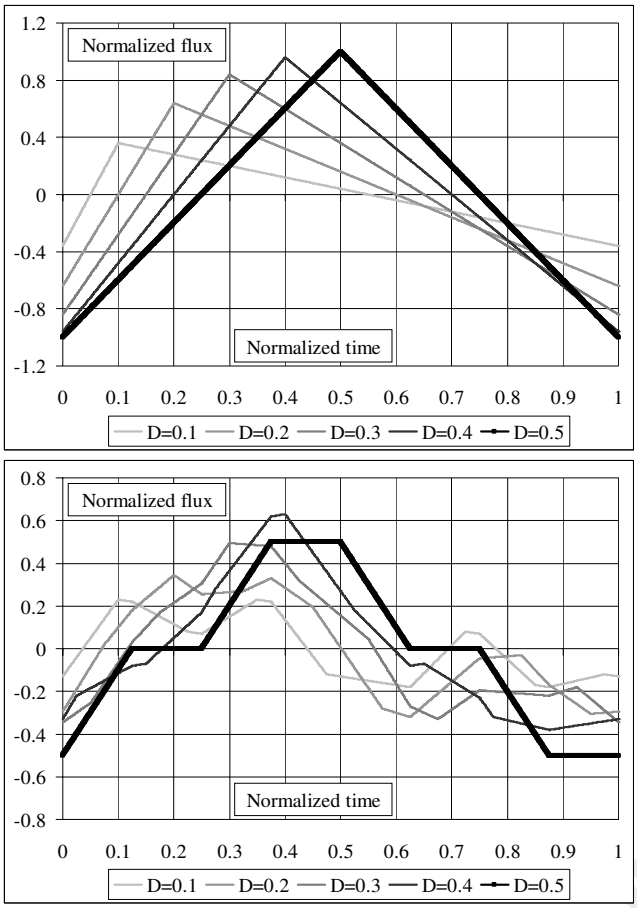



Figure 8: Induction vs. time for different duty cycles, in winding legs (top), in linking legs (bottom). Normalization based on the maximum triangular flux.

*3) Thermal model*

In the final system, the ICT is cooled by a forced-air flow with an input temperature equal to 55°C (UPS system specification). A first step is to assume that core and winding temperatures are homogenous. Their respective exchange surfaces are calculated as a function of the different size and shape parameters. Based on experience, by considering the size range of the ICT and the air-speed expected in the final system (5m/s), the exchange coefficient value is set to 35W/K/m².

*4) Design by optimization*

The ICT is defined as a 3D object by means of a set of parameters that includes independent size parameters and the number of cells. Using the previously described approach, the geometrical dimensions ($h_c$, $d_c$, $h_w$, $e_c$ and the number of turns) are varied by means of Matlab's standard *fmincon* gradient routine, which tends to minimize weight (sum of core weight and conductor weight is the optimization function) while checking that core losses, winding losses and the thermal model predict an acceptable temperature rise (inequality constraint). In this case, the number of cells was not allowed to vary. The only original point of our approach is probably that the current ripple, which is often considered as a specification for magnetic design, is considered here as a simple unconstrained output. In fact, high current ripples tend to increase losses, and optimizing for weight naturally limits this current ripple to an acceptable level.

Concerning the initial guess, a good practice seems to be to start with an ICT that satisfies constraints to help convergence. With this kind of problem, it is sufficient to consider a large ICT as an initial guess to allow the algorithm to converge.

The optimization results are given in Table 1. Figure 9 shows the initial guess and the final device.

TABLE 1: OPTIMIZATION RESULTS

| | | | | |
|---|---|---|---|---|
| Geometrical values | $h_c$ | 91.54mm | $Vol_c$ | 878cm3 |
| | $d_c$ | 29.00mm | $Vol_{Tot}$ | 1,478cm3 |
| | $h_w$ | 67.55mm | $Weight_w$ | 1.625kg |
| | $e_c$ | 99.92mm | $Weight_c$ | 4.089kg |
| | $Vol_w$ | 600cm$^3$ | $Weight_{Tot}$ | 5.714kg |
| Electrical values | $V_{Cell}$ | 400V | $J$ | 3.47A/mm² |
| | $I_{cell}$ | 90A | $P_{wTotal}$ | 269W |
| | $F_{sw}$ | 20kHz | $P_{wHF}$ | 33W |
| | $L_{ak}$ | 12.9µH | *Ripple* $\Delta i_p$ | 6.5A |
| | $L_{magn}$ | 562µH | *Efficiency* | 99.77% |
| Magnetic values | $n$ | 15 | $P_c$ | 72W |
| | $B_{DC}$ | 0.1269T | $P_{Tot}$ | 341W |
| | $B_{max}$ | 0.360T | | |
| Thermal values | $h_{exchw}$ | 35W/K/m² | $\Delta\theta_w$ | 45°C |
| | $h_{exchc}$ | 35W/K/m² | $\Delta\theta_c$ | 32°C |

Index *w* for winding, index *c* for core, see figure 7-a for ICT size notations

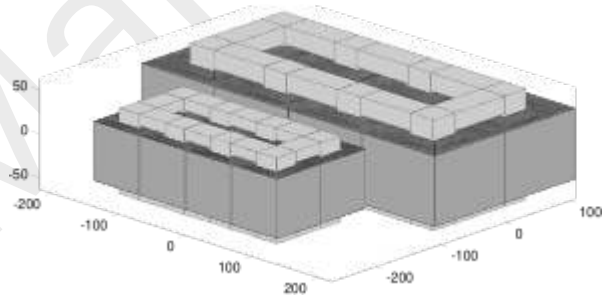


Figure 9: Dimensions of the ICT, Right: initial guess, Left: optimized device

The calculated material volume is less than two liters and the weight is close to 6 kg. The core temperature is 85°C and the winding temperature is 100°C. The current ripple per cell is very low (around 5A), this being one of the advantages of that particular magnetic solution compared to classic separated inductors.

In the present case, the part of the HF winding losses $P_{wHF}$ in the total winding losses $P_{wTotal}$ is low, but this is due to the low value of current ripple. It should be noted that other configurations can bring very high AC losses and it is necessary to include the AC loss calculation in the general design method. It can be also observed that the core losses are significantly lower than the conductor losses. This is related to the medium frequency used (20 kHz). For such a value, the core size is mainly determined by the maximal induction in the material and not by the core losses, which remain low.

*5) Final check*

With optimization converged, several checks can be made: AC resistance and leakage inductance are calculated via finite elements with the optimized dimensions to improve the estimation made by interpolation. In the present case, the main verification concerns the leakage inductance that imposes the current ripple. The value extracted from this checking

simulation is $L_{ak}$ = 13.5µH, to be compared with the 12.5µH value given by the interpolation. To verify this leakage inductance range, a 3D FE simulation (COMSOL) was added and gives a value of 18.4 µH. This is significantly higher, which is in accordance with the under-estimation of the 2D-3D method evoked III.B.1). The difference is close to 30% but the current ripple estimation does not require more accuracy, considering its low value.

Core losses are also re-calculated. Knowing the fluxes and induction in all branches of the core, the iGSE [16][17] is applied to these complicated waveforms (Figure 8) to estimate the extra losses induced by the *dB/dt* that is significantly higher than that of a triangular waveform with the same *pk-pk* amplitude. In this design, we find that the maximum *pk-pk* induction (obtained at 50% duty cycle) is 0.37T in the windings and 0.44T in the linking legs, but it is mainly the higher *dB/dt* observed in linking legs that generates a higher loss density (95kW/m$^3$ in the linking legs vs. 60kW/m$^3$ in the winding legs). As a consequence, the total core losses are re-evaluated at 86W instead of 69W in the optimization process.

Lastly, temperature estimations are verified by 3D FE simulations (ANSYS icepack). The virtual calculated device is placed in an air-flow with an input temperature of 55°C and a speed of 5m/s. Simulation results are given in Figure 10. The air input is on the front side.

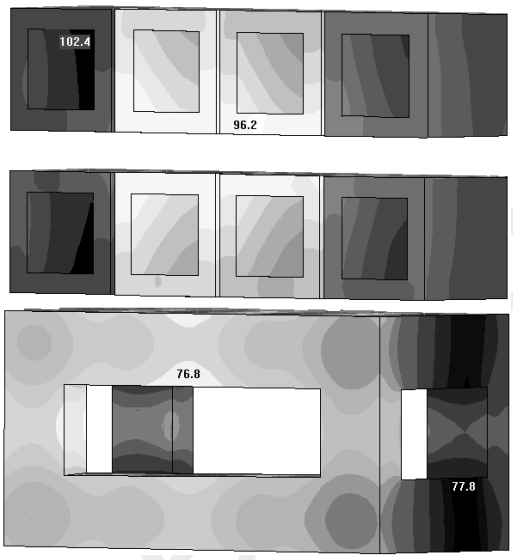



Figure 10: 3D EF thermal simulations, windings (top), and core (bottom)

The average exchange coefficient values extracted from these results are 37W/K/m² for the windings and 42W/K/m² for the core. This is close to the value used in optimization (35W/K/m²). The core exchange coefficient is not as good, but with the core temperature still being on the safe side, we decided to stick to this design. It can be observed that the assumption of a homogeneous surface temperature is correct. Indeed, the winding temperature range is [96.2°C to 102.4°C] and the core temperature range is [76.8°C to 77.8°C]. These results can be compared to those generated by the optimization routine which are respectively 100°C (45°C + 55°C) and 85°C (30°C + 55°C).

It should be noted that the first guess is not always this good and that a general design process may require at least a second iteration to fit the exchange coefficients.

### C. Comparison with a classic solution using inductors

In parallel to ICT development, an inductor solution was also extrapolated from the design of previous products (tradeoff between current ripple and losses). In the latter case, each converter cell includes two inductors such as those in Figure 11 (inductor manufacturer's proposal). The compared characteristics are given in Table 2. The ICT solution is widely better, regardless of the considered parameter.

TABLE 2: COMPARED CHARACTERISTICS

| | ICT | inductors |
|---|---|---|
| Material-core | Ferrite-U | Kool µ-toroid |
| Number | 1 | 8 x 2 (192µH) |
| Total weight | 6kg | 9.2kg |
| Max ripple current by cell | 6.5A | 53A |
| Losses | 340W | 650W |
| Cost | X | 1.4X |

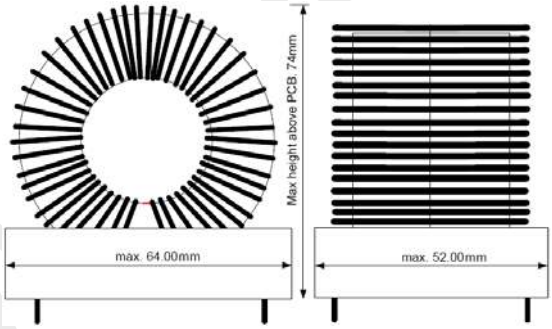



Figure 11: Elementary inductance of the classic design

## IV. BUILDING AND CHARACTERIZATIONS

### A. Building

Ferrite materials are the most appropriate in the present case, considering the switching frequency and the cost parameter. On this basis, the simplest way to build the proposed ICT is to associate eight U ferrite cores, each of them supporting phase winding. As standard U cores do not having the right dimension, special U cores were produced by a ferrite manufacturer. A photo of the prototype and a view of the U-cell are shown in Figure 12.

Such an assembly creates air-gaps on the linking legs. Their value is estimated at nearly 50µm. The only consequence of this is a decrease in magnetizing inductance, but the magnetizing currents remain negligible compared to the main currents.

Some preliminary measurements were made concerning the inductance values with an impedance analyzer. Measured leakage and magnetizing inductances are respectively $L_{ak}$ = 16.6µH and $L_{magn}$ = 500µH. These values are close to those given by the design routine.

### B. Test bench

Because the power DC/DC converter prototype is currently being developed, the ICT was tested on a test bench shown Figure 13.

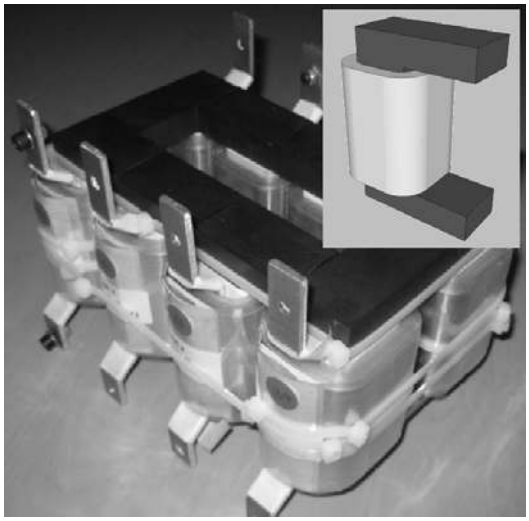


Figure 12: View of the prototype

It consists of eight standard water-cooled IGBT legs. The proposed topology enables reproducing the operating conditions of the ICT in the future converter, but only needs a 400V DC power supply and a low-value resistor. Conversely to the final converter, both groups of four legs are connected in parallel on the power supply and operate in an opposition mode, one being the generator, the other being the receiver. The duty cycles of both groups must be very close, with the voltage difference being applied to a quasi-short-circuit. The control part realizes two functions: adjustment of the current flowing between both groups, and balancing the eight cell currents.

*1) Opposition current control*

The principle of the opposition method applied to power electronic converters is described in [18]. To control the current flowing between both power stages, a differential duty cycle $\delta D$ must be generated, ideally by means of a closed current loop. The present test bench operates in an open loop with a low resistor (0.025Ω) that allows limiting the control sensitivity. Control is handled by an FPGA board. It generates the eight PWM orders with a basic duty cycle D, identical for each cell. A second control level generates the differential duty cycle $\delta D$, adjustable in steps of 1/1000. Then, the output current can be adjusted by a step of (400V).$\delta D$/0.025Ω = 16A, to compare with the nominal value of 360A. The control sequence is given in Figure 14.

*2) Current balance*

To ensure correct operations of the ICT, the phase currents must be balanced. Indeed, unbalanced conditions cause an average magnetic field to appear in the core, which can induce magnetic saturation. In the present case, a preliminary test has shown that the unbalance current must be lower than 1A, a very weak value compared to the nominal current of 90A.

To provide balance conditions [19][20], the chosen solution is to use differential current measurements on each four-cell group, e.g. measuring $i_1 - i_2$, $i_1 - i_3$, $i_1 - i_4$ for the first group, in order to obtain high accuracy on the unbalance estimation. Measurement is obtained by means of three hall effect sensors with low current capability (25A), but able to accept the crossing of two cell-lines (Figure 16). A fourth sensor (100A capability) is added to measure one of the cell-currents, here $i_1$. The differential measurements are then used to implement closed-loop balancing according to the principle illustrated in Figure 15.

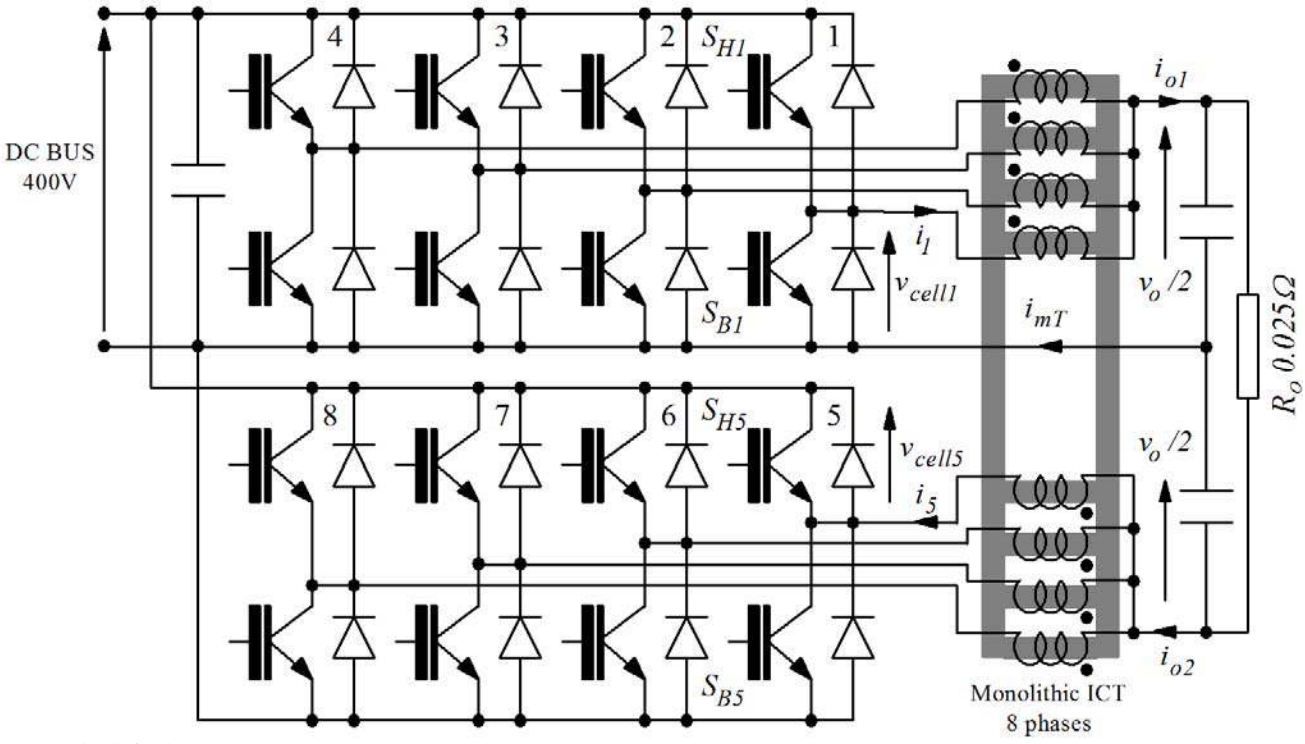



Figure 13: Circuit for the ICT test

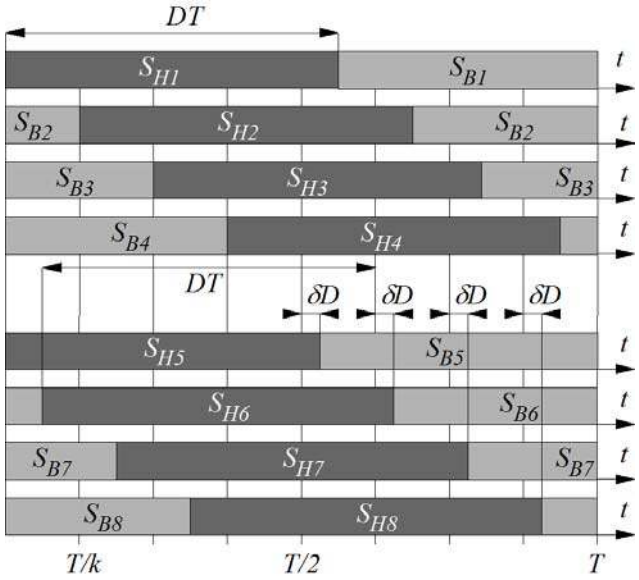



Figure 14: Control sequence

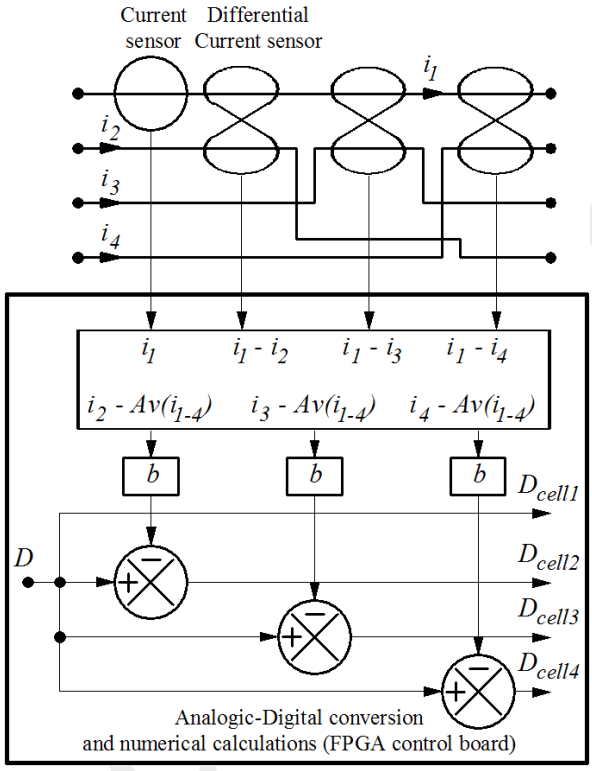



Figure 15: Differential balance loops for one four-cell group

The analog signals provided by the differential sensors are digitalized on the control board that performs the following calculations (scale factors are not considered):

$$[(i_1 - i_2) + (i_1 - i_3) + (i_1 - i_4)]/4 = i_1 - (i_1 + i_2 + i_3 + i_4)/4 = i_{cal} \quad (11)$$

then

$$i_{cal} - (i_1 - i_2) = i_2 - (i_1 + i_2 + i_3 + i_4)/4 \quad (12)$$

$$i_{cal} - (i_1 - i_3) = i_3 - (i_1 + i_2 + i_3 + i_4)/4 \quad (13)$$

$$i_{cal} - (i_1 - i_4) = i_4 - (i_1 + i_2 + i_3 + i_4)/4 \quad (14)$$

The results of (12) to (14) constitute accurate estimations of the difference between each phase current and the average of the four currents. Lastly, they are used as feedback values to correct the duty-cycle on each cell. This action tends to cancel the three current differences, therefore to cancel the unbalance. The $i_1$ measurement is used in the final system to regulate the total output courant, equal to $4i_1$ if the currents are balanced. The same control strategy is applied to the second cell-group with an input duty cycle equal to $D + \delta D$.

To summarize, the control board generates three levels of duty cycles: the main duty cycle $D$, the duty cycle $\delta D$ to adjust the current flowing between both cell-groups and the corrected duty cycles $D_{cell1}$-$D_{cell8}$ to balance the phase-currents.

Figure 16 shows several views of the test bench. A shunt (1% accuracy) is introduced in each cell output to measure and compare the average current values.

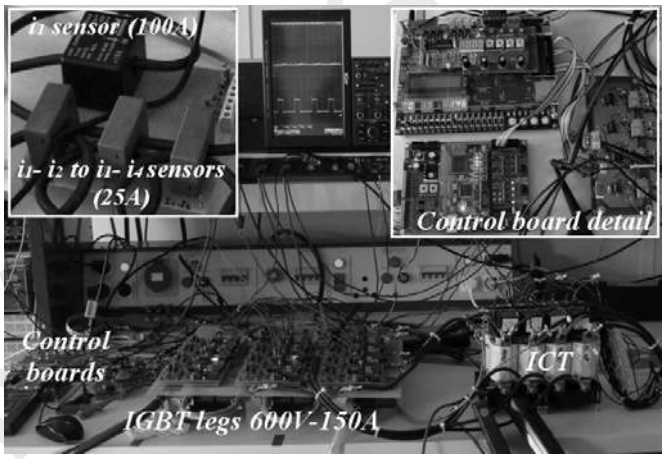



Figure 16: Test bench

### C. *Experimental results*

The test bench validated ICT operation and the balancing loop robustness. The oscillograms in Figure 17 show the four currents of one of the four-cell groups, and the voltage across one of the IGBTs for nominal power operation (400V-90A/cell). The inlay gives the average values of the same four currents. Very good current balancing can be observed, with the maximal difference (0.8%) between two measurements probably being due to shunt accuracy.

During the test, a first verification of ICT thermal behavior was made by means of an infrared camera. For the final system, it is planned to place the ICT in a ventilation tunnel behind the power semi-conductor devices. The expected temperature and speed of the incoming air should be 55°C and 5m/s respectively. This configuration is not reproduced in the test bench. Nevertheless, the ICT is placed on two horizontal fans providing an air-speed of 3.5m/s and the ambient temperature was about 25°C. Unfortunately, the thermal conditions of this free space disposition cannot be correctly defined in an Finite Element analysis.

Figure 18 shows an infrared image of the ICT for nominal power operation and under thermal stability conditions. The surface temperatures fall within a 55°C to 72°C range.

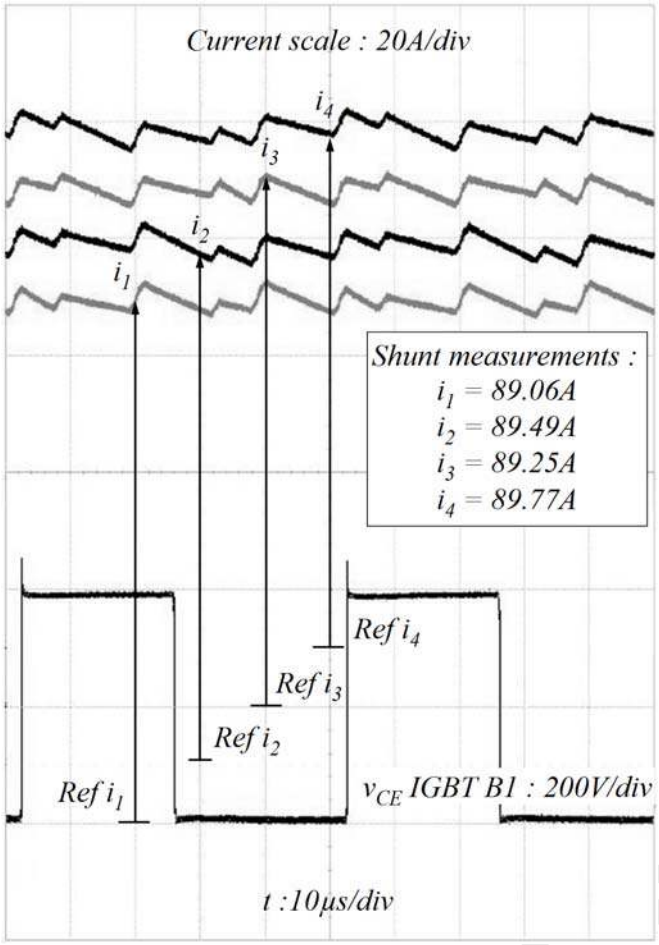



Figure 17: Waveforms at nominal operating point

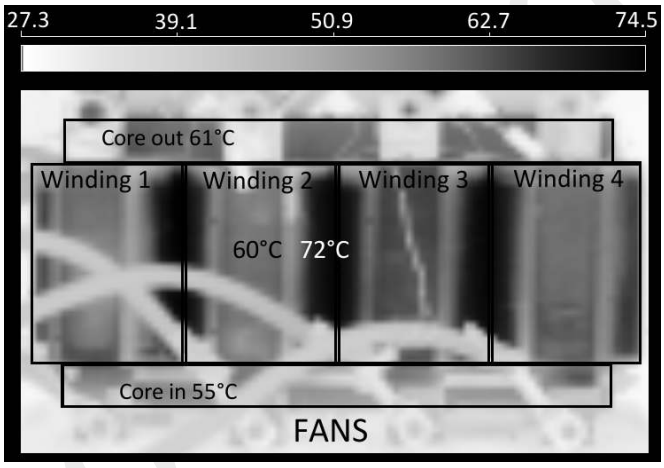



Figure 18: ICT infrared image for nominal operating points

Even this result cannot directly be compared in detail to the simulation of Figure 10, because of the different ventilation conditions, it nonetheless allow us to make some observations:

- The surface temperature range is in accordance with design estimations. Indeed, the increase in temperature range from the ambient temperature is 30°C to 47°C, close to the 32°C to 45°C range of the design.

- The good fit of temperatures demonstrates the good loss estimation given by the design routine.

- While a more detailed analysis still must be made for the final system, these results definitely validate the proposed ICT design.

## V. Conclusion

The aim of this paper is to demonstrate the interest of ICTs in the context of UPS systems, in the medium power range. Most manufacturers currently evaluate solutions based on multi-cell converter topologies for their future systems. The interleaving of cells is likely to become a standard configuration in the next generation of UPS systems. Therefore, the monolithic ICT is a very attractive option to be associated with these developments. In comparison to the separate inductor option, the monolithic ICT allows reducing weight, volume, current ripples, and cost.

To obtain these properties, it is necessary to have thorough knowledge of the characteristics and operation of this particular magnetic device, and to develop tools able to optimize its design. That is the aim of the two first parts of this paper describing the modeling approach and design routine suggested by the authors.

Building and testing a non-standard magnetic device are other original steps of that work, as presented in the third part of the paper. First, it is shown how a monolithic ICT can be built with ferrite U-cores to provide a competitive industrial solution, and a prototype is presented. Then, the prototype is placed in a test bench developed with standard IGBT legs, which use the opposition method and balancing differential loops implemented in an FPGA control board.

Lastly, experimental results obtained under nominal power conditions are presented. They confirm the efficiency of the design tools, with the characteristics of the prototype being close to those defined by the optimization routine and, considering these characteristics, the high potential of the ICT solution.

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