An Isolated Multicell Intercell Transformer Converter for Applications With a High Step-Up Ratio

François Forest, Thierry Meynard, Eric Labouré, Bertrand Gélis, Jean-Jacques Huselstein, Julio Brandelero

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Abstract—**This article proposes a converter topology dedicated to the interconnection between low voltage and high voltage networks or power sources. This topology uses the interleaving principle whose advantages are well known at this point. Its originality stems from the implementation of an isolating InterCell Transformer (ICT) that provides isolation, filtering and intercell coupling through a single magnetic stage.**

The first section of this paper presents two ways to build bidirectional multi-cell converters, based on classic buck (or boost) cells on one hand, and buck-boost cells on the other. From the non-isolated versions of these two families, the synthesis of isolated versions is achieved by introducing classic two-winding coupled-inductors or transformers.

A non-bidirectional isolated ICT version derived from the buck-boost family, the multi-cell ICT flyback converter, has already been studied and tested [1][2]. Therefore, the second section describes the isolated multi-cell ICT converter derived from the buck (or boost) family and constitutes the main contribution of this paper. Its very interesting features regarding high step-up ratio requirements are emphasized, particularly by considering some limitations of the ICT flyback converter.

Lastly, a 10 kW test bench is presented. This test bench includes eight cells and an ICT created with separated transformers, making it possible to validate converter operations under realistic power conditions.

Index Terms—Interleaved converters,

I. Introduction

Many electrical power systems currently under development require high voltage step-up converters. This is generally due to the interconnection of low-voltage sources such as batteries, fuel-cells or super-capacitors [5]-[16].

For example, the evolution of aeronautic systems typically creates such a need. New types of embedded electrical networks are required to supply new electrically-powered functions designed to replace current devices and actuators. In that respect, power distribution by medium voltage DC networks (270V-540V) is planned as their interconnection with low voltage DC safety networks (28V-48V). Because of its particular specifications, this context generates new challenges in power electronics, the main requirements being:

– High power levels with respect to low voltage (>10kW), resulting in very high current on the low voltage sides.

– High specific power in order to limit the embedded load.

– In some cases, power reversibility between the networks.

These particular factors contribute to the critical nature of designing power electronic converters that provide such a function efficiently. At the same time, many topology options can be considered. The goal of this paper is to present a family of solutions based on interleaved converters using Intercell transformers (ICTs) [1]-[4] of which the general characteristics appear to be appropriate for that specific context.

In [4] an interleaved ICT flyback converter, the isolated version of the interleaved ICT buck-boost converter was developed to address the specifications stated above. The advantages of this design were related to the low number of components per cell and the presence of a single magnetic stage (no smoothing inductors). Having a single switch in the high current path (low voltage side) is certainly an advantage, but the single switch design proves less attractive on the high voltage side.

Topologies with legs on the high voltage side and single switches on the low voltage side are described in literature, but all the advantages are never present in the same topology. In all cases, they include two cells [7]-[10], [13], [18]-[22], [24], or three cells [11][12][16][17][23], but never more. This limitation of the number of cells is a drawback to designing high power-high step-up converters, mainly due to the non-coupling of the smoothing inductors. Indeed, in that case, the increase of the number of cells can lead to both opposite negative effects [25]:

– An exaggerated reduction of the total current ripple if the current ripple is limited in each inductor (oversizing of the smoothing magnetic part)

– An exaggerated increase of the current ripple in each inductor if the total current ripple is maintained in a classic range.

In addition, two magnetic stages, transformers and smoothing inductors, are present in most cases.

To summarize: the features desired for 28V/270-540V converters are:

– Two-switch cells on the high voltage side

– Single-switch cells in the high current path

– Intercell coupling to allow high numbers of cells in parallel on the low voltage side, but no extra magnetic component.

– A wide duty cycle range (and maximum value higher than 0.5) to efficiently manage the wide voltage variation encountered with low voltage sources such as batteries.

In this paper, it is shown that the ICT interleaved converter, operating in buck mode for HV-to-LV power flow or in boost mode for reverse transfer, can be modified in an isolated version featuring all the desired characteristics. Considering its topology and operating mode, it is hereafter referred to as the buck or boost ICT converter, in order to differentiate from the buck-boost ICT converter, described at the same time.

The first part shows how isolated ICT interleaved topologies can be generated starting either from the (buck or boost) interleaved converter or from the interleaved buck-boost converter. It will first be shown how isolation can be added in both these converters, and then in a second step, how magnetic coupling can be provided to allow high numbers of cells with a reasonable current ripple.

In the second part, detailed operation of the (buck or boost) ICT converter is provided. In particular, the different modes corresponding to different ranges of duty cycles are analyzed.

These two parts consider the general case that corresponds to bidirectional topology using active switches on both sides. Unidirectional converter topologies using diodes on the LV or HV side can be derived directly from the bidirectional topology.

The third part presents results obtained with an experimental setup derived from that presented in [4]. Therefore, it is unidirectional and provides only LV-to-HV power flow. Nevertheless, the LV-to-HV configuration is often the most critical, particularly if the LV source is a 28V battery. Voltage can decrease as low as 20V. Such operating conditions lead to maximal current values on the LV side and induce maximal losses in the LV switches. If efficient operations are obtained in the LV-to-HV power flow configuration, the bidirectional version will be efficient in both cases.

Because the principles are quite different between the flyback converter described in [4] and the present converter, several modifications were required:

– Regenerative clamps were added on the low voltage side.

– The turns ratio of the ICT had to be modified.

– The HV diode cells were modified.

Experimental data obtained with this modified test bench are given and compared with those of the ICT interleaved flyback converter.

II. THE TWO FAMILIES OF MULTI-CELL ICT CONVERTERS

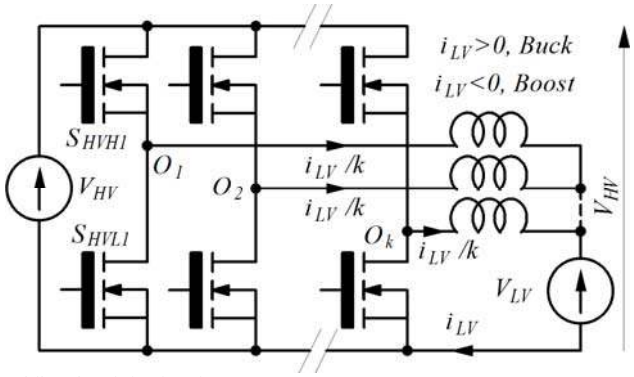
A. *Non-isolated basic topologies*

Both families are derived from the basic multi-cell topologies given Figure 1 (k cells).

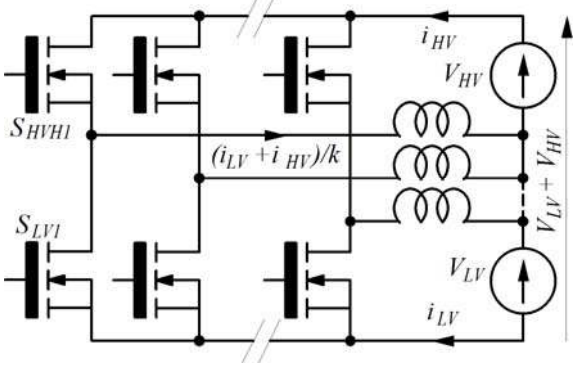
In the present context, power MOSFETs are the best devices to achieve this switching function and, therefore, will be used to represent current-bidirectional switches in all the diagrams of this paper (label S_X). According to the power flow direction, their current can be positive (controlled mode) or negative (diode operating mode as in synchronous rectifiers). Sign conventions concerning MOSFET current, labeled i_{SX}, remain unchanged in the descriptions of the operating modes.

The basic multi-cell (buck or boost) topology (Figure 1-a) is constituted by the association of bidirectional cells, each one including one inductor. It operates in buck mode for the HV-to-LV power flow and in boost mode for the LV-to-HV power flow. The Voltage Regulator Modules dedicated to processor power supply, using up to four cells, can be cited as a typical application example (non-bidirectional buck mode).

Figure 1-b describes the second option, based on the association of buck-boost cells, always including one inductor per cell. Multi-cell flyback converters are directly derived from this topology.



a) Bidirectional (buck or boost) converter



b) Bidirectional buck-boost converter

Figure 1: Basic topologies of bidirectional multi-cell converters

By supposing an interleaved control mode in both cases, the main characteristics of these converters can be respectively deduced from those of a classic single-cell buck (or boost) converter or buck-boost converter. These characteristics are summarized in Table 1. The current ripples are ignored in the current maximal values.

	Bidirectional (buck or boost) converter	Bidirectional buck-boost converter
V_{HV}/V_{LV}	$1/D_H = 1/(1-D_L)$	$(1-D_H)/D_H = D_L/(1-D_L)$
V_{SHVHM}	V_{HV}	$V_{HV} + V_{LV}$
I_{SHVHM}	I_{LV}/k	$I_{LV}/k(1-D_H) = I_{LV}/kD_L$
V_{SHVLM}	V_{HV}	
I_{SHVLM}	$-I_{LV}/k$	
V_{SLVM}		$V_{HV} + V_{LV}$
I_{SLVM}		$-I_{LV}/k(1-D_H) = -I_{LV}/kD_L$
Δi_L	$D_H(1-D_H)\,V_{HV}/L\,F_{sw}$ $(1-D_H)\,V_{LV}/L\,F_{sw}$	$D_H\,V_{HV}/L\,F_{sw}$ $(1-D_H)\,V_{LV}/L\,F_{sw}$

TABLE 1: MAIN CHARACTERISTICS OF THE CONVERTERS

Notations

- S_{HVH}, *high side MOSFET*
- S_{HVL}, *low-side MOSFET in (buck or boost) converter*
- S_{LV} *low-side MOSFET in buck-boost converter*
- V_{HV}, *voltage of HV source,* i_{HV}, *current in HV source*
- V_{LV}, *voltage of LV source,* i_{LV}, *current in LV source*
- I_{HV}, *average current in HV source,* I_{LV}, *average current in LV source*
- V_{SHVH}, i_{SHVH}, *voltage and current of MOSFET* S_{HVH}
- V_{SHVL}, i_{SHVL}, *voltage and current of MOSFET* S_{HVL}
- V_{SLV}, i_{SLV}, *voltage and current of MOSFET* S_{LV}
- V_{xM}, i_{xM}, *maximal values of the previous voltage and current*
- D_H, *duty-cycle defined on switches* S_{HVH}
- D_L, *duty-cycle defined on switches* S_{HVL} *or* S_{LV}, $D_L = 1-D_H$
- Δi_L, *current ripple in the inductors*
- F_{sw} *switching frequency*

B. Isolated topologies with non-coupled cells

The introduction of isolation in the buck or boost converter cannot be achieved directly. The topology must be modified to create an alternative bus between the HV and the LV sides.

The first change is the opening of the ground connection that allows the total current i_{LV} flowing back (Figure 1-a). Therefore, the remaining lines $O_1,...O_k$ constitute an alternative bus but the current sum on this bus is no longer null. To respect this condition and leave the current repartition in the LV branches unchanged, new switches S_{LV} must then to be added on the LV side (Figure 2-a). Lastly, they must be synchronized with the switches S_{HVL} in order to preserve the instantaneous power delivered to the LV side. This new arrangement also modifies the current repartition in switches S_{HVH} and S_{HVL}.

To establish the current repartition rules, the numbers of switches in an on-state and off-state have to be defined:

– N_{on}, number of S_{LV} and S_{HVL} switches in on-state

– N_{off}, number of S_{LV} and S_{HVL} switches in off-state

With $N_{on} + N_{off} = k$

Therefore, for the N_{off} cells where switches S_{LV} and S_{HVL} are in an off-state, the line current i_{Ooff} is:

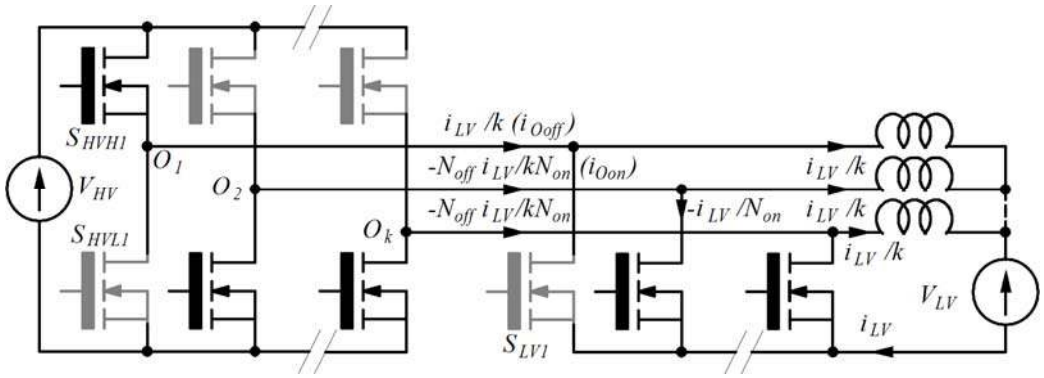
$$i_{Ooff} = i_{LV}/k$$

To obtain a null current sum on the alternating bus, the current i_{Oon} delivered by the N_{on} cells where switches S_{LV} and S_{HVL} are in an on-state must be:

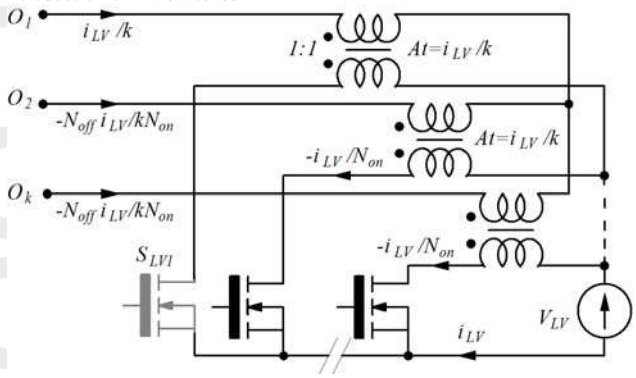
$$N_{on} i_{Oon} = -N_{off}\, i_{Ooff} \text{ then } i_{Oon} = -N_{off}\, i_{LV}/k\, N_{on} \quad (1)$$

From this equation, it follows:

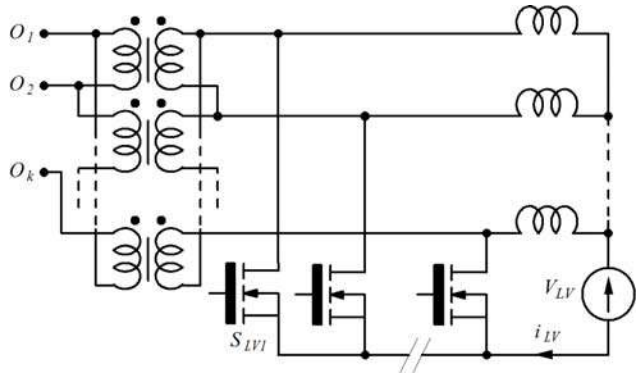
$$i_{SLVon} = i_{Oon} - i_{LV}/k = -\, i_{LV}/N_{on} \quad (2)$$



a-Introduction of LV switches



b) Isolated topology using one coupled-inductor per cell (LV part)



c) Isolated topology using one transformer and one inductor per cell (LV part)

Figure 2: Isolated version of the (buck or boost) bidirectional converter, *MOSFET in on-state black / MOSFET in off-state grey*

With the alternative bus created, isolation can now be introduced theoretically by replacing each inductor with a two-winding coupled-inductor, as shown on Figure 2-b (diagram limited to isolation and LV side). By fixing a particular 1:1 turn ratio, it can be observed that the total Ampere-turns (noted as "At") are equal to i_{LV}/k as in an inductor of the non-isolated version. Therefore, that isolation process defined an isolated converter of which the characteristics are very close to the initial characteristics. It can also be built with a "transformer-inductor" couple per cell (Figure 2-c). This option is probably more efficient, with the two-winding coupled inductor being well known for its problematic design (additional conductor losses due to the air gap). Under this last form, it constitutes the general representation of different configurations (two or three cells) described in literature [7]-[13], [16]-[24] by various names (current-fed boost converter, current-fed push-pull converter, two-inductor boost converter, current-doubler or tripler converter or rectifier, half-bridge, …). Considering both operating modes associated to both power flow directions, it will be referred to here as an isolated bidirectional buck or boost converter.

For the second option, the buck-boost converter, it is well known that the introduction of isolation is immediate because the inductive bus between the HV and LV sides is intrinsically alternating. Isolation is achieved by replacing the k inductors by k two-winding coupled inductors.

Table 2 summarizes the main characteristics of both isolated converters by considering the turn ratio m defined below. Except for the m weighting, most are unchanged compared to those of non-isolated versions.

	Bidirectional isolated (buck or boost) converter	Bidirectional isolated buck-boost converter
V_{HV}/V_{LV}	$m/D_H = m/(1 - D_L)$	$m(1 - D_H)/D_H$ $= mD_L/(1 - D_L)$
V_{SHVHM}	V_{HV}	$V_{HV} + mV_{LV}$
I_{SHVHM}	I_{LV}/mk	$I_{LV}/mk(1 - D_H)$ $=I_{LV}/mk\ D_L$
V_{SHVLM}	V_{HV}	
I_{SHVLM}	$- N_{off}\ I_{LV}/mk\ N_{on}$	
V_{SLVM}	V_{HV}/m	$V_{HV}/m + V_{LV}$
I_{SLVM}	$- I_{LV}/N_{on}$	$- I_{LV}/k(1 - D_H) = - I_{LV}/kD_L$
Δi_L	$D_H(1 - D_H).V_{HV}/mL\ F_{sw}$ $or\ (1 - D_H).V_{LV}/mL\ F_{sw}$	$D_H.V_{HV}/mL\ F_{sw}$ $or\ (1 - D_H).V_{LV}/mL\ F_{sw}$

TABLE 2: MAIN CHARACTERISTICS OF THE ISOLATED BIDIRECTIONAL CONVERTERS

Additional notations

$m = n_{HV}/n_{LV}$, *turn ratio of the coupled-inductor*

Modifications (grey cells in Table 2) only concern the current repartition in the isolated buck or boost converter that depends on number of switches S_{LV} in an on-state. This point will be developed in the next section.

C. *Topologies with InterCell Transformers (ICT)*

The InterCell Transformer (ICT) principle has been widely described in [1]-[4]. ICTs can be "monolithic" (one magnetic core with k branches) or made by interconnecting k separated transformers. An non-isolated ICT topology is obtained by replacing the k classical inductors by a non-isolated k-phased ICT.

The buck-boost converter and its isolated version, the ICT flyback converter, were presented and tested experimentally in [1][4]. It is not re-examined here.

The operating modes and characteristics of the ICT buck or boost converters are detailed in the next section.

III. THE MULTI-CELL BUCK OR BOOST ICT CONVERTER

A. *Non-isolated version*

All the properties of the isolated buck or boost ICT converter can be deduced from those of the non-isolated converter. Therefore, this presentation focuses on the latter and is based on the detailed diagram in Figure 3-b. This includes a simplified ICT model (Figure 3-a) elaborated in [3], in which magnetizing currents are ignored. This model takes into account the composition of the k cell voltages achieved by the ICT that is applied to an internal inductor L_{it} depending on the used magnetic structure. It stems from the following equation, characteristic of general ICT behavior:

$$v_{it} = \frac{\sum_{p=1}^{k} v_p}{k} - L_{it}\frac{di_{it}}{dt} \quad (3) \text{ and } i_p = i_{it}/k$$

In the present case, the particular form of this equation is:

$$v_{it} = V_{LV} = \frac{\sum_{p=1}^{k} v_{SLVp}}{k} - L_{it}\frac{di_{LV}}{dt} \quad (4) \text{ and } i_p = i_{LV}/k$$

Operation analysis using equations (1), (2), and (4) is possible, but they must be completed by the knowledge of N_{on} and N_{off}, whose values depend on the duty cycle. The higher the duty cycle, the higher the number of S_{LV} switches simultaneously in an on-state. Interleaving defines k ranges of duty cycles of which the width is $1/k$. Table 3 gives the N_{on} and N_{off} dependency with these duty cycle ranges, q being the range order. Due to the switching occurring on each T_{sw}/k interval, two values of numbers N_{on} and N_{off} (mode 1 and 2) are associated with each range.

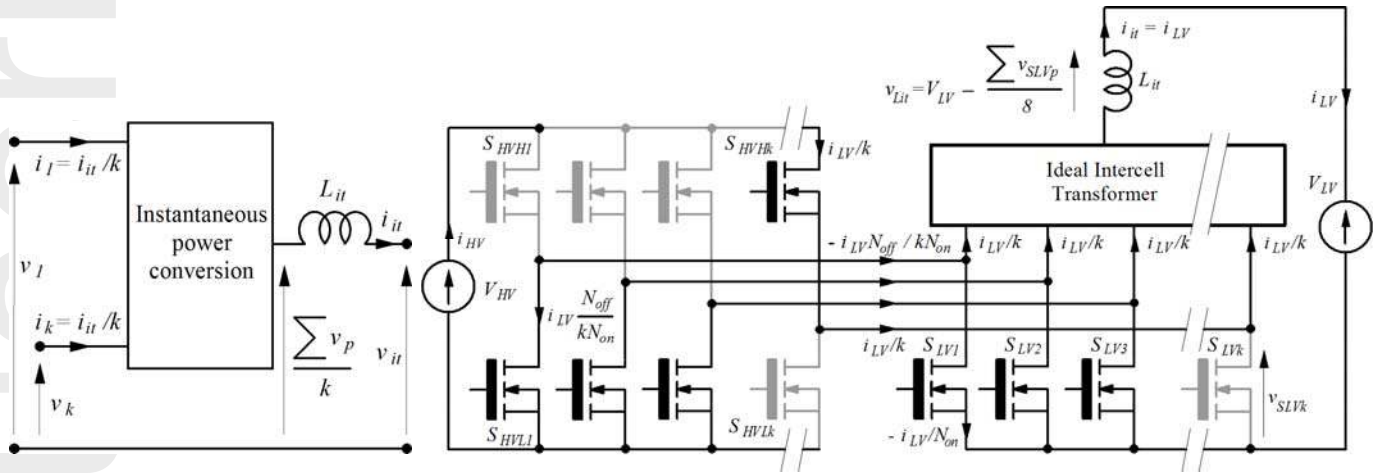
The particular case where $k = 8$ is used as an example here and in the next example because the experimental test bench is created with this number of cells. All the theoretical results can be generalized to any number of cells.

Except for the particular range 1, that will be analyzed at the end of that section, these operating conditions are available for both power flow directions. Therefore, when the power flow direction changes, the only consequence is a change of the current signs. From these observations, theoretical electrical waveforms can be established. Figure 4-a shows an operating mode corresponding to the HV-to-LV power flow direction, with $D_H < 0.5$. In this case, the current i_{LV} is positive.

A $k.F_{sw}$ total current ripple, resulting from the application of the interleaved voltage to L_{it}, is superposed to i_{LV}, as suggested by equation (4) (voltage ripple value V_{HV}/k, ripple frequency $k.F_{sw}$). According to the operating principle of ICTs, that total current ripple is proportionally reflected on the current of each cell. Therefore, the current waveforms in the switches are deduced from equations (1)(2) by considering the duty cycle value that defines N_{on} et N_{off} and by superposing the total ripple current divided by k.

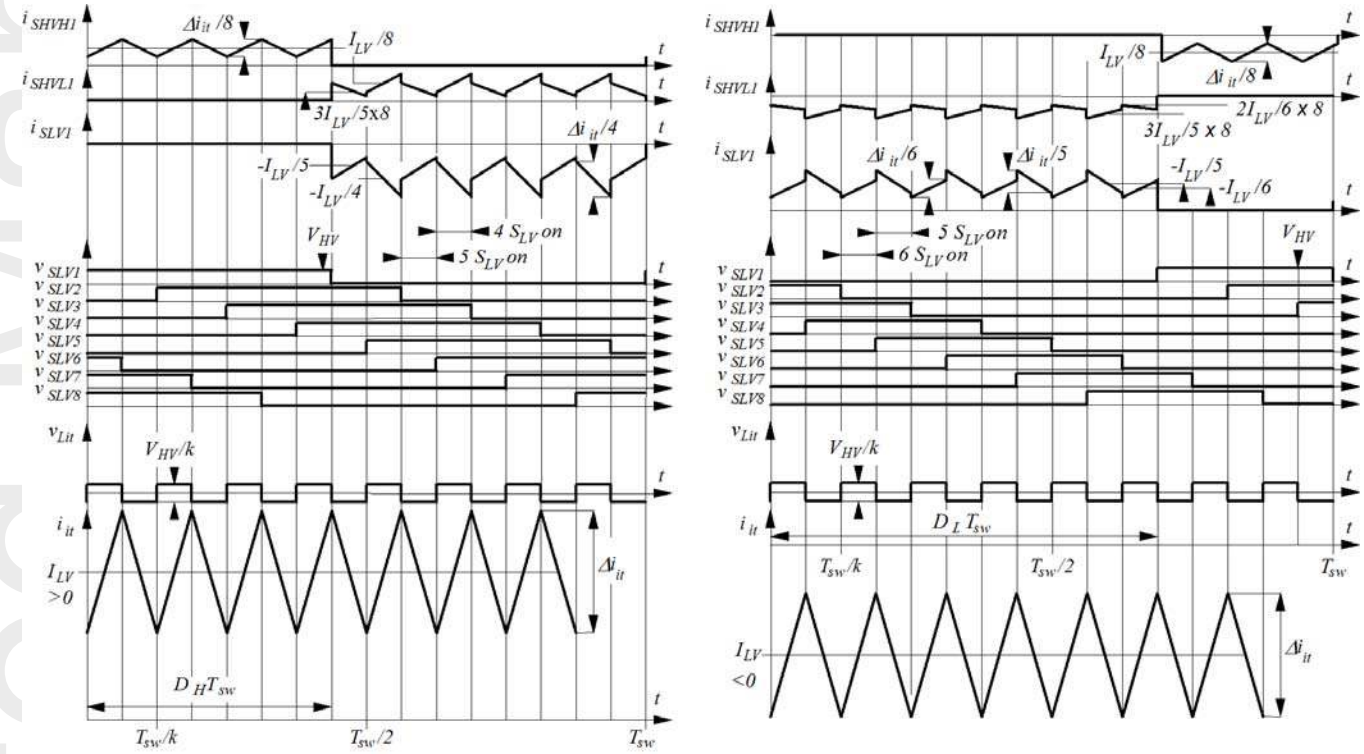
Duty cycle ranges		Mode 1		Mode 2	
		N_{on}	N_{off}	N_{on}	N_{off}
$(k-q+1)/k \geq D_H > (k-q)/k$ $(q-1)/k \leq D_L < q/k$		$q-1$	$k-q+1$	q	$k-q$
range 1 LV-to-HV	$0.000 \leq D_L < 0.125$ $1.000 \geq D_H > 0.825$	Theoretically not allowed			
range 1 HV-to-LV	$0.000 \leq D_L < 0.125$ $1.000 \geq D_H > 0.825$	8 S_{LV}	8 S_{HVL}	1	7
range 2	$0.125 \leq D_L < 0.250$ $0.875 \geq D_H > 0.750$	1	7	2	6
range 3	$0.250 \leq D_L < 0.375$ $0.750 \geq D_H > 0.625$	2	6	3	5
range 4	$0.375 \leq D_L < 0.500$ $0.625 \geq D_H > 0.500$	3	5	4	4
range 5	$0.500 \leq D_L < 0.625$ $0.500 \geq D_H > 0.375$	4	4	5	3
range 6	$0.625 \leq D_L < 0.750$ $0.375 \geq D_H > 0.250$	5	3	6	2
range 7	$0.750 \leq D_L < 0.875$ $0.250 \geq D_H > 0.125$	6	2	7	1
range 8	$0.875 \leq D_L < 1.000$ $0.125 \geq D_H > 0.000$	7	1	8	0

TABLE 3: N_{ON} AND N_{OFF} VALUES VERSUS DUTY CYCLE



a) ICT simplified model b) Detailed diagram

Figure 3: Multi-cell ICT (buck or boost) converter



a) HV-to-LV configuration (range 4) b) LV-to-HV power flow configuration (range 6)

Figure 4: Theoretical waveforms, eight-cell example

The approach is identical for the LV-to-HV power flow direction, the current signs simply being inverted (Figure 4-b, $D_L > 0.5$)

Current ripple evolution is an important feature of the ICT converter design. It can be evaluated with regard to the HV voltage source or LV voltage source. The results can be different and, considering the nature of interconnected sources, one or another solution is appropriate. The following equations (details in Appendix) give the theoretical current ripple value in each case, for both converter families.

Versus V_{LV}, for the two families:

$$\Delta i_{it} = \frac{[kD_L - q + 1][q - kD_L]}{1 - D_L} \frac{V_{LV}}{k^2 L_{it} F_{sw}} \qquad (5)$$

Versus V_{HV} for the buck-boost converter:

$$\Delta i_{it} = \frac{[kD_L - q + 1][q - kD_L]}{D_L} \frac{V_{HV}}{k^2 L_{it} F_{sw}} \qquad (6)$$

Versus V_{HV} for the buck or boost converter:

$$\Delta i_{it} = [kD_L - q + 1][q - kD_L] \frac{V_{HV}}{k^2 L_{it} F_{sw}} \qquad (7)$$

Figure 5 shows the normalized current ripples in each case versus the duty cycle D_L. Versus D_V, these curves are simply inverted according to the abscissa axis. They show an evolution due in part to the interleaving effect, and partly due to the behavior of the basic cell. Therefore, if V_{LV} dependency is considered, the curves are the same for both converters. The maximal current ripple value on each interleaving interval increases with D_L as the current ripple continuously increases with D in a buck-boost or boost single cell supplied by a constant voltage V_{LV}.

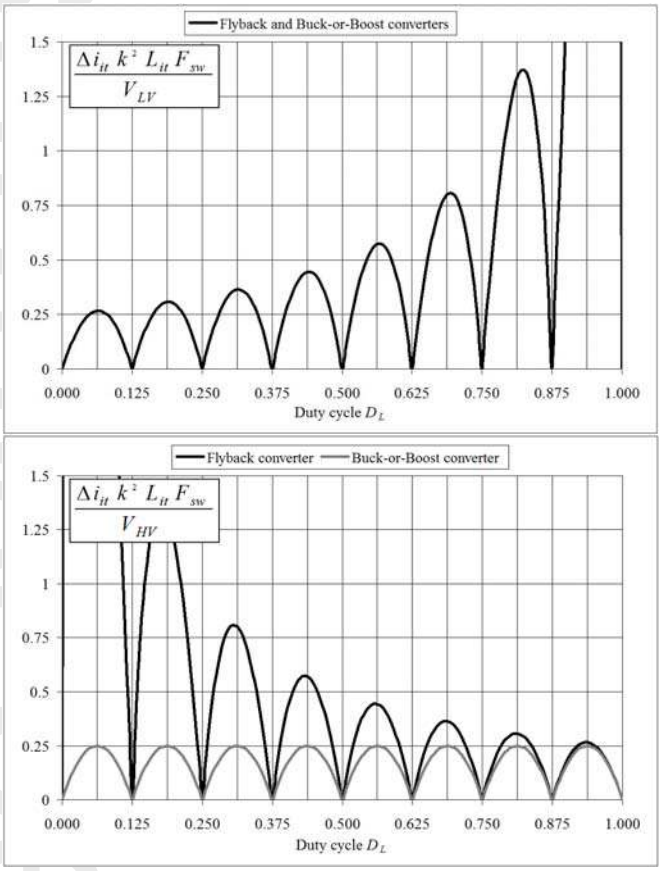


Figure 5: Current ripples in ICT converters, versus V_{LV} (top) and V_{HV} (bottom), eight-cell example

The V_{HV} dependency is different. Indeed, the buck-boost cell and buck cell must be considered at this point. For the buck-boost cell, the current ripple evolution is symmetrical to the previous one as it can be observed in a buck-boost single cell. As it is well known for the buck cell, the maximal ripple current value on each interleaving interval is constant. Therefore, the current ripple is significantly lower than in the buck-boost case over the entire duty-cycle range, giving the buck or boost converter an additional advantage in case of a regulated HV voltage bus.

At the beginning of this section, the particular case of range 1, in which all the LV switches are in an off-state, was mentioned. In the LV-to-HV power flow direction, this range must be avoided because operating conditions are no longer respected (current sum non-null on the AC bus). It can be used in the HV-to-LV power flow direction, but that induces a major change in the operating mode by creating a particular operation: all the switches S_{HVL} being in an off-state, any current can flow on the AC bus (Figure 3) but the k LV MOSFET's internal diodes become spontaneously conductive to maintain the current flow on the ICT LV side. This situation occurs k times per period, when the off-state duration of S_{HVL} switches become higher than $T_{sw}\,(k-1)/k$ (Figure 6). During that particular interval, the k voltages across the k switches S_{LV} are null and the output voltage of the ICT is strongly modified. The LV-to-HV relation then becomes:

$$V_{LV} = (1 - D_H)\, V_{HV}\, (k-1)$$

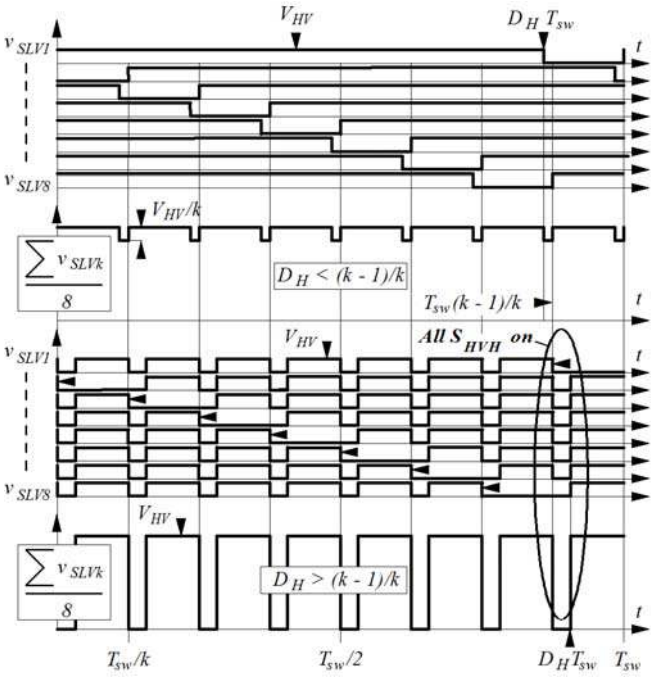


Figure 6: Particular operating mode for $D_H > (k-1)/k$, eight cell example

Therefore, V_{LV} reaches the maximal value $V_{HV}\,(k-1)/k$ for $D_H = (k-1)/k$ and then decreases to zero for $D_H = 1$.

That particular operation is not really usable because it induces high current stress on the switches S_{HVL} ($I_{it}\, N_{off}/\, k\, N_{on}$, with N_{off} high and N_{on} low).

B. Isolated version

The principle of the isolated ICT is described in [1]. It can be directly extended to the building of the isolated buck or boost converter. The theoretical diagram is shown in Figure 7, in the particular case of a monolithic ICT, easier to represent.

The ICT can also be realized with separated transformers, a solution that is used in the test bench described in section IV.

Compared to classic solutions using inductors, the ICT solution provides the following advantages:

– The average flux flowing into the different core legs is the total average leakage flux divided by k. For high values of k, it is significantly lower than the alternating flux. In an inductor, the average flux-alternating flux ratio is always the same as the average current-ripple current ratio. Therefore, the magnetic part is significantly reduced in a multi-phase ICT.

– For high k values, the intrinsic leakage inductor L_{it} is sufficient for filtering. Therefore, the air gap is eliminated and, in the case of the separated transformer option, all types of cores can be considered, including amorphous or nanocrystalline material cores.

In isolated interleaved converters, only one magnetic stage is necessary, constituted of one monolithic component or of k separated transformers. This last configuration is also obtained with two-winding coupled inductors but, in addition to the average flux consideration, they suffer from the air-gap effect on conductor losses.

In a monolithic ICT, the total magnetic core is smaller than in the separated transformer option because some magnetic parts are shared. The counterpart is the need for a specific magnetic core and higher sensitivity of the windings to high frequency current components (conductor losses), which is critical in isolated converters. Therefore, the monolithic option is more appropriate for non-isolated converters. The separate transformer option allows using standard cores and the behavior of each magnetic cell is very similar to classic transformer behavior. Therefore, HF conductor losses can be limited by introducing the same kinds of winding arrangements (imbrications).

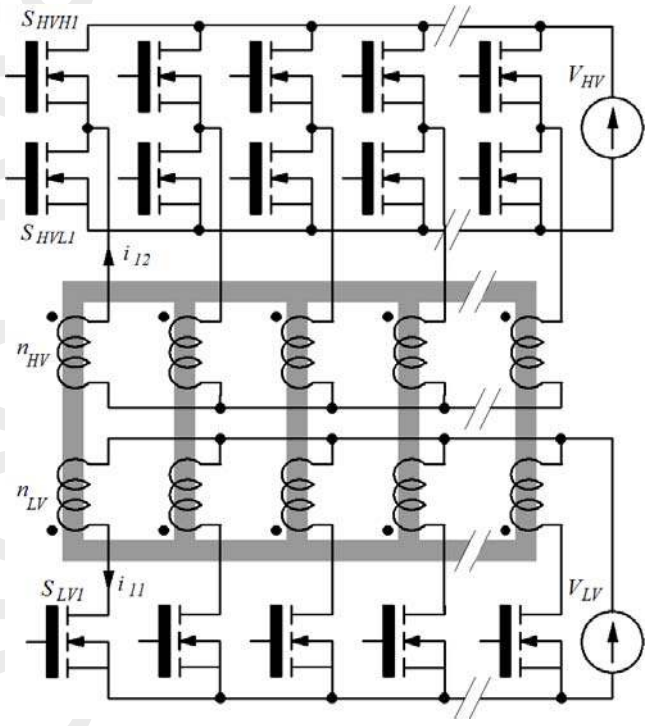


Figure 7: Isolated (buck or boost) ICT converter

The magnetic flux distribution in an ICT is very particular. This can be illustrated by considering the example of an isolated monolithic ICT (Figure 8), assumed symmetrical and closed in upon itself. In the present converter, the main fluxes Φ_p are generated by the interleaved voltages v_p applied to the windings as follows:

$$v_p - V_{LV} = n_{LV} \frac{\Phi_p}{dt},$$

in case of an excitation imposed on the LV side.

In such a magnetic component, the sum of main fluxes can only flow into the air, and constitutes the total leakage flux Φ_a.

The representations in Figure 8-a are made by supposing two simplifying assumptions:

– The reluctance of transverse legs is negligible compared to the reluctance of the leakage zones.

– These leakage zones are distributed symmetrically and mainly located in the inter-winding spaces. The real distribution is more complex, with leakage fluxes flowing all around the magnetic legs, but this cannot be described by a simple diagram.

With these assumptions, the leakage fluxes Φ_{ak} in the inter-winding spaces are identical and equal to Φ_d/k, itself equal to the sum of the main fluxes that have a triangular shape imposed by the rectangular interleaved voltages. The transverse flux distribution can be deduced by superimposing the k contributions of each main flux in the transverse legs, as shown in Figure 8-a (all the flux values are normalized with regard to main flux amplitude). For an eight cell ICT, the calculation gives:

$$\Phi_{t1} = \frac{\Phi_1}{2} - \frac{3\Phi_2}{8} - \frac{\Phi_3}{4} - \frac{\Phi_4}{8} + \frac{\Phi_6}{8} + \frac{\Phi_7}{4} + \frac{3\Phi_8}{8} \quad (8)$$

This leads to the transverse flux shape in Figure 8-a, drawn on the normalized switching period. Other transverse fluxes are obtained by a circular permutation of indexes.

For the isolated ICT, the current distribution in the two windings of the same phase can be approximated by using the one cell reluctance circuit in Figure 8-b. R, R_T R_{ak} are respectively the reluctances of the main legs, transverse legs and leakage zones. A reluctance R_{a1} can be added to represent the leakage flux between the two windings of the same phase. If R_{a1} is not considered, it becomes:

$$n_{LV}\, i_{11} + n_{HV} i_{12} = R\Phi_1 + 2R_T\Phi_{t1} + R_{ak} \frac{\sum \Phi_p}{k} \quad (9)$$

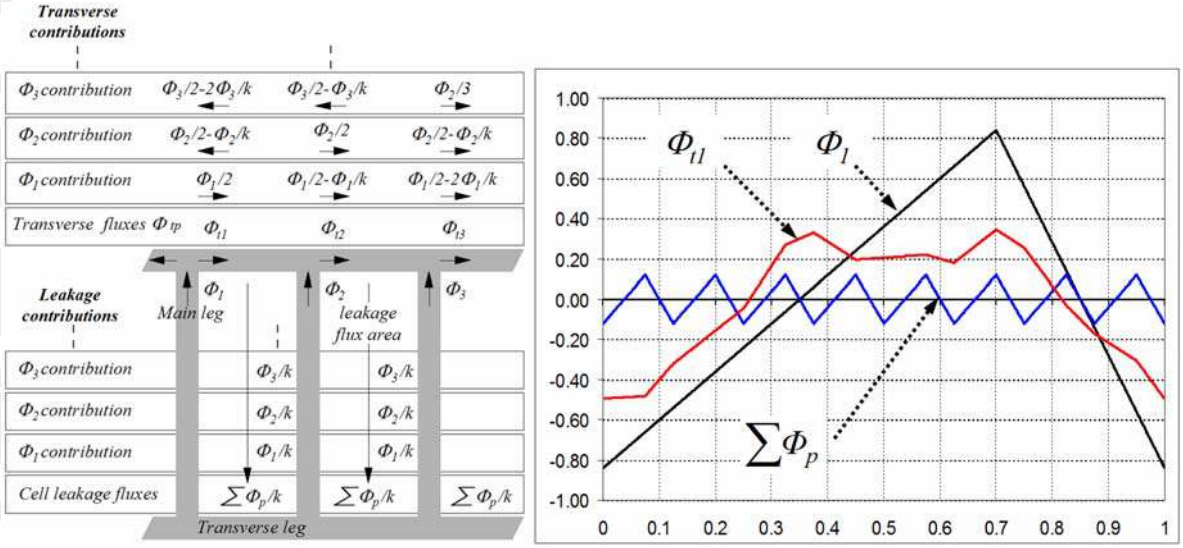
The flux term specific to each phase that generates the magnetizing phase current is $R_{F1}+2R_T\Phi_{t1}$. By supposing that introduction of a transverse reluctance R_T does not significantly modify the previous Φ_{t1} shape (true is $R_{ak} >> R_T$), the application of equation (9) gives the ampere-turn shapes in Figure 8-b. The magnetizing ampere-turn shape is close to the triangular shape observed in a classic transformer supplied by rectangular voltage.

In the separated transformer option, the flux in each core and the magnetizing ampere-turns have the same shape as the transverse flux in the monolithic ICT.

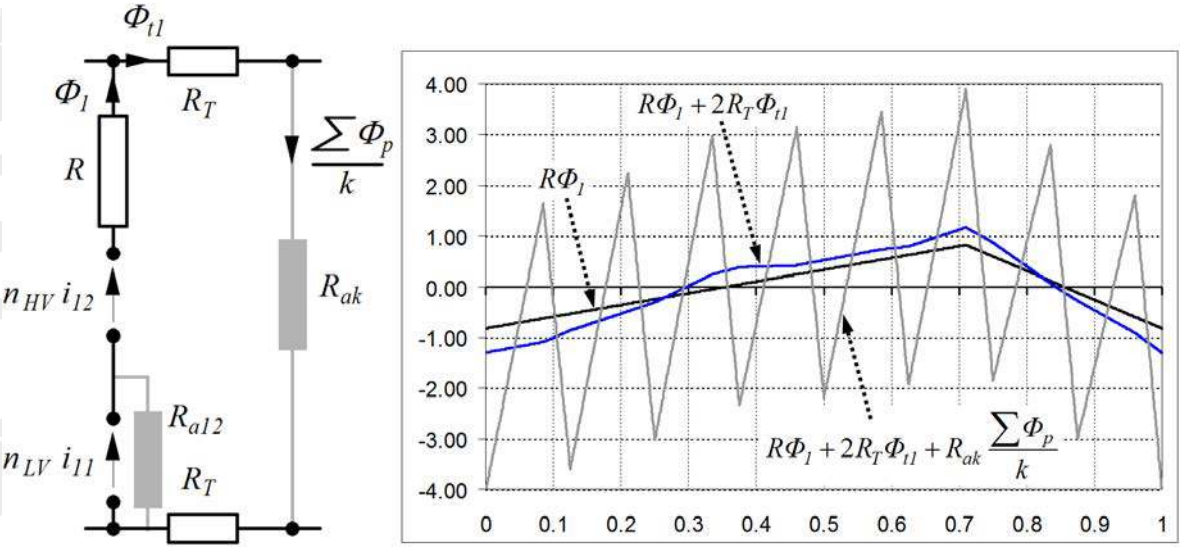
In the proposed approach, only magnetic cores without an air gap are considered, which leads to high coupling between the phases, and to low values for leakage inductors. The ratios between R_T and R_{ak} typically vary from a few hundred to one thousand. Therefore, it is necessary to use a high number of cells to provide correct filtering with the intrinsic leakage inductor L_{it}. Its value is:

$$L_{it} = n_{LV}^2/k\, R_{ak}$$

In a low voltage-high current converter, the parasitic inductors of connections can contribute to filtering (see experimental section).



a- Theoretical flux distribution in a monolithic ICT



b – Current components in ICT windings

Figure 8: Flux distribution and magnetizing current in an ICT, eight-cell example

The main characteristics of the isolated ICT buck or boost converter are unchanged with respect to the non-isolated version (introduction of the turn ratio $m = n_{HV}/n_{LV}$). Some local differences exist due to the leakage inductances between the HV and LV windings of each cell present here. As a positive effect, they enable ZVS-mode operation in the HV-to-LV power flow configuration, as can be encountered in various converters, particularly in phase-shift bridge converters, [26]. As a negative effect, they make switching management more difficult on the LV side.

C. *Buck or boost converter versus flyback converter*

The flyback converter described in [1][4] is an attractive topology using a very simple elementary cell. Nevertheless, with regard to this flyback converter, the buck or boost converter presents some interesting advantages.

The first advantage is the two-switch leg configuration on the HV side that is truly more appropriate, particularly with respect to switching conditions. The voltage stress on the switches is considerably reduced (see experimental results, section IV).

The second advantage is the better behavior of the buck or boost converter concerning the current ripple for regulated HV voltage that was emphasized by the results of section III.A. For a duty-cycle D_L included in a value range [0.3 – 0.7], the current ripple in the buck or boost converter is 3 to 1.2 times lower than in the flyback converter (Figure 5).

The third advantage of the buck or boost converter is the lower value of the turn ratio m that is required. By using the results of table 2, the relation between m_1 (buck or boost) and m_2 (buck-boost), with the same LV-HV voltages and the same duty cycle, can be established and demonstrates this fact:

$m_1 = m_2 D_L$, D_L being lower than 1.

That difference is amplified in case of large variations of the LV voltage, typically encountered with batteries. This can be shown by considering the 28V-270V example with regulation of the 270VHV bus. The voltage delivered by 28V batteries can vary approximately between V_{LMin} = 20V and V_{LMax} = 32V (full discharge in LV-to-HV operation and full charge in HV-to-LV operation). If 100V MOSFETs are considered to produce the LV stage, with a safety derating of 80%, the maximal voltage V_{SLVM} that can be applied to that MOSFET is 80V. This limit defines the first design elements of both converters, summarized in Table 4, considering an overvoltage ΔV_S (20V) across the switches during turn-off.

Flyback converter	(buck or boost) converter
$V_{SLVM} = \frac{V_{HV}}{m} + V_{LV} + \Delta V_S$ 80V with ΔV_S = 20V	$V_{SLVM} = \frac{V_{HV}}{m} + \Delta V_S$ 80V with ΔV_S = 20V
$m_{Max/Min} = \frac{V_{HV}}{V_{SLVM} - V_{LVMax/Min} - \Delta V_S}$ m_{Max} = 10, m_{Min} = 7	$m = \frac{V_{HV}}{V_{SLVM} - \Delta V_S}$ m = 4
$D_{LMax/Min} = \frac{\frac{V_{HV}}{m_{Max} V_{LVMin/Max}}}{1 + \frac{V_{HV}}{m_{Max} V_{LVMin/Max}}}$ D_{LMax} = 0.58, D_{LMin} = 0.46	$D_{LMax/Min} = 1 - \frac{mV_{LVMin/Max}}{V_{HV}}$ D_{LMax} = 0.67 D_{LMin} = 0.53

TABLE 4: DESIGN CONSIDERATION FOR TURN RATIO

The main difference is the voltage applied to the LV switches: for the buck or boost converter, it only depends on the HV voltage; for the flyback converter, it also depends on LV voltage variations that must be taken into account for the *m* choice. Lastly, the retained *m* value must be the higher (*m* = 10) value to cover the entire operating range.

In this example, the m value is 2.5 times lower in the buck or boost converter (*m* = 4). The direct consequence is an easier development of the ICT, but two additional positive effects are: the independency of the LV stage with respect to LV voltage variations, and the higher values of the duty-cycle. The latter aspect leads to lower values of RMS and switched currents in the LV stages.

IV. EXPERIMENTAL RESULTS

Experimental validation concerning the LV-to-HV power flow configuration, the most critical regarding stresses, was achieved using the multi-cell flyback converter prototype described in [4]. This included eight cells and an ICT created with separated transformers (Figure 11), arranged in a cyclic-cascade configuration described in [1]. With nominal power of 12 kW, it provided a 28-to-300V conversion. The nominal duty cycle was close to 0.5 with a transformer ratio *m = 12*.

The prototype was modified to introduce the buck or boost topology and to provide a 28V-to-270V conversion, with a minimal low voltage value around 20V.

A. Regenerative clamp

The first change concerns the LV stages. The parasitic inductors due to the connections (l_{con}) and the ICT leakage inductors (total value around 100 nH per cell) impose the introduction of switching-aid circuits, such as a regenerative snubber, active clamp and regenerative clamp [7][9]-[12][21][26]-[30]. In the flyback converter test bench, regenerative snubbers were chosen [4]. Unfortunately, they were inappropriate for the buck or boost converter. Therefore, a regenerative clamp, constituted of an 80V-to-28V buck converter, replaces the latter (Figure 11). In a final implementation, it should be integrated on the LV side. That clamp limits the voltage across the LV switches during turn-off and returns a part of the stored inductor energy (approximately 200W) toward the LV source (see the oscillogram in Figure 9).

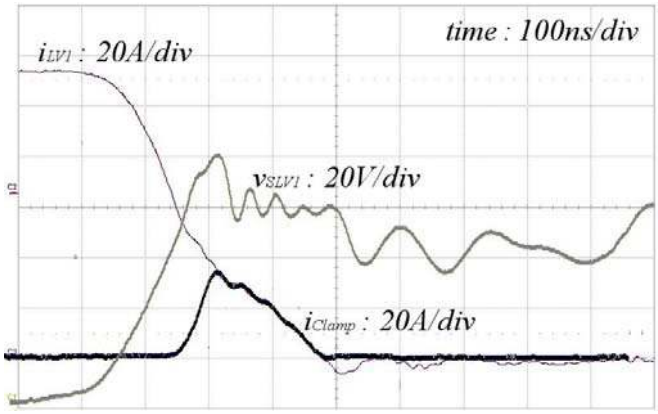


Figure 9: Operation of regenerative clamp at turn-off

B. ICT

The second modification is the *m* reduction from 12 in the previous flyback to 4, as shown in Table 4. This was achieved by modifying the turn number lof the ICT HV winding.

This ICT is realized with separated planar transformers. A design tool based on methods described in [31][32] was used to optimize the components. The core is an EI 58 planar N97. The main sizing parameters are given in Table 5:

P = 10 kW/8	F_{sw} = 50 kHz	ΔB_M = 0.19 T	J_{RMS} =7 A/mm²
P_c = 2.7 W	P_w = 8.47 W	A_c = 300 mm²	Weight: 1500g
Cell magnetizing inductor L_m, 5 µH		Cell leakage inductor, 20 nH	
1 LV layer, 19mm x 0.5mm		4 HV layers, 19mm x 0.05mm	

ΔB_M , maximal induction in the core, J_{RMS}, current density in conductors
P_c, core losses, P_w, conductor losses, A_c, core area

TABLE 5 : TRANSFORMER CHARACTERISTICS

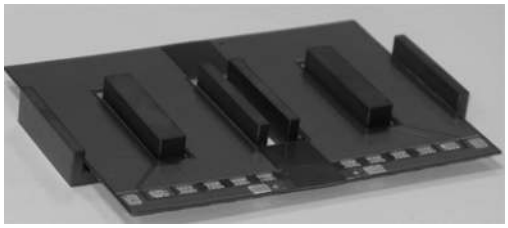
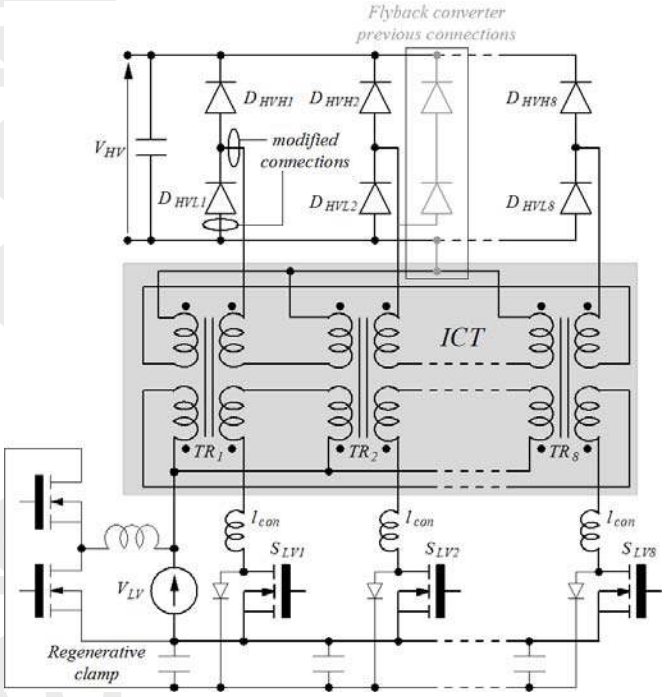


Figure 10: HV winding layer

This figure shows the HV winding layer based on Kapton-copper PCB technology.



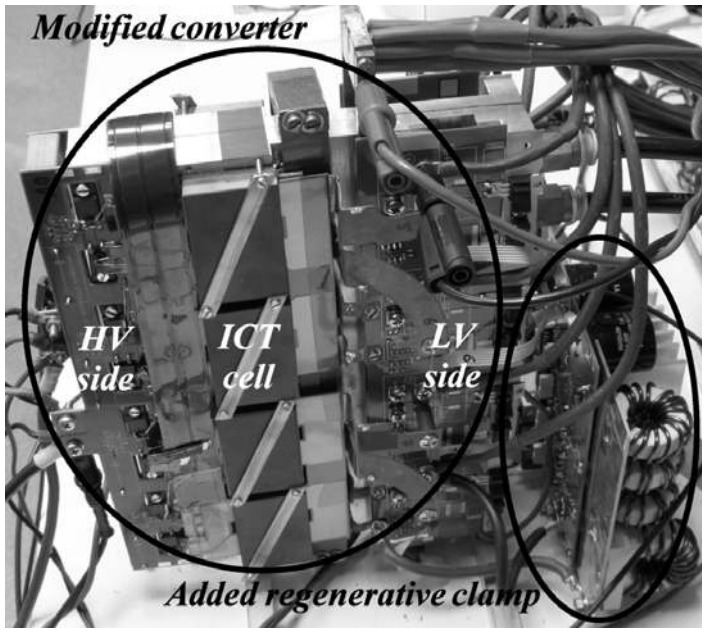
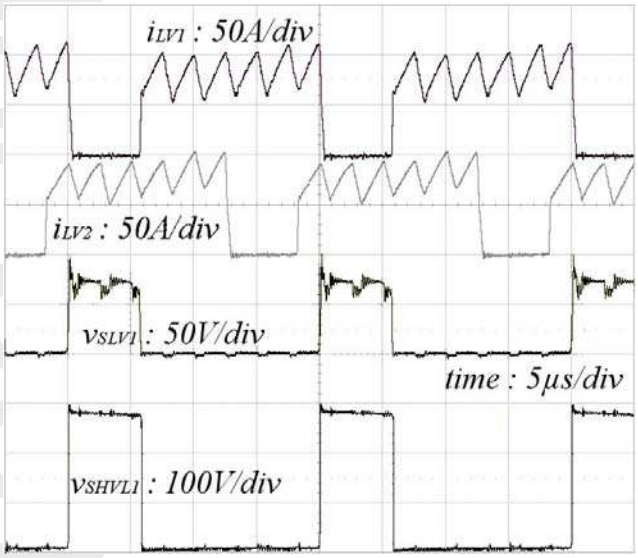
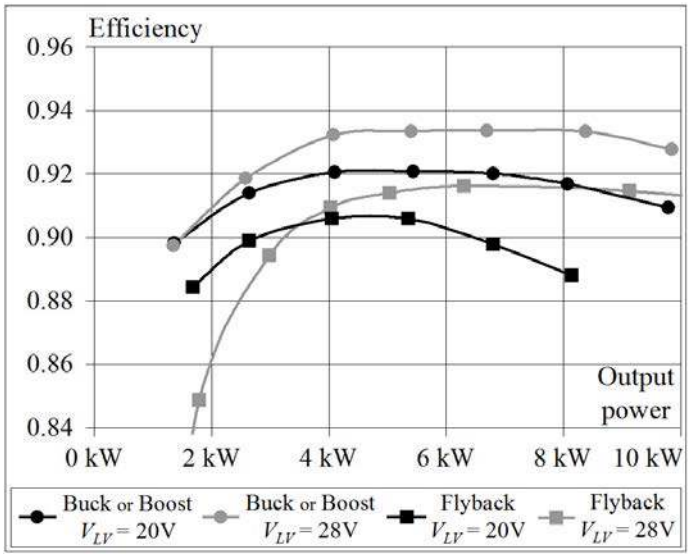


Figure 11: Diagram and view of the modified prototype



a) Experimental waveforms (270V-30A-8.1kW)



b) Efficiency of Buck or Boost converter and of flyback converter

Figure 12: Experimental results

The planar core technology leads to low value of leakage inductor. As evoked is section III.B, in the present case the connection inductors (around 70 nH) contributes to limit the current maximal ripple to 50 A.

C. *HV rectifier*

The last modification is necessary to build the diode legs on the HV side. In the flyback converter, two 600V-diodes were connected serially on HV side as shown in the grey section of Figure 11. In the modified configuration, they are placed on the DC bus and their middle point is connected to the ICT.

D. *Current balance*

The current unbalance problem can be encountered in any multi-cell parallel converter. In industrial applications, it is necessary to introduce current balance loops, as in VRM modules.

Considering the aim of the present test bench (validation of the power stage capability) and its complexity, the possibility to operate in an open loop was evaluated and significant unbalance robustness was demonstrated. Indeed, an estimation of the authorized current unbalance to avoid core saturation is possible.

If an unbalance exists on the average currents of two adjacent cells, this creates a DC magnetizing current I_{unbal} in the considered cell transformer. On the LV side, the DC induction induced by this DC current can be estimated by the following expression:

$$B_{DC} = L_m I_{unbal} / n_{LV} A_c$$

With the maximal induction in normal operation being 0.19T and the saturation induction of the N97 material being 0.4T, the allowable B_{DC} value is close to 0.2T. This leads to an I_{unbal} value of 12 A, more than 15% of the average normal cell current. Due to good mechanical symmetry of the test bench and the digital synthesis of the PWM, the observed unbalances remain lower than 3-4 A. Therefore, open loop operations can be provided and experimental results confirm that fact.

Experimental results are given in Figure 12. Figure 12-a shows electrical waveforms, the currents in both LV cells 1 and 2, the voltage across the switch S_{LV1} and the voltage across the diode *HVL1*. The current forms are typical of the ICT converter with the kF_{sw} current ripple. The current steps existing in the theoretical waveforms of Figure 4 cannot be observed here, due to the connection inductors l_{con}, that contribute to current ripple limitation in a different operating mode with respect to that of ICT internal inductors. Therefore, the steps are masked by this mechanism but the experimental forms remains very close to the theoretical forms.

The experimental voltage form across the diode *HVL1* confirms the interest of the leg-cell on the LV side. This form is very soft without any recovery overvoltage, suggesting low recovery losses. In addition, the use of 400V diodes on the 270V DC bus is possible and leads to the minimization of on-state losses.

E. Loss estimation

Figure 12-b shows the buck or boost converter efficiency compared to that of the flyback converter described in [4]. The improvement is significant, despite higher switching losses (the regenerative clamp does not aid the turn-off), and the undersizing of the HV windings, the HV turn number having been reduced without increasing the conductor section.

Detailed loss measurements cannot be obtained from the experimental setup. Theoretical estimations have been made from design tools and device data sheets on two operating points. Therefore, they are necessarily inaccurate but do give tendencies on loss distribution. They are summarized below in Table 6

	MOSFET	Diodes	Snubber or Clamp	ICT	Conn*	Total
1 - Flyback 20 V – 9.55 kW	Experimental					1247 W
2 - Buck or boost 20 V – 9.8 k W	Experimental					974 W
3 - Flyback 20 V – 10 kW	220 W	162 W	280 W Snubber	120 W	400 W	1182 W
4 - Buck or boost 20 V - 10k W	330 W	130 W	10 W clamp	100 W	400 W	970 W
5 - Flyback 20 V – 10 kW	*420 W*	*162 W*	*20 W Clamp*	*120 W*	*400 W*	*1122 W*

* Connections

TABLE 6 : EXPERIMENTAL AND ESTIMATED LOSSES

The two first lines give the experimental results of two operating points close to 10 kW. Lines 3 and 4 give estimations for 10 kW output power and can be compared to the previous lines. With the two converters using two different auxiliary networks (snubber or clamp), line 5 gives an estimation of flyback converter losses if a clamp was introduced. In any case, the lower RMS and switched current values make the buck-or boost converter more efficient.

Therefore, the ICT buck or boost converter can be considered very promising. Technological optimization concerning connections and turn-off aid could lead to high efficiency values.

V. CONCLUSION

In the high-power/low voltage configuration considered here, converter interleaving is an interesting option. It distributes the electrical stresses in modular cells that are easier to design, and leads to a decrease in filter sizes due to the equivalent frequency increase.

The interleaving principle can be applied to most converter topologies. The ICT buck or boost converter presented here is related to the isolated ICT converter family from which a unidirectional flyback converter was previously presented by the authors. The main advantage of the concept is the removal of discrete inductors, and, as a consequence, facilitating the implementation of integrated magnetic strategy.

The present converter is an attractive option to achieve a high step-up power conversion, the LV-to-HV power flow configuration being the more critical. In that mode, its boost behavior enables the use of a low transformer ratio, and therefore makes it possible to design efficient ICTs. Leg cells are the optimal solution for minimizing switch stresses on the HV side. In addition, high duty cycle operations in LV-to-HV power flow configuration are allowed and are favorable to the minimization of switch loss.

The experimental results obtained on a 10kW test bench in the LV-to-HV power flow configuration confirm the multi-cell ICT buck or boost converter as a good candidate for designing interconnection stages between low- and high-voltage sources.

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Appendix

Current ripple calculations

The example of current ripple in buck or boost converter is retained to illustrate the calculation method. The ripple current results from the interleaved voltage application (amplitude V_{HV}/k, frequency kF_{sw}) to the ICT output inductor L_{it}, as shown on Figure 13.

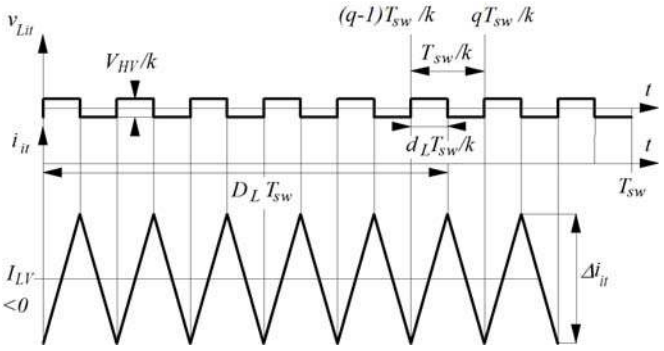

Figure 13: Waveforms for the current ripple calculation

Due to interleaving, the current ripple evolution has a periodicity of T_{sw}/k. Therefore, a local duty cycle d_L can be defined as follows:

$$\frac{d_L}{k} = D_L - \frac{q-1}{k} \quad \text{With } 1 \le q \le k-1$$

$$d_L = kD_L - q + 1$$

The periodic evolution of the ripple current depends on the local duty cycle as:

$$\Delta i_{it} = [1 - d_L][d_L]\frac{V_{HV}}{k^2 L_{it} F_{sw}}$$

Finally: $$\Delta i_{it} = [kD_L - q + 1][q - kD_L]\frac{V_{HV}}{k^2 L_{it} F_{sw}}$$