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# Evaluation of $V_{ce}$ Monitoring as a Real-Time Method to Estimate Aging of Bond Wire-IGBT Modules Stressed by Power Cycling

Vanessa Smet, François Forest, Jean-Jacques Huselstein, Amgad Rashed, and Frédéric Richardeau

*Abstract*—The supervision of semiconductor power devices in operation demonstrates an obvious interest to improve the operating safety of electronic power converters used in critical applications. Unfortunately, this is a significant challenge due to the variability of stress conditions on the one hand and to the difficulty to implement accurate measurement systems in power stages on the other. Using  $V_{CE}$  measurement as a real-time supervision method is evaluated here by using aging test results obtained on insulated gate bipolar transistor (IGBT) modules stressed by power cycling. These results are related to the aging of bond wires and metallization, on the top part of the module. Results were obtained in original test benches whose characteristics are overviewed briefly in the first part of this paper, along with a description of test conditions. The second part presents selected results extracted from a larger work and focusing on the  $V_{CE}$  evolution with respect to degradations of the module's top part. Their analysis highlights the potential of  $V_{CE}$  measurement. The last part proposes the principle of a specific system able to achieve real-time  $V_{CE}$  supervision in the test benches in operation.

*Keywords*—Bond wire aging, IGBT modules, power cycling, real-time monitoring.

## I. INTRODUCTION

SEMICONDUCTOR power devices are the key part of electronic power systems. Therefore, the knowledge concerning the degradation and failure modes that can be sustained by these devices is critical with respect to applications requiring a high level of reliability [1]–[3]. One interesting repercussion of this knowledge is the identification of supervision methods [4]–[6] in addition to theoretical lifetime models. Indeed, an efficient health monitoring is an effective way to anticipate failure occurrences, whatever the stress conditions and their evolution may be, and to obtain safe operations for humans and/or high availability for systems.

Such a strategy can concern all the components and subsystems. For example, significant research has been, and continues to be, conducted in that field for converters and drives [7]–[13]. In all cases, the health monitoring is not particularly easy to carry out, particularly for power semiconductor devices [4].

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Some research has long been associated with detection units that allow an elementary form of supervision. This can be found in intelligent power modules [14] and smart power devices [15], but more generally in the modern gate drivers.

For example, measuring die temperature is commonly introduced to keep operations with the safe thermal area [16].  $V_{CE}$  measurement is another solution frequently used in the design of the IGBT gate drivers to detect an overload or a short circuit [17], [18]. These examples are representative of an industrial state of the art that only considers instantaneous stress detections. They are not able to provide predictive information on the aging which constitutes the major point of interest of this paper.

In numerous applications, power devices suffered from thermomechanical stresses resulting from power cycling and which induce aging mechanisms [19]–[26]. In IGBT power modules, all components are concerned, as wire bonds are the most common technology for implementing top face interconnections. The aim of this paper is to evaluate the  $V_{CE}$  parameter as an aging indicator of the bond wires in a power-cycling context and, then, to propose a real-time measurement technique that could be applied to power converters in operation. This last point constitutes the main originality of this paper regarding references cited earlier.

The presentation is based on the results obtained during a larger project focused on aging and failure mechanisms in IGBT modules. Twenty IGBT modules of 600 V and 200 A were tested by applying different protocols covering a wide range of thermal stresses. Throughout the aging tests, the junction-to-case thermal resistance and the  $V_{CE}$  voltage of the dies were measured regularly to detect possible changes and estimate the aging state of the devices.

The first section provides a brief overview of the main features of the experimental test bench with a focus on the module's thermal operating conditions. The second section presents a summary of the more significant results with respect to  $V_{CE}$  supervision. The third section analyzes these results to emphasize the pertinence of  $V_{CE}$  monitoring: It enables the effective evaluation of the top face state of the modules, on condition that sufficiently accurate and reproducible measurements are collected. Lastly, the possibility to introduce

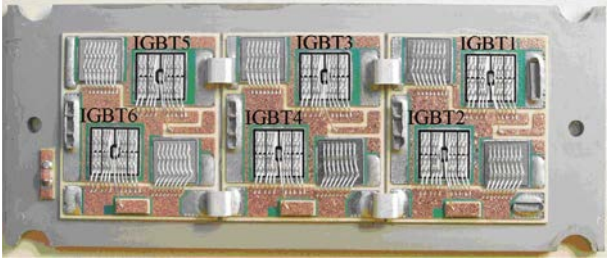


Fig. 1. Interior view of the tested module.

such monitoring in operating electronic power converters is discussed, and an acquisition board to carrying out this function in the test bench is described.

## II. AGING TEST BENCH AND MONITORING STAGES

### A. Tested Devices

The tested devices are IGBT modules including three inverter legs mounted on three independent direct bonded copper (DBC) substrates [27] and using 600-V-200-A trench gate chips (see Fig. 1). The DBC technology is the most currently used in power IGBT module.

### B. Power Section of the Test Benches

The samples are aged in a test bench operating in switching conditions (pulse width modulation (PWM) mode control, as shown in Fig. 2).

This test bench uses two of the module's DBCs to constitute a PWM bridge that operates as a drive inverter with respect to the electrical stresses applied to IGBT dies (PWM switching, sinusoidal modulation of the load current).

Therefore, the dies are placed in conditions very similar to real-world conditions. A periodic load supply provides the power cycling.

### C. Thermal Distribution—Use of the Central DBC

The test bench stresses only two of the three DBCs implemented in the module. To minimize the dispersion of average chip temperatures, the use of side DBCs is preferred.

Thermal finite element analysis (FEA) simulations and thermal analysis in operation (using an infrared (IR) camera) were performed to verify the thermal cartography and correct temperature distribution in the four IGBT dies being tested. A module was especially prepared (see Fig. 3) to enable this IR thermal analysis (dissolving of silicone gel, making connection modifications and painting the DBC top black).

FEA simulations are performed in 3-D using COMSOL software. Fig. 4 shows the proper matching between simulation and measurement. The values added on the graphs are the average chip temperatures on the top of the thermal cycle.

These results confirm that the four IGBT dies operate with similar thermal conditions. In any case, it is impossible to strictly impose the same thermal stress to the dies, due to the thermal asymmetry of the module as well as the loss dispersion in the dies.

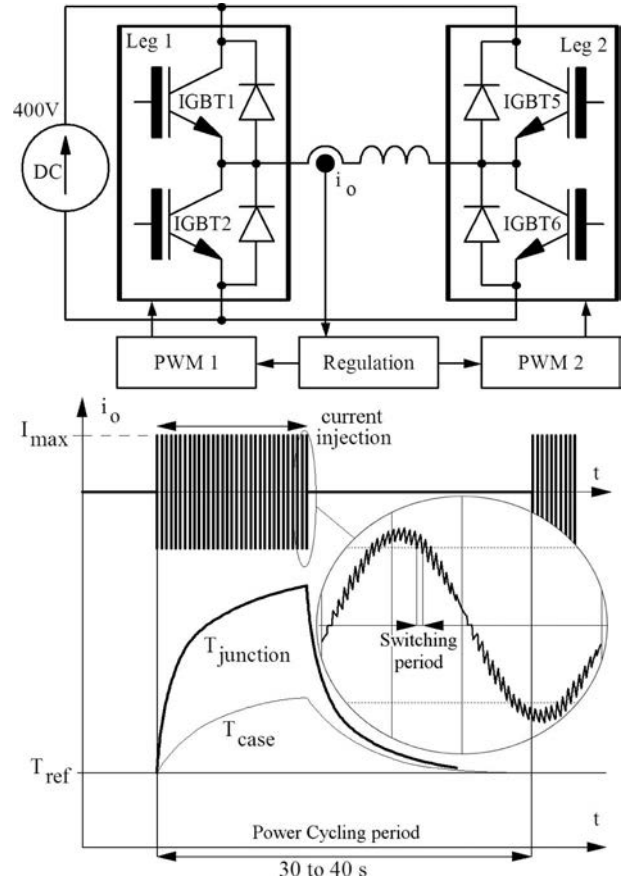


Fig. 2. PWM test bench.

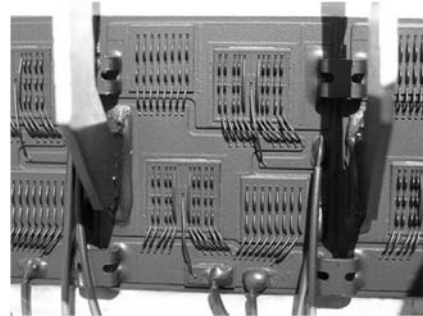


Fig. 3. Sample prepared for thermal measurement by IR camera.

In Fig. 5, the temperature profiles on the dies are provided for the same configuration. Once again, strong correlation between simulation and measurement is observed.

Die temperature is not homogeneous, which is a classic result, but the temperature die on the gate pad, placed on the die center, is close to the average temperature. This fact justifies the measurement technique described in Section II-D.

As shown previously, the test configuration causes aging only in the side DBCs. When a die reaches an aging state defined by a critical value of one of the indicators (see Section II-E), the test of the corresponding leg (and DBC) is stopped. The second side leg can then be tested by using the central DBC, unstressed until that time. This option has been applied to the majority of the samples presented hereafter.

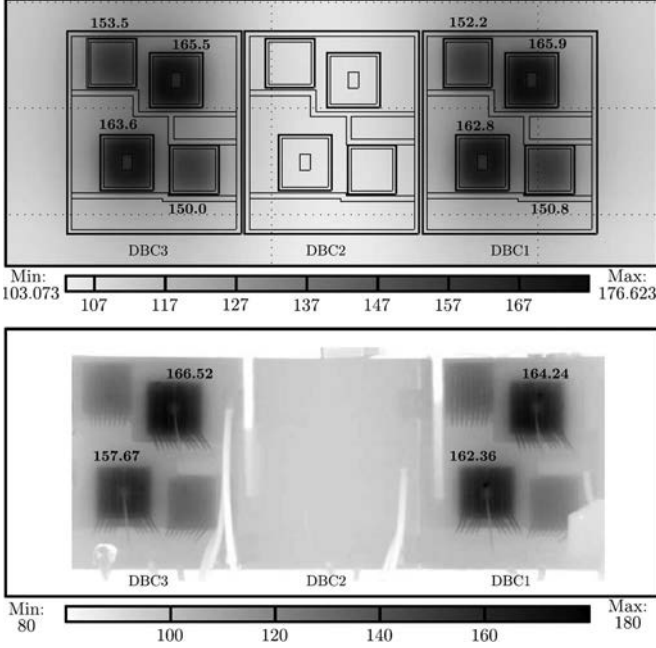


Fig. 4. (Top) FEA and (bottom) experimental thermal cartographies.

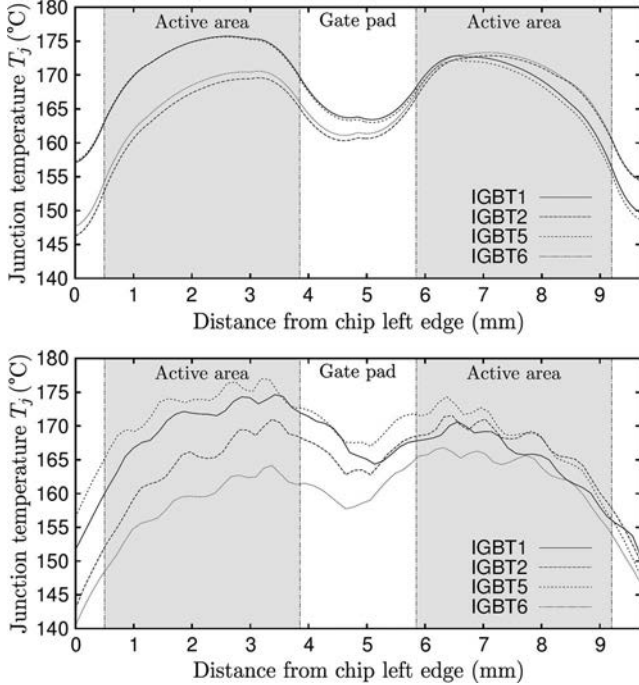


Fig. 5. Temperature distribution along the die surface given by (top) FEA and (bottom) IR camera.

Thermal test conditions are changed slightly (see FEA simulations in Fig. 6), but this test extension makes it possible to generate twice the number of aged dies and allows additional observations (see Section IV-A).

#### D. Control Part

The temperature measurements are critical for proper test progression. Two platinum sensors placed on the case under the side DBCs and thermo-optical sensors, positioned on the IGBT

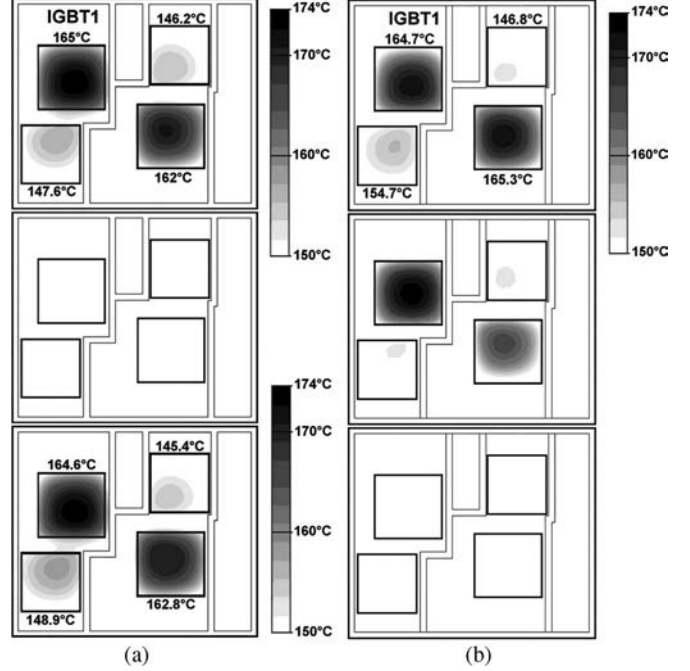


Fig. 6. FEA thermal cartographies in both tests.

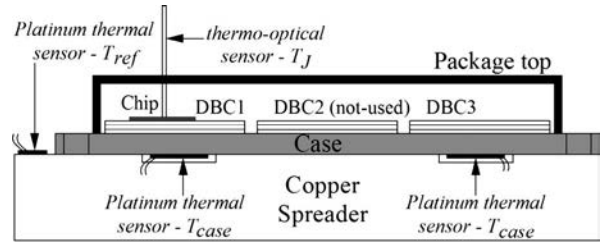


Fig. 7. Thermal instrumentation of a module in PWM test bench.

die center, give respectively case and junction temperatures (see Fig. 7).

The test bench supervision system includes two parts. The first is a group of field programmable gate array (FPGA) boards dedicated to PWM control and to protection management for power stages. The second is a group of PC and acquisition boards that manage the power cycling, handle the regulation, and acquire and store all the test data (namely, temperatures, voltages, and currents). A more detailed description can be found in [24].

#### E. Monitoring Conditions

Throughout the aging tests, four parameters are measured regularly: junction-to-case thermal resistance  $R_{TH}$ , voltage  $V_{CE0}$  ( $V_{CE}$  value under constant current and temperature conditions), gate voltage threshold, and leakage current. The measurement period varies from 1000 to 5000 cycles, chosen with respect to protocol harshness.

These measurements were not automated because of the experimental difficulty (see Section IV-B1). To proceed, test benches are stopped, and the main voltage source is disconnected. Special measurement boards are then temporarily inserted.

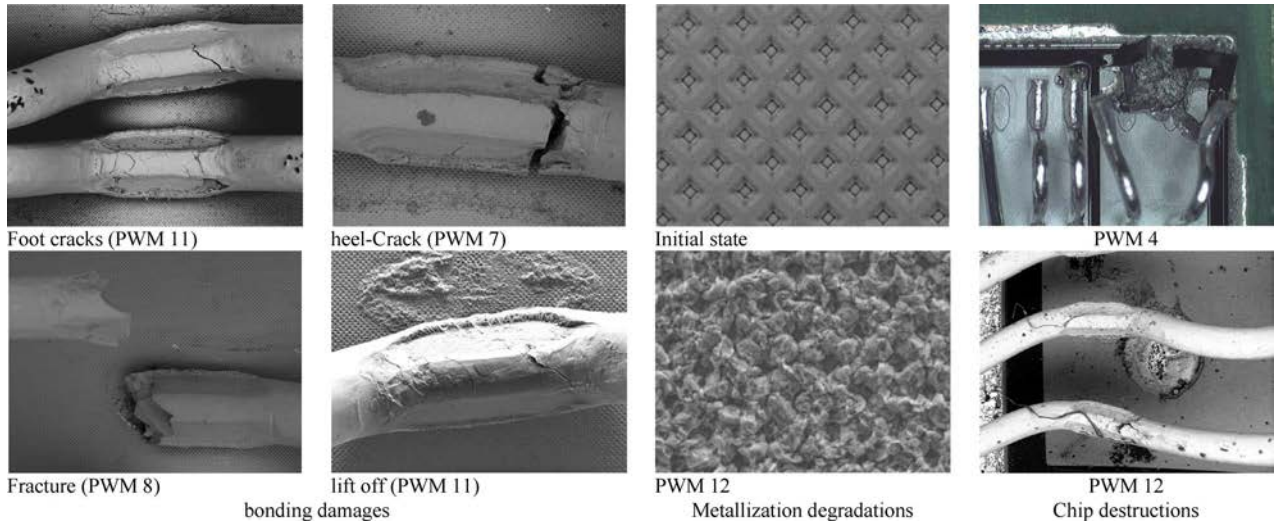


Fig. 8. Examples of degradations.

### III. EXPERIMENTAL RESULTS AND ANALYSIS

In the overall work, presented in another publication [26], five protocols were used with a gradation of thermal stresses. The main degradations are localized on the top part of the modules and first concern the wire bonds. Fig. 8 gives some examples of aging consequences.

The devices are considered degraded when  $V_{CEo}$  has risen by 2%–3% and  $R_{TH}$  has risen by 10%. These criteria values were chosen lower than the usual values [28] in order to reduce test duration.

These parameters are regularly measured, in the same current and temperature conditions (100 A and 125 °C for  $V_{CEo}$ ), in order to detect an eventual evolution (sign of wire bond or metallization degradations) at the same operating point. The threshold voltage and the collector leakage current were also measured but have never changed in any tests. In some cases, aging was interrupted by a chip failure. Lastly, in most of the cases, only the parameter  $V_{CEo}$  has changed and reached the degradation criteria.

Tables I and II show a part of the results, limited to the three protocols that are the most significant in the context of this paper. The cartographies give the degradation distribution of the wire bonds. In accordance with the intent of this paper, the associated curves show the  $V_{CEo}$  voltage evolution versus the number of cycles for each sample. This is the principle data used in the discussion in the next section. The other parameters are not considered here.

Fig. 9 shows the distribution of each degradation type considering the three protocols and the four IGBT dies. The percentage of degradations is an average value calculated for all the samples in a given protocol and based on SEM analysis.

The bonded area corresponds to the area where the bond foot is connected to the metallization on the chip top. The “total bonded area” represents the total number of bond feet per chip.

“Heel crack” is a classical cracking mechanism that occurs at the heel of a wire bond and due to a flexure fatigue caused by thermal cycling. The term “foot crack” refers to cracks observed

on the bond foot itself, distributed throughout the bond foot upper surface, giving it a “scaly” aspect. Their origin can be attributed to predamage induced during the wire-bonding operation.

Liftoff and foot-crack mechanisms depend mainly on temperature cycling amplitude. Conversely, the proportion of heel cracks does not increase with the harshness of the temperature cycles because this mechanism occurs over a long time frame. In the harshest test conditions, the chip gets destroyed before the wire-bond fatigue could induce much damage.

Heel crack and liftoff are the most prejudicial types of damage with respect to the  $V_{CEo}$  increase. Heel crack can lead to the disconnection of the wire-bond line part following the crack. In the worst case, the entire wire-bond line may be lost. One liftoff cannot cause such an effect, but if they are numerous, the result on the  $V_{CEo}$  increase is similar.

Therefore, with the percentage of heel-crack and/or liftoff occurrences being significant in the three protocols, a change of  $V_{CEo}$  voltage was detected in all the samples.

This confirms the relevance of this parameter as an effective indicator of the wire-bond aging and, more generally, of the top-part aging. This topic is further developed in the next section.

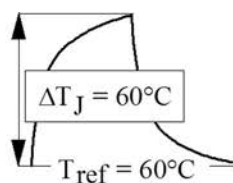
### IV. $V_{CEo}$ MONITORING

#### A. Result Analysis

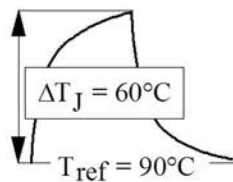
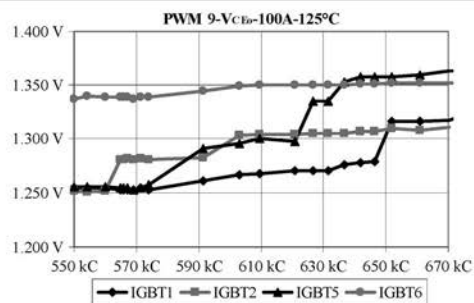
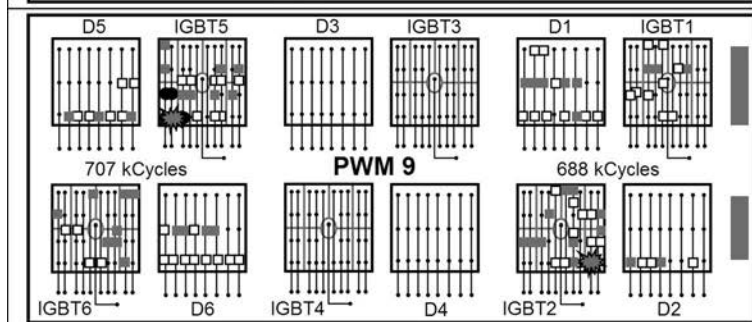
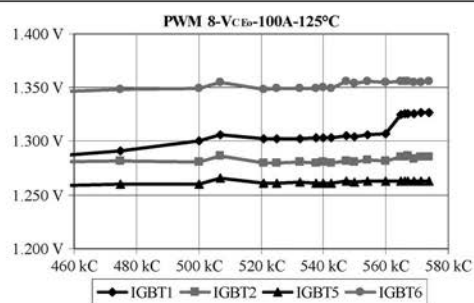
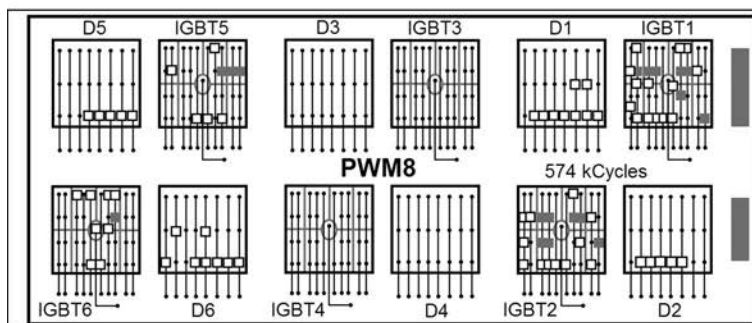
1) *Robustness of the Indicator  $V_{CEo}$* : Three approaches were taken to conclude aging tests.

- 1) The test stop for PWM 2 and PWM 8 is a consequence of a  $V_{CEo}$  increasing by 2% above the initial value.
- 2) PWM 9 and PWM 11, after a detection of a  $V_{CEo}$  increasing on a first side DBC, were deliberately aged until a failure occurred on each side DBC, by using the central DBC for the second one.
- 3) PWM 14 and PWM 15 first suffered from a failure on one of the side DBCs before any detection of a parameter evolution. In both cases, the second side DBC was aged until  $V_{CEo}$  evolution using the central DBC.

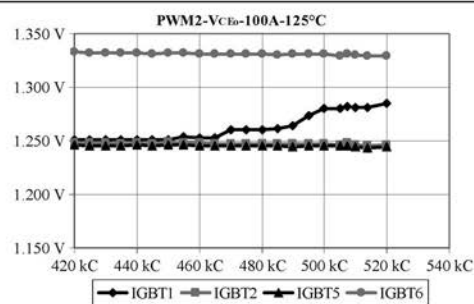
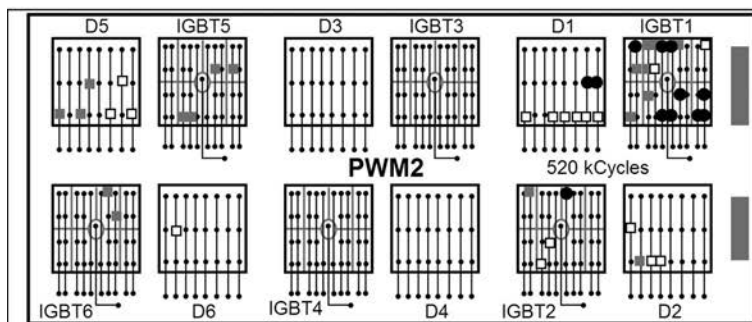
TABLE I  
TEST RESULTS FOR PROTOCOLS 2-1 AND 1-1



Protocol 2-1



Protocol 1-1



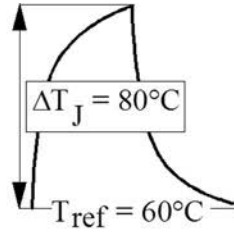
● lift off   ■ Foot-crack   □ Heel-crack / fracture   ✶ Chip destruction

In most of the cases, particularly for the less harsh protocols (protocols 2-1 and 1-1), the  $V_{CE0}$  voltage is an effective aging indicator with a measurement period around 2000 or 3000 cycles.

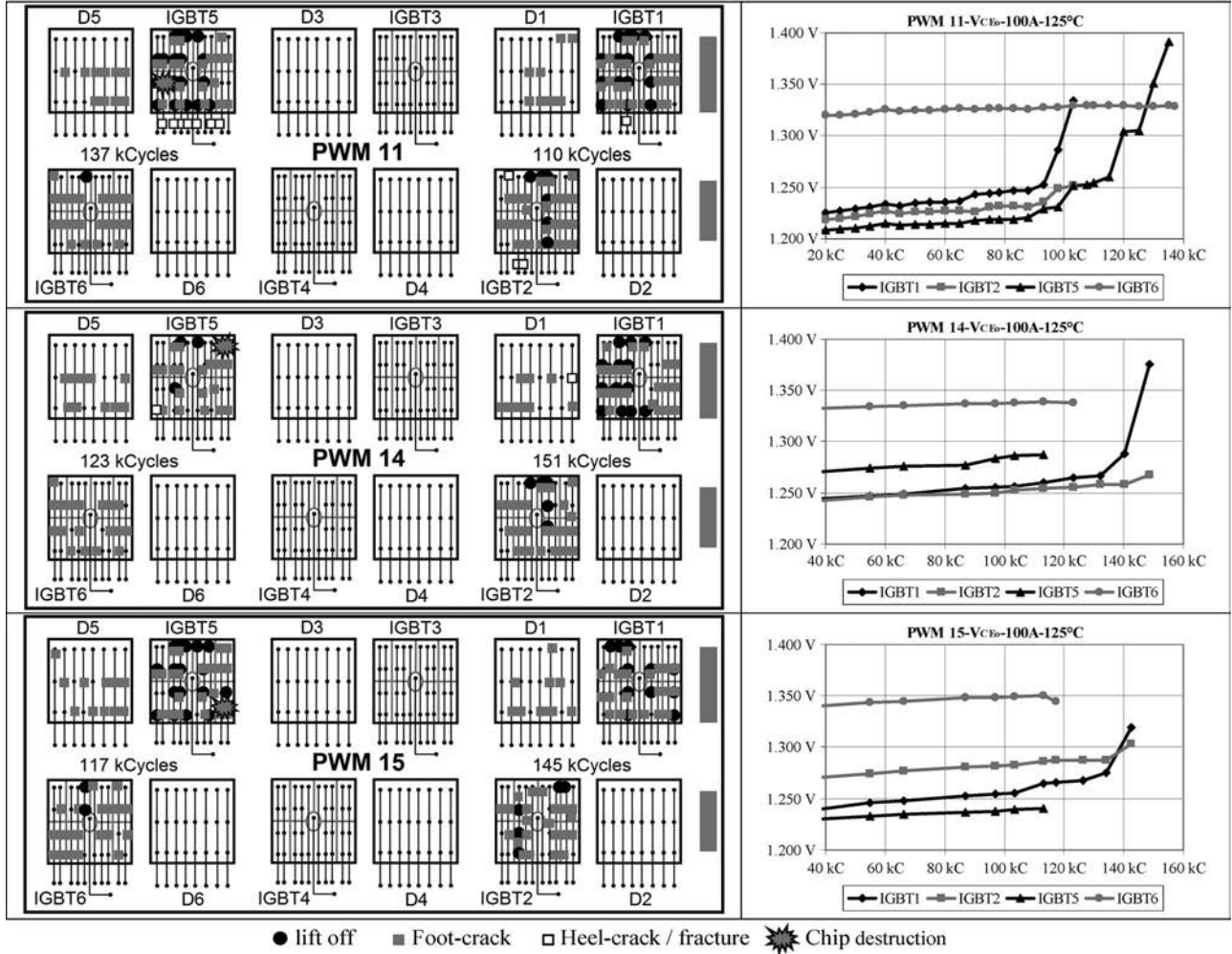
In the case of protocol 2-2, the harshest, any  $V_{CE0}$  increase preceded the failure of the first side DBC. Unfortunately, the supervision period was enlarged for those samples (5000 cy-

cles), due to the project timing, even when the curves show a faster  $V_{CE0}$  increase, characteristic of faster aging imposed by that protocol. A lower value of the measurement period, as thus chosen for PWM 11, would most likely have led to a detection of  $V_{CE0}$  increase. These observations lead to a positive statement regarding  $V_{CE0}$  measurement used as a method to provide health monitoring on the top part of IGBT modules. In

TABLE II  
TEST RESULTS FOR PROTOCOL 2-2



Protocol 2-2



case of harsh power cycling, a low period for the characterization step is necessary in order to detect fast increases. This could be achieved by an automated “online” measurement (see Section IV-B).

2) *Estimated and Real Lifetime*: If used, the  $V_{CE0}$  monitoring must provide information sufficiently in advance of a potential failure. Therefore, the difference between the estimated lifetime given by the indicator and the real lifetime, that would be reached by destruction if nothing is done, must always exist and be significant. The results obtained on samples PWM 9 and PWM 11 provide direct information on this feature.

For PWM 9, the voltage  $V_{CE0}$  varied significantly ( $> 3\%$ ) across one of the hotter dies ( $IGBT_1$  or  $IGBT_5$ ) on both

DBC around 600 kCycles (see Table I). Nevertheless, the aging test was extended to reach failure, which finally occurred at 688 kCycles for the first DBC and 707 kCycles for the second DBC. On the one hand, a very similar lifetime is observed for both DBCs, and on the other hand, the delay between the detection of  $V_{CE0}$  variation and the failure is close to 100 kCycles. This delay is significant with respect to the safety but represents only 14% of the lifetime. Detection can be then not considered as premature.

For PWM 11, a  $V_{CE0}$  variation was detected around 100 kCycles for the first DBC ( $IGBT_1$ ). Its aging was interrupted, but the test continued on the second DBC by using the central DBC. Then, the  $V_{CE0}$  voltage across IGBT 1 varied from 120 kCycles, and the die was destroyed at 135 kCycles. In

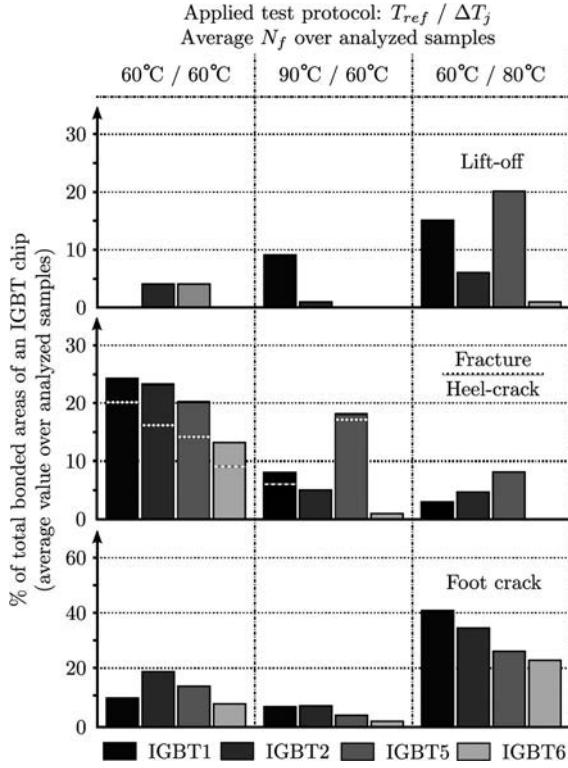


Fig. 9. Bond wire damage distribution by protocol.

this case, the delay between detection and failure is 15 kCycles, which represents 11% of the lifetime.

These two examples confirm that  $V_{CEo}$  voltage is an effective indicator to anticipate failures due to wire-bond aging and that it can be introduced into predictive maintenance strategy.

## B. $V_{CEo}$ Real-Time Monitoring

1) *Problem*: The previous section highlighted the interest of an “online” measurement of  $V_{CEo}$  to supervise the aging. This could be very useful in the test benches as described here and also in industrial operating converters to handle a real-time health monitoring of the semiconductor devices.

Unfortunately, such measurement is very critical. Indeed, it must be extremely accurate (uncertainty lower than 1%) and carried out under strictly controlled temperature and current conditions (125 °C and 100 A in the present tests). A major difficulty is the insertion of instrumentation devices [26], [29] able to provide that accuracy in power stages supplied by high voltage and in which the currents and temperatures vary periodically. In addition, in case of operational converters, the measurement must be performed without modifying their operating characteristics.

The next section presents a strategy that provides such a measurement, but it will be only available for the test bench described earlier. In this case, it is possible to modify the PWM control to insert the measurement process, with the changes introduced in the time scale of some switching periods having no significant effect on the thermal stresses generated by the test bench.

2) *Proposal of a Real-Time Measurement Strategy*: Repetitive  $V_{CEo}$  measurement must be made under constant tempera-

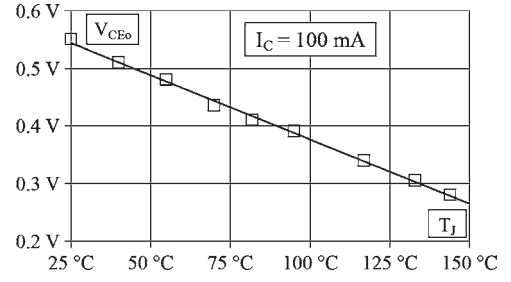


Fig. 10. Indirect temperature measurement via  $V_{CEo}$ .

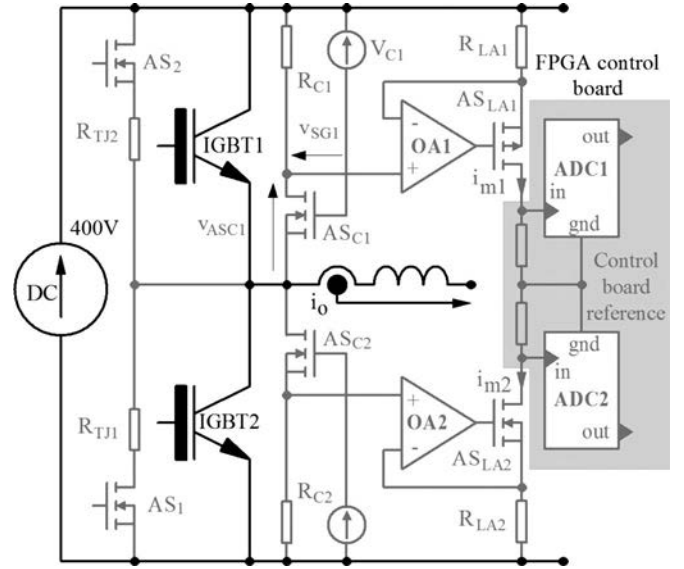


Fig. 11.  $V_{CEo}$  measurement scheme.

ture and current conditions. The first choice for the strategy is to carry out an indirect temperature measurement via  $V_{CEo}$  [3], [19]. This requires a preliminary characterization of each die as shown in Fig. 10, which is easy to achieve. It must be performed under a low current level in order to eliminate the voltage drop due to the connections.

On that basis, the proposed instrumentation structure is shown in Fig. 11. To simplify the schematic, parallel diodes are not drawn. This structure uses two stages, one for the high side IGBT and one for the low side IGBT. Each stage includes a  $V_{CEo}$  clamp ( $AS_{C1}$ ,  $R_{C1}$  and  $AS_{C2}$ ,  $R_{C2}$ ) to limit the measured voltage when IGBTs are in OFF state, a 100-mA current sink for the indirect temperature measurement ( $AS_1$ ,  $R_{TJ1}$  and  $AS_2$ ,  $R_{TJ2}$ ), and a voltage-to-current converter (line amplifiers OA1,  $AS_{LA1}$ ,  $R_{LA1}$ , and OA2,  $AS_{LA2}$ ,  $R_{LA2}$ ). All these devices are implemented near the IGBT power module. Another identical measurement board is associated with IGBTs 5 and 6.

The different auxiliary MOSFETs have to support the high dc voltage but conduct very low currents (100 mA or less) with respect to the power IGBT.

*Voltage clamp*: The principle can be deduced (example of the high stage) from the following equations:

$$V_{RC1} = V_{CEo} - v_{ASC1} = V_{C1} - V_{SG1} \quad (1)$$

$$V_{SG1} = V_{C1} - V_{CEo} + v_{ASC1}. \quad (2)$$



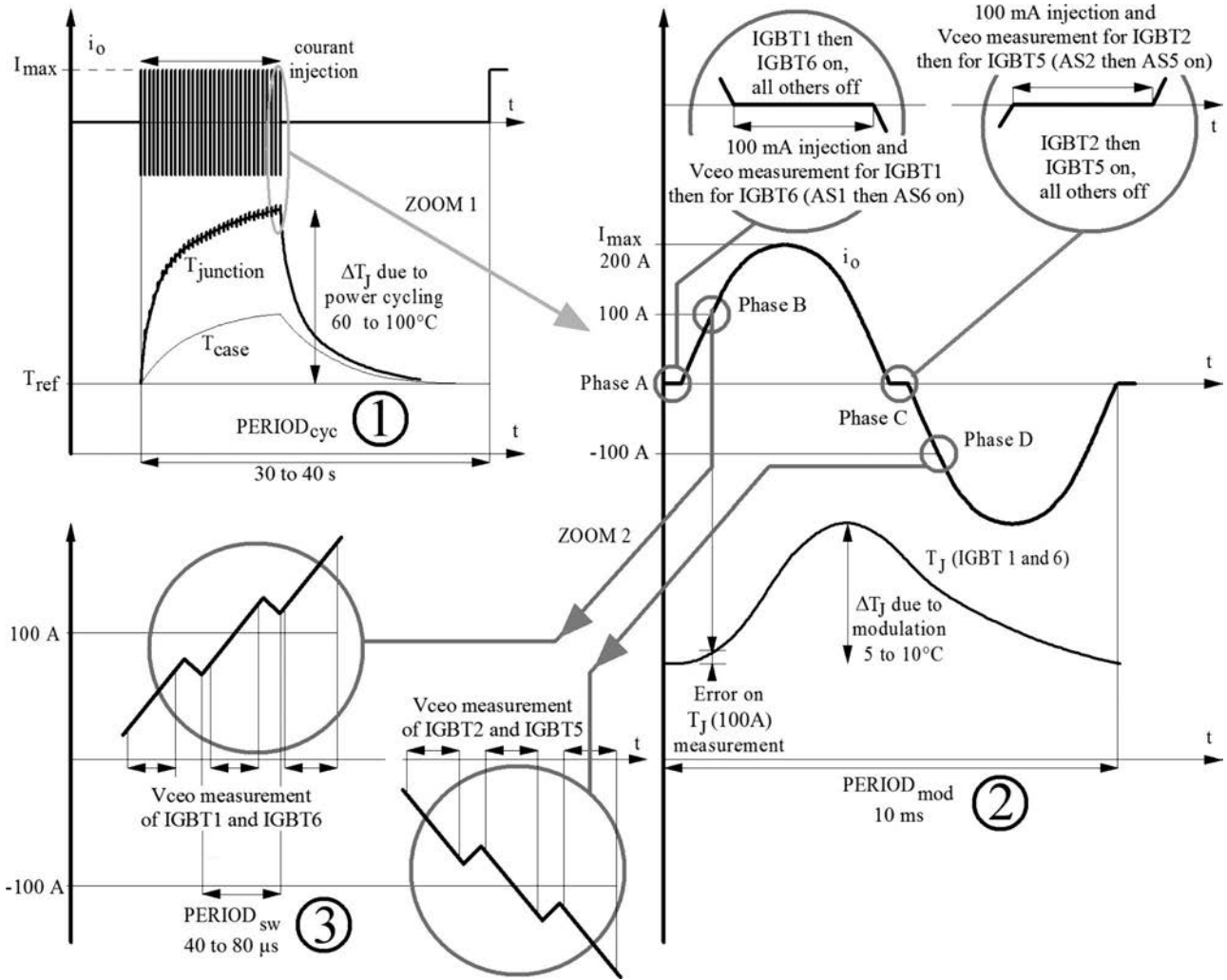


Fig. 12. Chronogram of  $V_{CEo}$  measurements.

If  $AS_{C1}$  is in the ON state, the voltage  $V_{RC1}$  is equal to  $V_{CEo}$  (1), with the  $AS_{C1} R_{DSON}$  being widely lower than  $R_{C1}$ .  $AS_{C1}$  is in the ON state if  $V_{C1} - V_{CEo} + v_{ASC1} \leq V_{SGTH1}$  (2), with  $V_{SGTH1}$  being the threshold voltage of  $AS_{C1}$ . When  $V_{CEo}$  increases then reaches the value  $V_{C1} - V_{SGTH1}$ ,  $AS_{C1}$  begins to operate in linear mode, the clamping mode is active, and the voltage clamp value is close to  $V_{C1} - V_{SGTH1}$  (10 V in the test bench).

**100-mA current sink:** With the 400-V dc voltage being provided by an regulated voltage power supply, the 100-mA current is simply determined by fixing the value of resistors  $R_{TJ1}$  and  $R_{TJ2}$  (400 k). The current injection in IGBT 1 or 2 is realized by turning on respectively  $AS_1$  or  $AS_2$ .

**400-V voltage-to-current converter:** The use of 400-V voltage-to-current converters is the main originality of this proposal.

Through the amplifier OA1, the voltage  $V_{RC1}$  ( $V_{CEo}$  clamped) is reproduced on the resistor  $R_{LA1}$ , which generates a current  $i_{m1}$  equal to  $V_{RC1}/R_{LA1}$  and conveyed by  $AS_{LA1}$ .  $AS_{LA1}$  also absorbs the high voltage variations. The principle allows transmitting the  $V_{CEo}$  voltage information through high current values ( $i_{m1}$  and  $i_{m2}$  of a few dozens of milliamperes) to the analog-to-digital converters of the FPGA control board,

with the benefit of a high immunity transmission. In addition, they avoid introducing galvanic insulation stages, with the electrical reference being thus that of the control board.

Fig. 12 shows the operation timing that was chosen for carrying out all the required measurements during one PWM modulation period (10 ms). Three time scales are imbricated in the operation and are relative, from the higher to the lower, to the power-cycling period ( $PERIOD_{cyc}$  - ①), to the PWM modulation ( $PERIOD_{mod}$  - ②), and, lastly, to the switching period ( $PERIOD_{sw}$  - ③). With power cycling being provided by a sinusoidal current flow generated by PWM (100 Hz), the junction temperature variation during the cycle includes a main component adjusted to define the protocol and a parasitic component due to the current modulation.

The Zoom 1 shows the qualitative waveforms of the load current and of the junction temperature variation (here, IGBTs 1 and 6) on  $PERIOD_{mod}$ . The amplitude of the junction temperature variation at this scale is comprised between 5 °C and 10 °C (verified by IR camera measurements), depending on the chosen protocol.

The acquisition sequence is based on an indirect temperature measurement performed for each cancellation of the load current followed by a series of  $V_{CEo}(I_c)$  measurements around

100 A (Fig. 12—part ②). A load current sensor is already operating in the test bench to regulate the load current, with a typical amplitude value of 200 A at a frequency of 100 Hz in the case of the protocols described earlier. It is therefore possible to identify the time zone in which the current in two opposite IGBTs (IGBTs 1 and 6 or IGBTs 2 and 5) reaches  $\pm 100$  A (phase B or D in Fig. 12). Next, a series of pair values ( $V_{CEo}$ ,  $I_c$ ) is acquired over a few switching periods in the 100-A zone (Fig. 12—part ③) when the IGBTs 1 and 6 or IGBTs 2 and 5 are in the ON state. The sampling must avoid the switching phases in order to minimize acquisition noise. An accurate value of  $V_{CEo}$  (100 A) can be extracted from these measurements (see experimental results).

In a similar approach, still by keeping three IGBTs out of four in an OFF state, “zero-current” phase (phase A or C in part ② of Fig. 12) can be reserved to carry out indirect temperature measurement. During this phase, the 100-mA current is injected successively in both considered opposite IGBTs by turning on the auxiliary switches  $AS_1$ , then  $AS_6$  or  $AS_2$ , and then  $AS_5$  (with  $AS_5$  and  $AS_6$  being the homologous switches of  $AS_1$  and  $AS_2$  in the measurement board of IGBTs 5 and 6). The technique must consider the leakage current due to the IGBT+diode in the OFF state under dc voltage, which circulates into the IGBT under characterization. Fortunately, this leakage current is low: Its value is around 1 mA at 400 V for devices used in the presented tests. It can be neglected with regard to the 100-mA characterization current. More generally, the choice of the characterization current requires a compromise taking into account this consideration and the limitation of drop voltages across the connections.

In this configuration, the temperature measurement via  $V_{CEo}$  (100 mA) is not strictly synchronized with  $V_{CEo}$  (100 A) measurement. Nevertheless, the two phases (A and B and then C and D) are separated only by less than 1 ms, which makes it possible to neglect the temperature variation between both phases. The qualitative form of temperature variation given in part ② of Fig. 12 is close to the real form and shows that the error due to the delay is low. Therefore, the temperature of phase B (respectively D) can be considered as identical to that measured in phase A (respectively C).

Lastly, the value of  $V_{CEo}$  (100 A) must be measured at constant temperature, for example, 125 °C in the previous results. To respect this additional condition, the measurements of  $V_{CEo}$  (100 A) and  $V_{CEo}$  (100 mA) are made for each modulation period during the rise time of the thermal cycling. After temporary storage of the different pairs of values (around 1000), only the pair in which the temperature is closest to 125 °C will be stored in the end.

If an additional sensor provides the case temperature, which can be easily implemented, the value of the junction-to-case thermal resistance can be deduced from the previous measurements by the relation

$$R_{TH\text{ junction-case}} = (T_{\text{Junction}} - T_{\text{case}}) / V_{CEo}(100\text{ A}) \cdot 100\text{ A}$$

Therefore, if the proposed diagnosis system is effectively focused on the  $V_{ce0}$  monitoring, it needs to measure the junction temperature, voltage  $V_{ce0}$ , and current. If the measurement

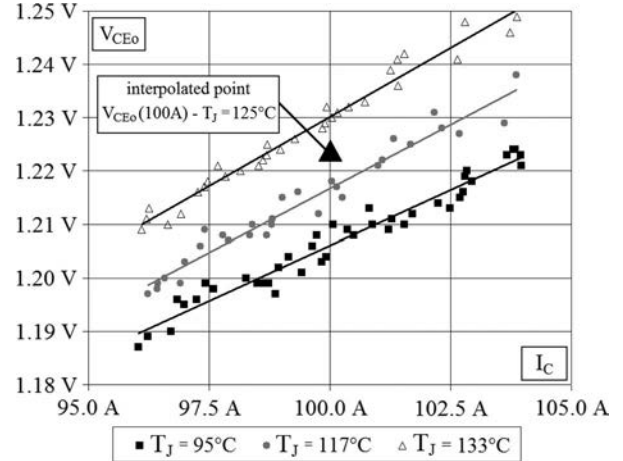


Fig. 13. Online measurements of  $V_{CEo}(I_c)$  on IGBT 6 for three temperatures.

of  $R_{TH\text{ junction-case}}$  is added, four significant parameters are supervised. They could be used in a more general monitoring of devices in order to prevent various kinds of failures.

3) *First Experimental Results:* A first test bench of the scheme presented in Fig. 11 was elaborated to evaluate the measurement feasibility. Fig. 13 shows the first results obtained on IGBT 1. For the moment, the data filtering and processing (linear regression) are not automated. Nevertheless, those points will not constitute a major difficulty. The important outcome is the high quality of these first acquisitions that demonstrates the method availability.

In Fig. 13, each measurement series corresponds to a modulation period (100 Hz) and to a junction temperature value extracted from the indirect measurement result [ $V_{CEo}$  (100 mA)], according to the process described in Fig. 12. In that first test, the measurement was not be made for each modulation period of the temperature cycle; therefore, the point  $V_{CEo}$  (100 A)-125 °C must be extrapolated from the closest results, corresponding here to junction temperature values of 117 °C and 133 °C. In a next step, it will be evaluated if the accuracy of such an interpolation is sufficient or if a higher number of samples will have to be acquired. Then, the measurement process will be entirely automated to provide the online supervision and the data storage.

## V. CONCLUSION

This paper leverages capital out of experimental results provided by a larger work concerning the IGBT module aging under power cycling and thermal cycling. The extracted results focus on  $V_{CE}$  voltage sensitivity with respect to the connection aging. Results show that  $V_{CE}$  is a relevant aging indicator if an appropriate measurement period is used throughout the module test. From this observation, the possibility to achieve supervision of IGBT devices in real operation by the mean of  $V_{CE}$  measurement is raised. The difficulty of such implementation is then emphasized. The last section proposes a particular solution available for the test benches used here. Currently under development, a measurement board will enable fast and efficient supervision of the future tests, without interrupting the

power operation. Techniques to apply this measurement to real converters in operation will be studied over the long term.

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