P-Type Doping of 4H-SiC for Integrated Bipolar and Unipolar Devices

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Abstract. P-type 4H-SiC layers formed by ion implantation need high temperature processes, which generate surface roughness, losing and incomplete activation of dopants. Due to dopant redistribution and channeling effect, it is difficult to predict the depth of the formed junctions. Vapor-Liquid-Solid (VLS) selective epitaxy is an alternative method to obtain locally highly doped p-type layers in the 10^{20} cm^{-3} range or more. The depth of this p-type layers or regions is accurately controlled by the initial Reactive-Ion-Etching (RIE) of the SiC. Lateral Junction Field Effect Transistor (JFET) devices are fabricated by integrating p-type layers created by Al ion implantation or VLS growth. The p-type VLS layers improve the access resistances on the electrodes of the fabricated devices.

Introduction

Power discrete SiC devices as Schottky diodes, Bipolar Junction Transistors (BJT), Junction Field Effect Transistors (JFET) and MOSFET are already commercialized. To improve performance and reliability in power electronics, a monolithic integration of this type of devices in SiC single crystal wafers is recommended. Thus the size of converters is reduced, the switching operation is improved and the power loss is decreased. Monolithic integration of SiC devices was already invoked to build vertical JFET and Junction Barrier Schottky diodes [1] and vertical or lateral BJT [2]. Industrial development of the SiC monolithic technology is still in progress, delayed by the need to improve some technological steps, particularly those that can enhance the quality of semi-insulating SiC substrates or that can reduce the resistivity of the p-type layers.

In this paper, SiC p-type doping by aluminum (Al) ion implantation is compared to the alternative VLS epitaxy method to fabricate integrated power devices.

Al ion implantation

P-type localized regions in SiC are in general obtained by ion implantation which is still the unique method of local doping due to the very slow diffusion of dopants in SiC. Moreover, due to the high activation energies of the p-type dopants in SiC (~0.2 eV for aluminum and ~0.3 eV for boron), obtaining a net doping level requires to implant higher doses of ions. That leads to create numerous crystalline defects up to local amorphisation of the material if the ion implantation is processed at room temperature (RT).

To recover a good crystalline quality and to activate the implanted impurities by migration of implanted ions in SiC atomic substitutional sites (for example, Al is a dopant only when it substitutes to a Si site), a high temperature annealing is necessary, typically in the range of 1600-1800°C [3]. Figure 1 presents sheet resistances (R_{sh}) measured with a four-point probe

technique on p-type layers created by Al ion implantation. Post-implantation annealing has been performed during 30 min or one hour at various temperatures from 1600°C to 1800°C. R_{sh} decreases when either the annealing temperature or the annealing time increases. The linearity of the R_{sh} variations with the post-implant annealing temperature, proves a non-saturation of the electrical dopant activation even after annealing at 1800°C [4].

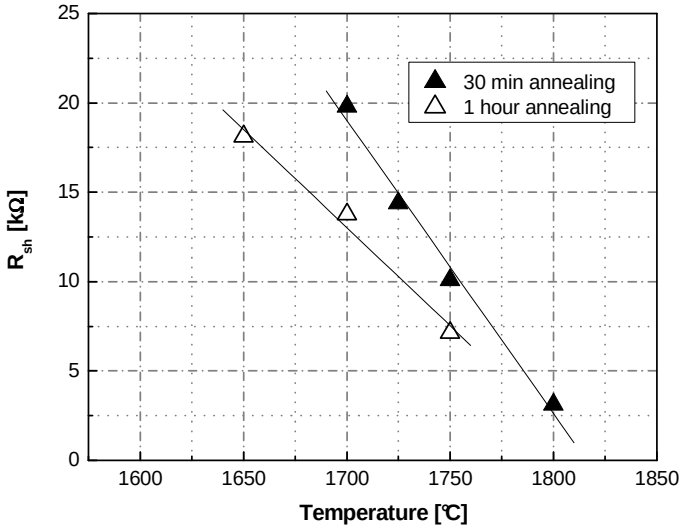
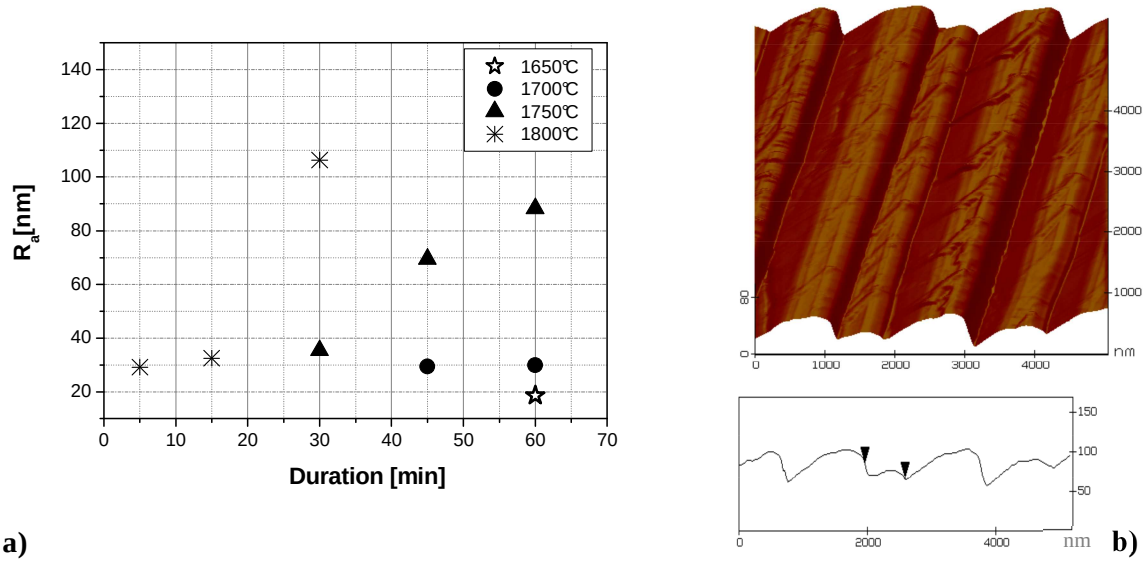


Fig.1. Sheet resistance measured at RT by four-point probe technique on p-type SiC layers created by Al ion implantation and annealed at different temperatures and durations [4].

The annealing temperature is limited by the surface deterioration of the implanted layers. A strong degradation of the surface occurs by sublimation of Si from the SiC, resulting in a rough surface. Surface roughness limits device performances by inducing an increase of leakage currents in off-state and a degradation of the breakdown voltages. The roughness increases when either the annealing temperature or the annealing time increases (Fig. 2a) by forming terraces of several tens of nanometers (Fig. 2b).



a) **b)**

Fig2. Surface deterioration of SiC: arithmetic average roughness (R_a) measured with Tencor alpha-step stylus after annealing at different temperatures and durations (a), Atomic Force Microscopy (AFM) measurement on a virgin SiC sample annealed at 1700°C during 30 min (b).

By increasing temperature, the sublimation of Si can induce also an etching effect of the SiC surface and thus a significant loss of implanted dopants in the near surface region [5]. Figure 3 presents Al implanted doping profiles measured before and after annealing. Compared to samples just implanted, the Al profiles after annealing seems to be offset toward the surface. The quantity of the dopant loss increases with the annealing temperature. It is worth mentioning that on these samples the ion implantation was performed at 300°C to avoid SiC amorphization [6]. In amorphous layers, a redistribution of the dopants occurs, this phenomenon being discussed thereafter at the end of this section.

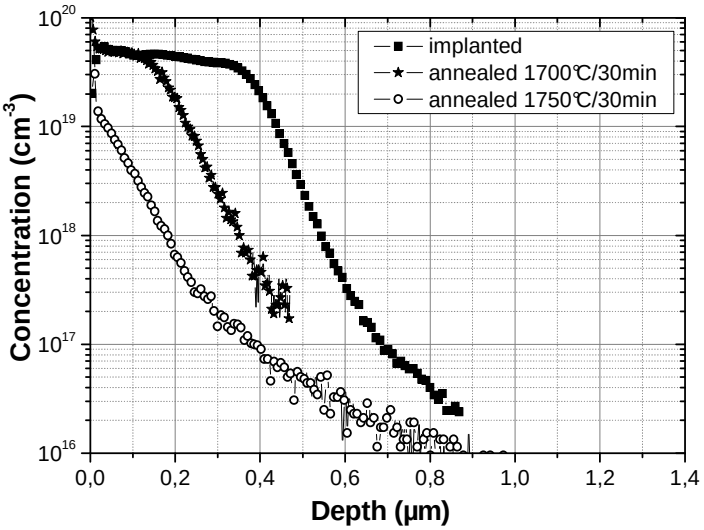


Fig.3. Al profiles measured by Secondary Ion Mass Spectrometry (SIMS) before and after post-implantation annealing highlighting the lost of the dopants after high temperature annealing.

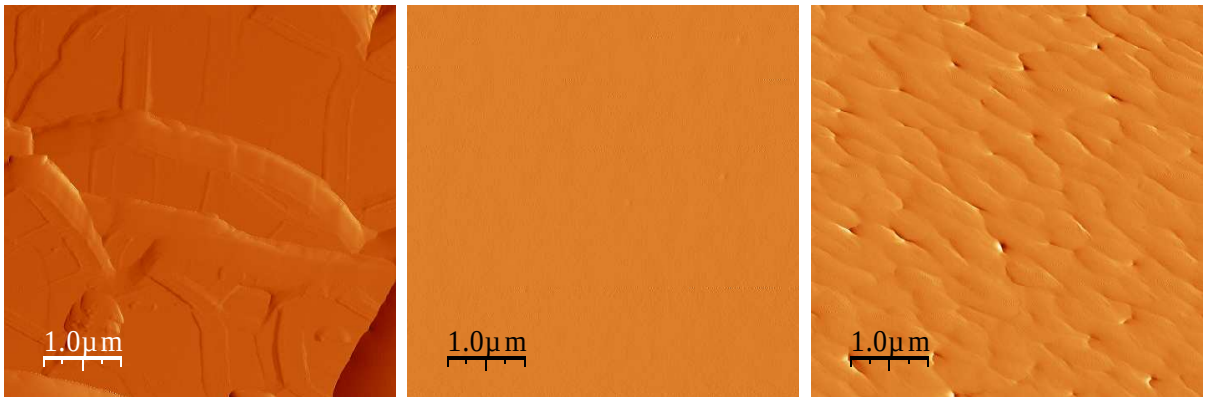
Surface deterioration and the shift towards the surface of the implanted dopants should induce an increase of the sheet resistance of the p-type layers which is in contradiction with the results we present in figure 1 where the sheet resistance decreases by increasing the post-implantation annealing temperature. The p-type SiC sheet resistances from figure 1 have been measured on samples whose surfaces were protected with a dedicated cap (detailed hereafter). Therefore, in figure 1 the decreasing of the sheet resistances either with the temperature and the duration of the annealing is fundamentally caused by the increase of the dopant activation.

Si sublimation has been reported to be prevented by capping the surface with AlN [7], graphite (C) [8] or by using silane partial overpressure during annealing [9]. In this later case an accurate control of the gas flux is necessary to prevent Si droplet deposition.

However, the efficiency of these protections is shown to be temperature limited except for the graphite layer which resists up to 1800°C. The graphite cap layer is obtained by baking at ~750°C a photoresist layer deposited by spin-coating at the SiC wafer surface. This method is widely used today in SiC device fabrication needing doping by ion implantation.

The C cap showed in general a very good preservation of the sample surface state. Nevertheless, the surface morphology after annealing was shown to depend on implantation parameters (temperature and total doses), even when using a graphite cap protection. The use of the graphite cap influences also the diffusion of dopants and their activation rate [10]. Figure 4 presents AFM images on Al implanted SiC samples measured after annealing with and without a C-cap. After annealing the C-cap has been removed by an oxygen dry plasma etching. For an Al total dose of $1.75\times10^{15}cm^{-2}$ the presence of the C-cap during annealing allowed a very good preservation of the sample surface sate. After 1800°C/30 min annealing, the average roughness is 0.46 nm, slightly higher than for an unimplanted sample (0.31 nm).

By increasing the Al total implanted dose to 3.5×10^{15} cm^{-2} the average roughness increases to 1.49 nm despite the use of the C-cap during annealing.



a) b) c)

Fig.4. 5×5 µm² AFM images for 1.75×10^{15} Al.cm^{-2} implanted sample after 1800°C/30 min annealed without graphite cap (a) and with a graphite cap (b). The right AFM image (c) is for 3.5×10^{15} Al.cm^{-2} implanted sample after 1800°C/30 min annealed with a graphite cap.

Preserving the surface state during annealing by using the C-cap allowed us to focus on the study of the crystal recovery of amorphous SiC layers created by Al room temperature (RT) ion implantation. The presence of the amorphous layers, in general, is identified and localized by Rutherford Backscattering Spectrometry in the Channeling mode (RBS/C) measurements. Figure 5 presents the example of the 1.75×10^{15} cm^{-2} Al implanted sample at RT.

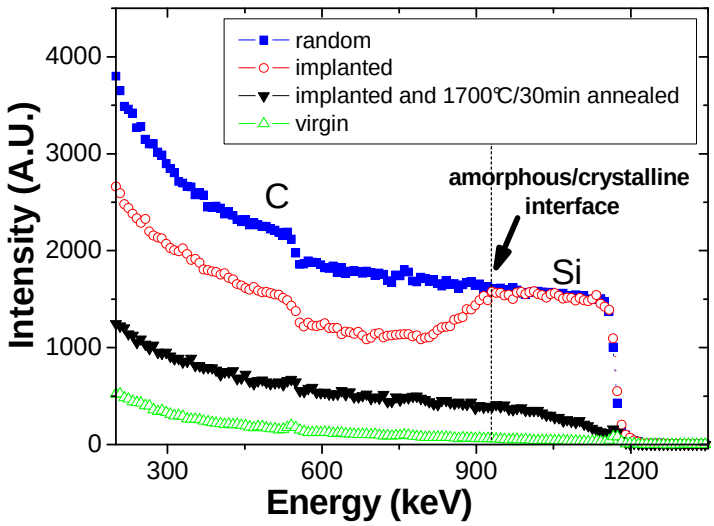


Fig. 5. RBS/C spectra on 4H- SiC samples implanted at RT with 1.75×10^{15} cm^{-2} Al total dose, before and after annealing

When ion implantation is performed at RT, dopant redistribution occurs also during the annealing, by a gettering phenomenon localized at the proximity of the end-of-range defects formed at the initial amorphous-crystalline interface [11]. In figure 6, SIMS (Secondary Ion Mass Spectroscopy) dopant profiles are presented for four total implanted doses after 1700°C/30min annealing. After annealing, dopant diffusion increases with the dopant dose.

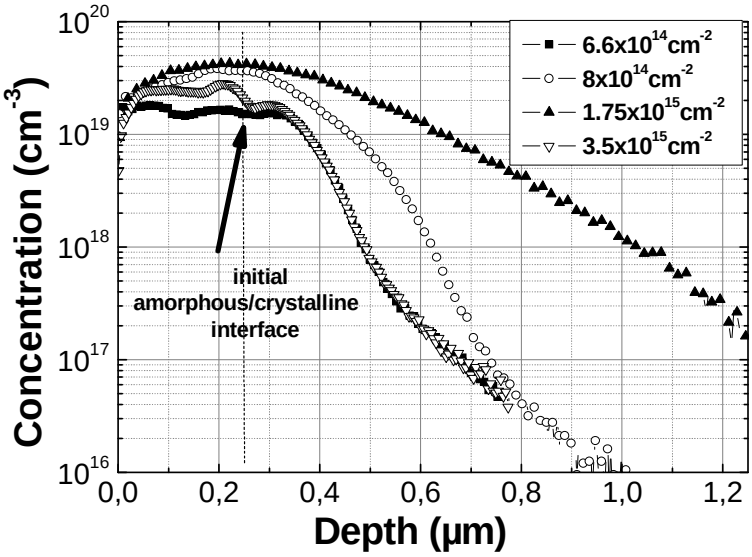


Fig.6. SIMS doping profiles obtained after annealing on samples implanted Al with varying total doses

Dopant redistribution and diffusion are observed towards the bulk and the surface (dopant loss) with a peak formed at the former initial amorphous/crystalline interface observed by RBS/C after ion implantation and before annealing.

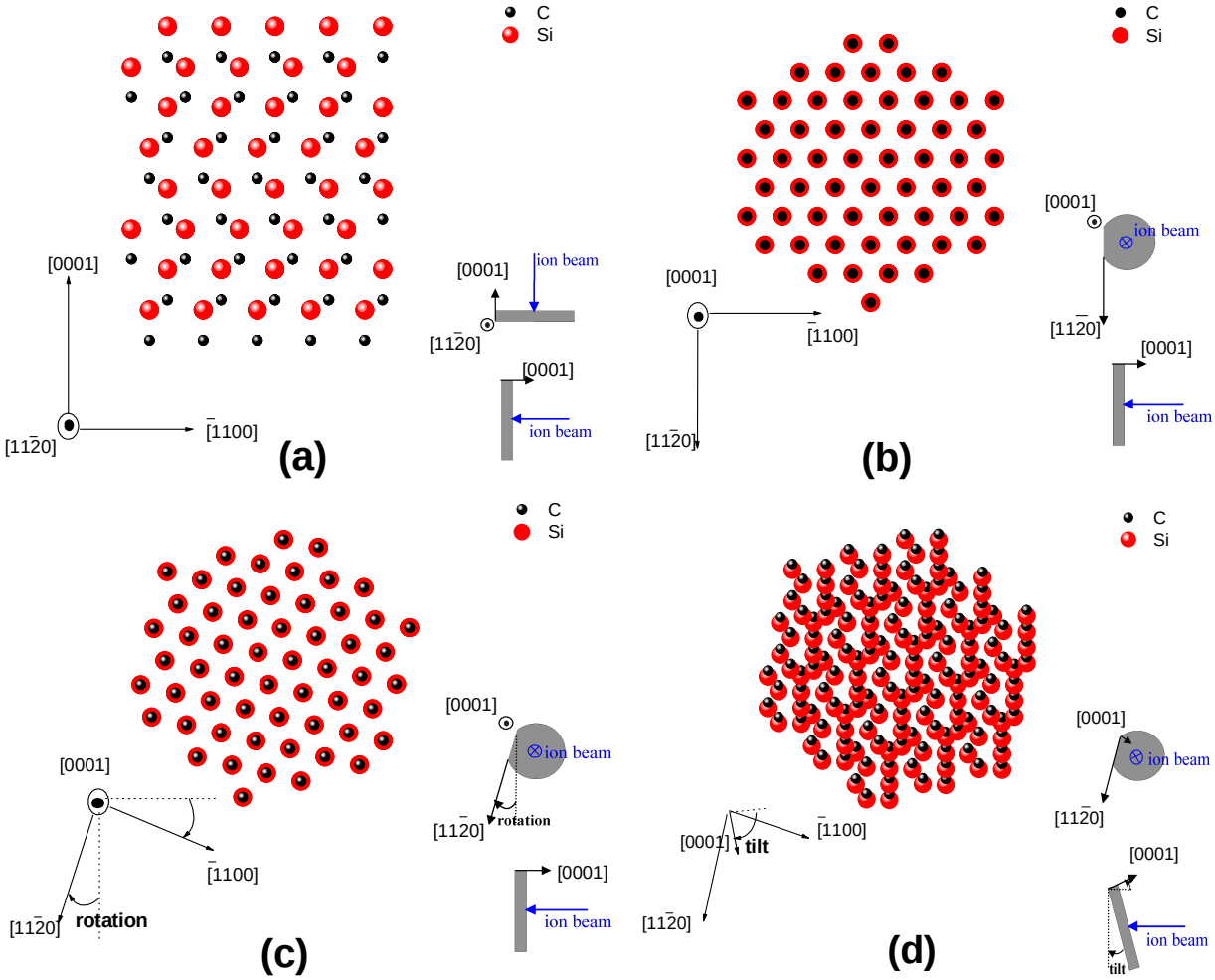


Fig.7 4H-SiC crystalline structure with cross-section (a), top view (b) and disorientation of the surface with two defined angles, rotation (c) and tilt (d), in order to avoid the channeling effect.

The shape of the dopant profile considerably affects the electrical behavior of devices based on these p-n junctions. Dopant redistribution may have a positive influence on the increase of the p-n junction breakdown voltage. Nevertheless, graduate junctions are in general not compatible with high levels of carrier injection.

Implanted dopants profiles and the depth of the formed junctions are also difficult to be accurately estimated due to the channeling effect. As 4H-SiC presents a hexagonal crystalline structure, a strong channeling effect is observed especially in the case of Al ions. Figure 7 presents the crystalline structure of the 4H-SiC polytype and disorientation of the ion implanted surface (with two defined angles rotation and tilt) in order to avoid or at least minimized the channeling effect. The channeling of the Al ions is quite difficult to control and to eliminate in 4H-SiC even when in addition to the surface disorientation an amorphous layer as SiO_2 is present in the surface. To estimate the doping profile of Al implanted ions, dedicated Monte-Carlo software has been developed considering the crystalline structure of the SiC [12]. Electrical characteristics of the final fabricated SiC devices could be predicted, but with uncertainties due to the difficulty to estimate the depth of the different p-type layers.

Vapor-Liquid-Solid Growth

An alternative method to locally dope SiC is Vapor-Liquid-Solid (VLS) selective epitaxy. Highly p-type doped SiC can be obtained leading to considerable reduction of both the p-type SiC resistivity and the specific resistance of ohmic contacts formed on it.

The technological process is detailed in [13] and is schematically presented in Fig. 8. The depth of the p-type layers is accurately controlled by the initial plasma dry etching of the SiC, performed to create the wells where the Al-Si stacks are deposited and converted in 4H-SiC by VLS epitaxy. Thus, as Al ion implantation, our VLS epitaxy is a local doping method to create p-type 4H-SiC layers.

Al-Si stacks are deposited by electron-beam PVD deposition, thicknesses of the layers and deposition rate are precisely monitored by quartz piezoelectric crystals. Dry etching of the SiC is made by Reactive-Ion-Etching (RIE) or Inductively-Coupled-Plasma (ICP) with SF_6/O_2 chemistry and using a Ni hard mask defined by photolithography at the surface of the SiC samples.

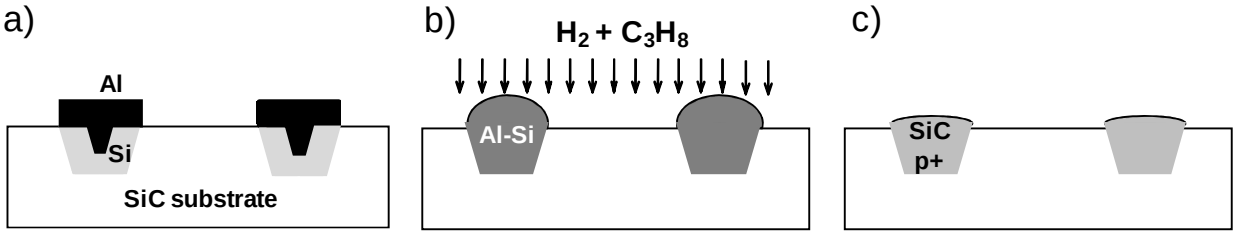


Fig. 8 - Schematic description of the VLS process: a) deposition of Al-Si stack inside the trenches formed by RIE or ICP in SiC, b) melting of Al-Si and addition of propane for the VLS growth, c) formation of P^+-type SiC [13].

During the VLS growth the samples are heated in a vertical cold wall reactor (Figure 9) up to 1100°C. This value is very low compared to temperatures needed for post-implantation annealing (~1700°C) or classical SiC CVD epitaxy (~1400°C-1600°C), reducing thus device cost fabrication if this alternative method is implemented at an industrial scale.

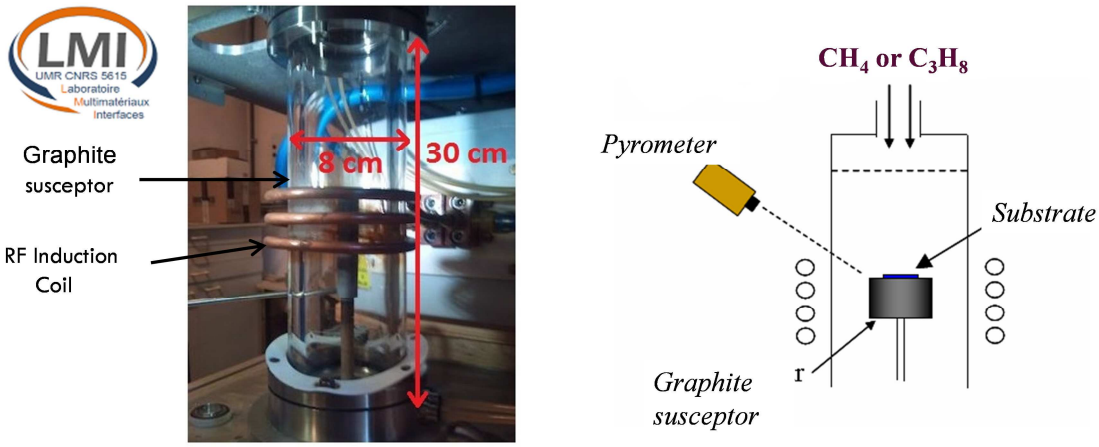


Fig. 9 – Cold wall vertical reactor utilized during VLS growth

P^+-type SiC layers obtained by VLS have high Al doping concentrations, in the 10^{20} cm^{-3} range. Fig. 10 presents a typical profile obtained by SIMS [14].

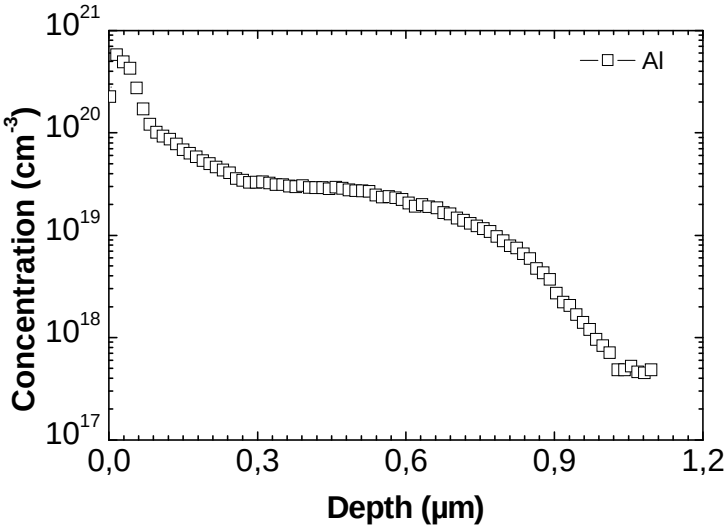


Fig10. Al doping profile from SIMS on VLS SiC p^+ layers.

Ohmic contacts have been evaluated on these p-type VLS layers with patterned Transfer Length Method (TLM) structures using a specific Ni-Ti-Al metal alloy [15]. The contact is ohmic even without post-metallization annealing. Specific contact resistances as low as 1.3×10^{-6} $\Omega.cm^2$ have been obtained after 500-800°C Rapid Thermal Annealing performed under a pure argon atmosphere [16].

Nevertheless, the VLS growth is still an immature technological process. Works remain to identify the steps to be optimized in order to improve the quality of the obtained pn junctions, which still suffer from a poor interface between the p-type VLS layers and the initial substrate. Figure 11 presents current-voltage measurements on two PiN diodes with p-type emitters fabricated by VLS growth. These measurements were made on vertical diode configuration with a “Signatone S1160” probe station and Keithley 2410 or 2636 Source Measure Unit (SMU).

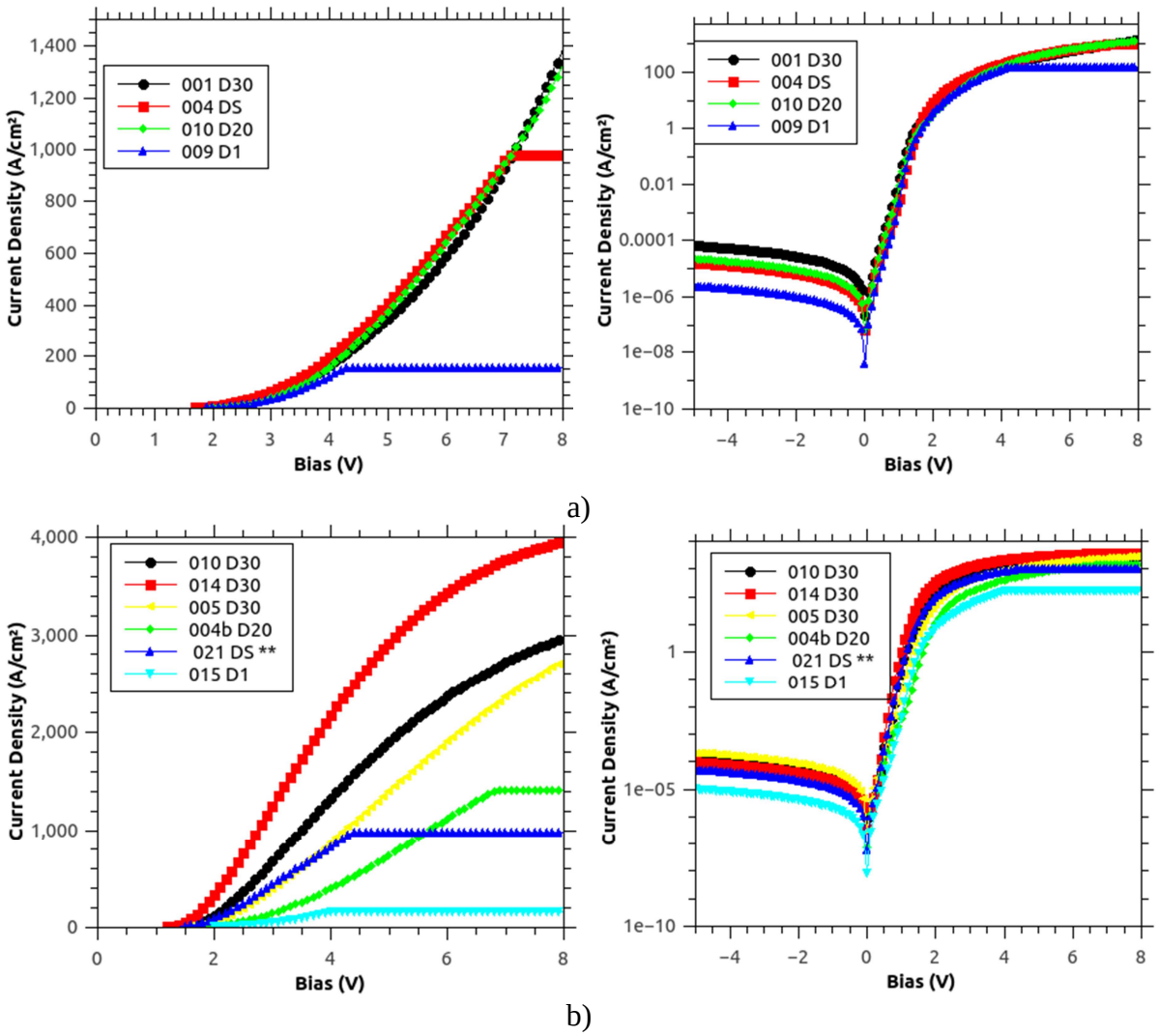


Fig. 11. Current-voltage characteristics of PiN 4H-SiC diodes with the emitter fabricated by VLS. Current densities versus applied bias are presented for various diode sizes; a) and b) correspond to two samples with different technological and VLS growth parameters. The constant current plateau obtained for the diodes with larger sizes is due to the Source Measure Unit current limit.

Current densities obtained on diodes with varied sizes from 150 µm to 1mm are plotted in forward bias. For the diodes with larger sizes, the constant current plateau obtained at the end of the current densities - voltage characteristic, is a measurement artifact due to the SMU current limit.

In general very high current densities are obtained (several thousand of A/cm^2) thanks to the high Al level doping in the p-type emitters that VLS method allows (Figure 10 – SIMS spectra of the Al doping profile). But if for the sample presented in Fig. 11a the current density is independent on the diode sizes and a typical threshold (~3V for 4H-SiC P/N junctions) is obtained, for the sample presented in Fig. 11b lower threshold is obtained in forward regime. Moreover, for these diodes the current density varies with the diameter sizes. However in reverse bias, for the all presented VLS diodes, low values are obtained for the leakage current.

Integrated lateral JFETs

Lateral JFET (LJFET) transistors with n-type and p-type channels have been fabricated, integrated monolithically within the same SiC wafer. The ultimate goal of this study is to realize an integrated inverter leg with complementary LJFET switches on the same 4H-SiC chip (Figure 12).

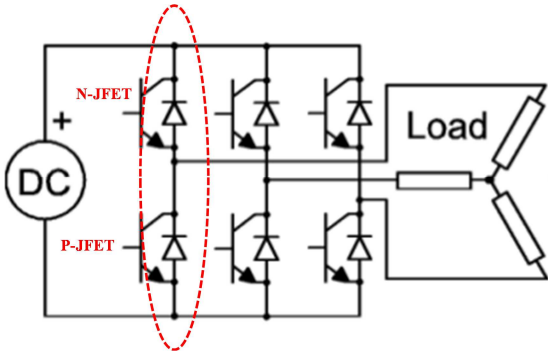


Fig. 12. Simplified inverter diagram with a leg based on complementary lateral JFETs.

Several batches have been fabricated, the first one (detailed in [17]) with p^+ wells created by Al ion implantation, and the second one (detailed in [18]) with VLS p^+ wells. The p^+ wells were utilized as source and drain contacting layers for the P-JFET and as p^+ gate for the N-JFET. For both batches, the n^+ wells have been obtained by nitrogen ion implantation.

For the structure with both p^+ and n^+ wells realized by ion implantation, the thickness control of the p-type channel was problematic due to the channeling of the ions implanted to dope the gate (Figure 13). This phenomenon was less marked for the N-JFETs due to the higher project ranges (the average penetration depths during ion implantation) of the nitrogen ions used to dope the n-channel. Whereas the p-type channels of the P-JFETs were unintentionally normally-off or even always blocked.

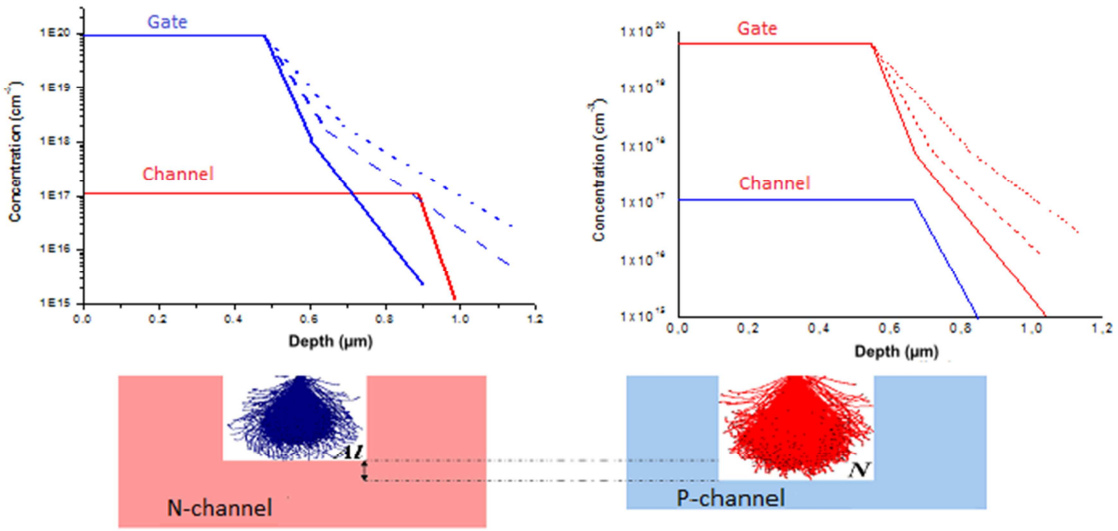


Fig. 13. Schematic presentation of the JFET channels hidden by the ion implanted gates.

Finally an experimental study based on SIMS measurements and MC simulations was necessary to consider the channeling effect in the 4H-SiC hexagonal crystalline structure. A technological process has been defined to obtain devices working despite the presence of the channeling effect.

The VLS process allowed us to accurately control the thickness of the p-type wells. However, the electrical characteristics of the JFET with p^+ wells created by VLS are affected by the interface between the VLS p^+ gate and the n-type channel, which is a CVD epilayer. The structural defects observed by Transmission Electronic Microscopy [19] explain the high reverse leakage current measured between gate and source. Nevertheless, the obtained results have shown that the p^+ VLS layers could already be used to improve the access resistances on the P-JFET transistors where the VLS p^+ layers have been utilized as source and drain. Figure 14 compares typical results we obtained for the first p-type JFETs fabricated by Al ion implantation and those made by VLS. The VLS process allows us to multiply drain-source current by more than one order of magnitude.

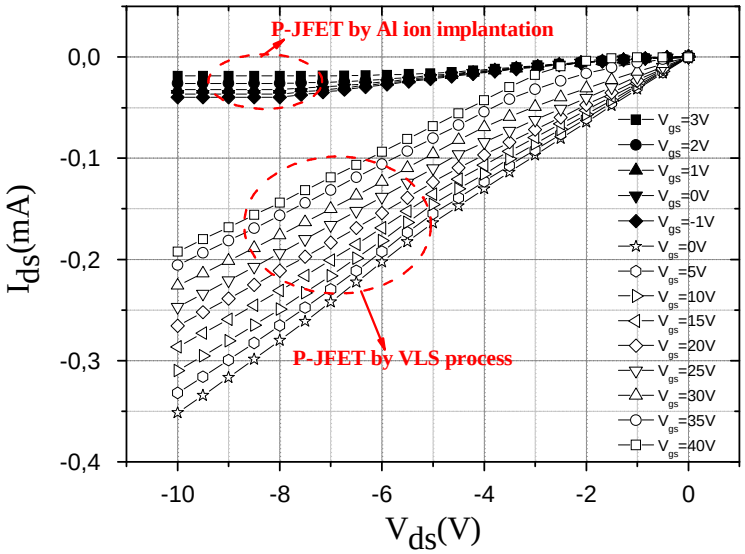


Fig. 14. $I_{ds}(V_{ds},V_{gs})$ characteristics for P-type JFETs with p-wells created by Al ion implantation (solid symbols) and VLS process (open symbols)

Conclusion

Industrial development of the SiC monolithic technology needs a significant drop of the resistivity of the p-type layers and of the ohmic contact formed on them. A technological breakthrough will be obtained when an alternative method to ion implantation will be found in order to locally dope SiC, using only low temperature processes, thus preserving the surface state and allowing to precisely predict the junction depths. VLS selective epitaxy is a good candidate for such objectives. If creating reliable P/N junctions by this method seems to be yet premature, highly p-type doped layers and ohmic contacts with specific contact resistances as low as 1.3×10^{-6} $\Omega.cm^2$ have already been obtained by VLS. Therefore we demonstrated that VLS layers could already be utilized on the top of p-type CVD epilayers in order to improve the access resistances.

Acknowledgments

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