Using Laminated Metal Foam as the Top-Side Contact of a PCB-Embedded Power Die

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***Abstract*—The proposed innovative manufacturing process—described in detail—uses metal foam to create a pressed contact between the top side of a PCB-embedded power die and the rest of the circuit. Initial prototypes were constructed using diodes with die dimensions of 4 mm × 6.35 mm. The prototypes were electrically characterized: the chip and contact DC and AC impedance values were measured and compared with those obtained for conventional packaging that uses bond wires. The electrical impedance of the prototypes was found to be similar to that of a state-of-the-art industrial package. Moreover, the proposed process is simple and cost-effective. Although the results presented in this letter are promising, further research is necessary to fully assess the benefits and limitations of the process.**

***Index Terms* — Embedded die, high-density integration converter, PCB embedding, PCB integration, power electronics packaging, pressed contact**

I. Introduction

Almost all discrete power components and modules use bond wires to connect the top side of the chips to the leads. Although this process is cost-effective and mature, it has some limitations for high-speed power semiconductors. First, overvoltages are produced by the relatively high inductance of the wire bonding interconnects (about 10 nH; TO247 package) in conjunction with high switching speeds, which forces designers to oversize the semiconductors [1]. Second, the relatively low reliability of bonding wires often determines package lifetime [2], [3].

Previous research has mainly sought to replace bonding wires in power electronics with improved technologies. Flipping the chips is a common approach in small signal electronics (e.g., BGA packages, etc.) that use planar transistors. However, this technique is unsuitable for power electronics, which use mostly vertical components.

Bonding wires can be replaced with flex foils that are sintered or soldered onto the top sides of the dies, thereby decreasing stray inductance by about 10 % while improving power module reliability [4], [5]. Furthermore, if one side of the flex foil is used to connect the power dies, the gate drive circuit can be built on the other side [5]. However, for this technique the top-side metallization of the die, which often consists of an aluminum alloy, must be compatible with the sintering or soldering process. Some sintering pastes can be used to connect aluminum and copper, but solders cannot. Thus, before soldering, an appropriate metal layer (e.g., titanium/nickel/silver) must be deposited.

Another solution, which is expected to solve most of the wire bonding drawbacks listed above, consists in embedding the chips within a PCB. In the most common process, the bottom sides of the embedded dies are soldered [6], [7] or sintered [8], [9], [10] onto a PCB or DBC, and the resulting assembly is then fully embedded in prepreg. The contacts on the top side are manufactured by 1) drilling through the prepreg down to the die and by 2) growing vias, for example through copper electrodeposition. Drilling may be mechanical [6], but is typically done with a laser [8], [9]. One of the drawbacks of this method is that the die top sides are usually not directly compatible with copper electrodeposition and thus require intermediate metal deposits. Furthermore, the process involves numerous steps, some of which are quite costly (metallization, laser drilling) and time-consuming (electrodeposition).

On the other hand, PCB manufacturing processes are fully mastered, which should improve the reliability assessment—a crucial factor in critical applications. Additionally, copper planes placed above and below the dies embedded within the PCB act as shields, greatly improving the electromagnetic compatibility (EMC) of the module. Moreover, PCB integration aims to functionalize the PCB: the copper tracks are used not only for electrical links, but also for capacitors, inductor windings, heat sinks, etc. Finally, PCB integration paves the way for 3D electronics, for example by stacking dies [11], [12].

This letter only examines the integration of active components: an innovative process for chip embedding is proposed, it uses a pressed contact made of metal foam. The process is described in Section II. Section III presents the electrical characterizations of several prototypes. Our conclusions are presented in Section IV.

II. Proposed Manufacturing Process

Intended as a first step, this letter considers the integration of a vertical diode with a single large pad on each side.

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Nevertheless, ongoing research is investigating power MOSFET integration.

The manufacturing process is quite straightforward; it consists of only two main steps. First, the bottom side of the chip is soldered onto a "bottom PCB" in a reflow oven (Fig. 1a) using a standard soldering paste and thermal profile. Then the stack is prepared, composed of (Fig. 1b)

- the bottom PCB (and the chip)
- layers of prepreg
- a piece of metal foam
- the top PCB

For the prototypes, we used Ni-5763 nickel foam (obtained from Recemat BV) with an average pore diameter of about 350 µm and with between 57 and 63 pores per inch [13]. The connectivity (mean number of cell edges meeting at any node) of the foam, not specified on the datasheet, was estimated at about 4 with an optical microscope.

We used a piece of foam that was smaller than the die to keep the pressed foam from covering the guard rings of the embedded diode. This precaution prevented any modification of the electric field distribution above the guard rings, thereby preventing the degradation of the blocking capabilities of the device [11]. We used 4 mm × 6.35 mm chips and 2 mm × 4 mm pieces of foam, resulting in a "safety" distance of about 1 mm between the foam and the edges of the die. A simple cutter blade that provided accurate and sharp cuts was used to cut the foam.

We stacked four layers of Panasonic R-1650V prepreg. One layer was used to center the piece of foam on the chip (Fig. 1b). Maintained in position by this layer of prepreg, the piece of foam was neither attached to the top PCB nor to the die. This stack was then laminated using the temperature and pressure profiles required by the prepreg. In our case, this step consisted of two phases: 1) 40 min at 130 °C, 1 MPa, and 2) 90 min at 190 °C, 2.5 MPa. During the heating phases, the temperature was ramped up at a rate of $0.1\ ℃ \cdot s^{-1}$.

The top and bottom copper planes could then be used, as in a standard PCB, to make an electrical circuit and/or a heat sink.

This process yields a compact assembly (Fig. 1c) in which the epoxy resin has replaced the air in the entire device and has flooded the metal foam. The foam is in direct contact with the PCB track (nickel/copper contact bonding) on one side and with the die top-side metallization on the other side (nickel/aluminum contact bonding). Lamination only negligibly affected the width of the piece of foam and its centered position on the die (Fig. 2). A series of prototypes constructed to characterize the foam deformations showed that the lateral expansion of the foam due to lamination was limited to about 0.15 mm—that is, less than 4 % on each side of a 2 mm-wide piece of metal foam. These results indicate that the 1 mm-wide "safety" gap we retained between the foam and the edge of the die could be reduced, thereby improving the electrical and thermal properties of the contact.

Before pressing, the Ni-5793 foam was 1.4 mm thick with a porosity of 96 %; after-pressing values were 220 µm and 75 %, respectively. Our tests used highly cohesive foam: no loose foam threads were found in any of the 30 prototypes we cut open.

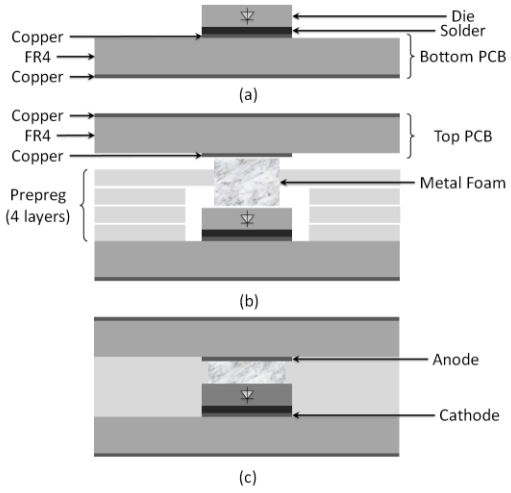

Fig. 1. Steps of the manufacturing process using metal foam: (a) the die is soldered onto the bottom PCB; (b) prepreg layers and a piece of metal foam are positioned; (c) the stack is laminated, the epoxy resin polymerizes and floods the foam.

III. Integration of a Power Die

A. Introduction

The proposed process was used to integrate a diode. Because of die availability constraints with our industrial supplier, we used the body diodes of 3 $m\Omega_{maxi}$, 18 A, 65 V N-MOSFETs, which had their sources and gates short-circuited. They could thus be considered PIN diodes consisting of the transistor body diodes. These dies are intended for use in intelligent power switches sold in a standard PQFN23 package. Made of aluminum with 1% silicon, the top-side metallization was 3.6 µm thick. The 1.6 µm-thick bottom-side metallization was made of Ti/Ni/Ag, which is compatible with standard soldering processes. In addition, these dies were large enough (4 mm × 6.35 mm) to be handled easily with bare hands.

The prototypes we manufactured using our process were electrically characterized in the on- and off-states. The results were then compared with those obtained for the standard PQFN23 package.

B. DC characteristics

A Keysight B1505a power device analyzer was used to

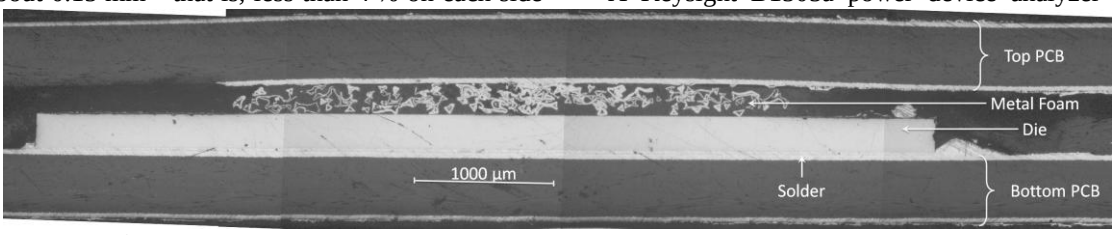

Fig. 2. Cross-sectional view of an embedded diode. The die is 254 µm thick.

measure the forward characteristics of the integrated and reference devices (Fig. 3). Kelvin measurements were taken at ambient temperature: the current pulses were short enough to keep the dies from self-heating.

Under these conditions, the on-state forward voltage included the voltage drop in the power die, the bottom solder, and the connection between the top side of the die and the package (metal foam in our package vs. bonding wires in the reference).

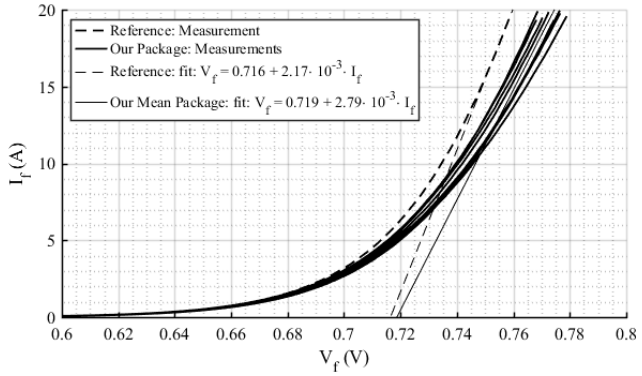

Fig. 3. Forward intrinsic diode current versus voltage drop: measured values of the reference and of our nine prototypes and steady-state model.

The traces (Fig. 3) were very similar: the reference diode and its package had a series resistance of 2.17 mΩ, compared with a mean resistance value of 2.79 mΩ for our nine prototypes. The process appears to be reproducible, given that the standard deviation was merely 153 µΩ (i.e., 5 % of the total resistance).

Differences between the prototype and reference series resistance values are attributable to variations in die characteristics and in the electrical performance of the contacts and solders. However, these measurements show that our pressed contact using metal foam had a resistance similar to that obtained with bond wires (the reference used six wires with a 300 µm diameter, each with two connections to the die).

A Tektronix 371a high-power curve tracer was used to test our prototype and the reference at higher currents. The test results indicated that both can handle repetitive surge currents of at least 300 A.

Furthermore, most of our prototypes had a breakdown voltage (measured at $I_f = -1$ mA) close to 75 V, and the characteristic curves were similar to the reference curve. The diodes had a specified breakdown voltage of at least 65 V. Their blocking performance was therefore not noticeably affected by the proposed integration process.

C. AC characteristics: dynamic impedance

We measured the dynamic resistance (resistance vs. frequency) of one of our prototypes and of the reference and compared the values using the setup illustrated in Fig. 4.

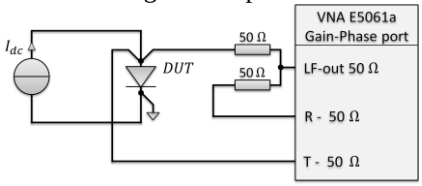

Fig. 4. Setup used to measure the dynamic impedance of a diode

A DC current I_{dc} was forced into the diode being characterized and a small AC stimulus was superimposed onto this biasing current. The forward-biased junction was directly connected to the gain-phase section of an E5061b vector network analyzer (VNA), which was used in GP-parallel mode to measure the impedance of the junction. The output power of the VNA oscillator was set to 0 dBm (in 50 Ω). Several measurements were taken at biasing currents ranging from 250 mA to 2 A (Fig. 5). All measurements were performed at thermal equilibrium; the junction temperature was above ambient because of self-heating. With this setup, the VNA-measured impedance value was equal to the dynamic impedance of the component, that is, the inverse of the slope of the (V_f, I_f) plot (Fig. 3) at the considered biasing point.

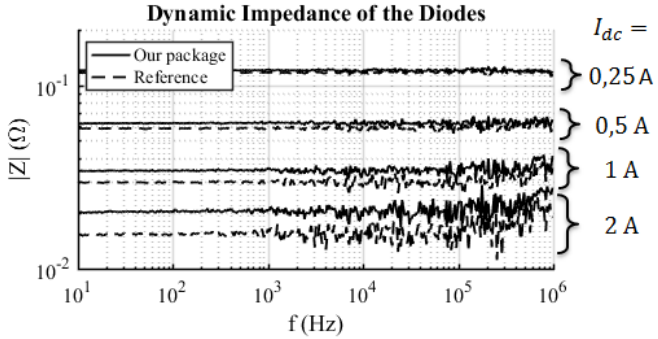

Fig. 5. Measured dynamic impedance of the diodes at various bias currents

The measured dynamic impedance values remained flat up to at least 1 MHz and were coherent with the results obtained with the component analyzer. These results showed that, despite the magnetic properties of nickel, no high-frequency loss is to be expected.

One of the objectives of PCB integration is to decrease stray inductances. The proposed process places the contacts between the die and the PCB, directly beneath and a few hundred micrometers above the die. The packaging-induced inductance is therefore quasi null and mostly accounted for by the layout.

IV. Conclusion

This letter presents an innovative process to manufacture the top-side connection of a PCB-embedded power die using metal foam. Compared with other PCB integration techniques, the proposed process is simple and cost-effective; it requires no expensive equipment. These characteristics make our process most appropriate for PCB embedding. Measurements showed that the electrical performance of the prototypes was very similar to that of a conventional, high-performance package with a wire-bonded chip.

Although this initial investigation delivered promising results, future research will be necessary to examine the impact of the process on embedded semiconductor performance. Subsequent studies should verify the stability of the method with respect to temperature, humidity, and time, as well as characterize the interface between the foam and the die top-side metallization.

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