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Networks-on-Chip Cortex Inspired Communication To Reduce Energy Consumption

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Introduction

Complex many-cores and SoCs contain one (if not several) NoCs. NoC power consumption can represent a significant proportion (40%) of the overall power consumption [M Taylor 2002].

Main components of a NoC



Cortex Inspired Communication

Brain is subjected to **two major constraints**:

- low level of available energy (i.e. sugar in the blood)
- 25 W overall maximum power dissipation [E R Kandel 2000]

The human brain stores and uses sensory information by using representational codes that rely on very few active neurons [P Lennie 2003].

Human neural system Network-on-chip

• Allow only **one transition** among a set of wires



Problem: only 1 bit of data sent

Use the bit position as an additionnal data For a bus of N wires, it gives log₂(N) bits of data



Related works

-Links power consumption computation:

$$P_d = \sum_{i=1}^{N_w} \alpha_i \times C_i \times V_{dd}^2 \times f_{clk}$$

- P_d, wires dynamic power consumption • C_i, wire i capacitance • N_w, the number of wires • α_i , wire i switching activity
 - V_{dd}, power supply • f_{clk}, clock frequency

Crosstalk effects have an important impact

-	-
Active nerve fibers rate: 1%	• Active wires rate per transmission : 50%
Power hungry neurons spikes	• Simultaneous wire transitions cause Crosstalk
Energy efficient coding representation	No data coding
	 Network maximum bandwidth under-used

Opportunities to reduce the NoC energy transmission cost

Tradeoff between bandwidth and energy efficiency

Proposition: Reduce the wire use rate to decrease energy consumption and delete Crosstalk





This is still not enough to send a data in one cycle, we must **decompose** a flit in several parts



Problem: Increase the packet transmission time

Allow the CIC transmission considering the network local state

Transmission strategies

CIC restriction according to the **local state** of the network. Three strategies are proposed:

- OCC : Buffer occupancy checking of the following router
- CONT : Contention checking at each output
- CONT+OCC : Restriction increased with both checking

Buffer occupancy checking architecture



JL

on links power consumption

 Several links energy optimizations have been proposed for NoCs:

- Bus coding to avoid Crosstalk in [M Taassori 2009]
- Serialized links [S Ogg 2008]
- Approximate computing [A Mineo 2013]

Only effective on very long wires

No tradeoff energy/throughput considered

Idea: mimic the brain processing, only few synapses among myriad are active at the same time.

Practical example

Clock cycle i	Data to send F[3 :0] (4 bits)	One-hot coding a ₁₅ -a ₀ (16 bits)	Data on links w ₁₅ -w ₀ (16 bits)
0	0001	0000 0000 0000 0010	0000 0000 0000 0010
1	1010	0000 0100 0000 0000	0000 0100 0000 0010
2	0101	0000 0000 0010 0000	0000 0100 00 <mark>1</mark> 0 0010
3	0001	0000 0000 0000 0010	0000 0100 0010 0000

Contention checking architecture



Results and conclusion

Application description

Dijkstra: compute the shortest path

Sapp: Susan-corners, Susan-edges, LU, Water and Water-spatial

Experimental set up

- ○5 clust app: same apps as 5 app, each app uses 4 cores in parallel
- •Full HD: 150MHz video flow through 6 image processing IPs

Cons

Strong delay overhead with OCC strategy

Pros

- The NoC need a frequency increase to run unidirectional high throughput video application
- Area overhead of 21% per router

0.95 0.90 0.85 0.80 ි 0.75

Classic NoC CIC with CONT □ CIC with CONT+OCC □ CIC with OCC

- Cycle-accurate, bit-accurate NoC simulator Application traces extraction from MPSoCBench Hardware overhead considered NoC 4x3 clocked at 1GHz, XY algorithm
- ~65nm CMOS technology,
- Wires length of 2mm, 32 bits

Up to 67% of links energy saving

- Up to 35% of total energy saving
- Delay between computations exploited



Adapt the method to design a CIC router

	CIC architecture with OCC strategy				CIC architecture with CONT			CIC architecture with				
					strategy			CONT+OCC strategy				
	Links	Encoder	Extra	Processing	Links	Encoder	Extra	Processing	Links	Encoder	Extra	Processing
Application	energy	use rate	delay	throughput	energy	use rate	delay	throughput	energy	use rate	delay	throughput
	(%)	(%)	(cycles)	(%)	(%)	(%)	(cycles)	(%)	(%)	(%)	(cycles)	(%)
Dijkstra	-67.7	99.6	42	0	-61.5	66.5	18	-0.001	-59.5	62.9	13	0
5	-63.6	0/1 08	21	-0.001	-57 5	64.4	8	-0.001	-50.6	58	7	0
applications	-05.0		∠⊥	-0.001	57.5	04.4	0	-0.001	-30.0	50	/	U
5 Clusters	-63.2	78 /	25653	_27.8/	-62.3	62.5	177/11	_12 5	_31 2	36	17	-0.01
applications	-05.2	70.4 23033	-27.04	-02.5	02.5	TCCHT	-12,3	-31.2	50	±/	-0.01	
Full HD	-64.1	78	42477	-42.2	-57.2	88	29070	-29	-57.2	87.5	29070	-28.9