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# Proposal for combined conducted and radiated emission modeling for Integrated Circuit

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**Abstract** — This paper describes a methodology to build a combined conducted and radiated emission model for integrated circuits. The development of emission models of a FPGA extracted from two different approaches is presented and discussed. The first approach allows to build a predictable model from FPGA implementation and some passive measurement on FPGA device. The second approach allows to build a model from only NFS measurement. In conclusion, the accuracy of both models as well as the advantages and disadvantages are discussed.

**Keywords** — Integrated circuit; modeling; ICEM; conducted; radiated; emission; FPGA; Near field.

## I. INTRODUCTION

Several standards exist to build EMC model. The IBIS model is a standard for electronic behavioral specifications of integrated circuit input/output analog characteristics. This model is mainly used for the Signal Integrity simulation. The Integrated Circuit Immunity Model (ICEM) and the Integrated Circuit Emission Model (ICEM) proposed by the IEC62433 standard are oriented to describe both the immunity and emission behavior of Integrated Circuit (IC). So for each EMC issue, a specific model could be developed.

We propose in this paper a methodology to build a combined model to describe the conducted and radiated emission behavior of FPGA device in only one model. This approach is compared with a second proposal to build a radiated emission model from Near Field Scan (NFS) measurements. Given the complexity of the new IC generation, the NFS measurement helps to model highly complex behaviors.

In the remainder of this paper, the two proposed approaches are described and a final discussion is start on the advantages and disadvantages of using the two models.

## II. NEAR FIELD MEASUREMENT OF THE DEVICE UNDER TEST

The studied circuit is a FPGA Spartan 6 from Xilinx which includes 9152 configurable logic blocks and up to 186 user IOs divided in 4 banks with separated power supplies (see Fig. 9). It is mounted in a fine pitch BGA256 package. The FPGA

is clocked by an external 16MHz quartz oscillator connected to the input T8. Near Field Scan (NFS) measurements have been done with six different programs implemented in the FPGA device, as described by Table I. The activity rate, i.e. the number of internal resources used in the FPGA, and the number of switching IOs are changed to show their contribution to the near-field radiation.

TABLE I. PROGRAMM CONFIGURATION OF FPGA DEVICE

Activity rate	Configurations	
	With periodical switching of two I/Os at 8 MHz (T9 and C16)	Without IOs switching
20 %	“Config 20% IOon”	“Config 20% IOoff”
40 %	“Config 40% IOon”	“Config 40% IOoff”
90 %	“Config 90% IOon”	“Config 90% IOoff”

Fig. 1 presents the test board. The measurement frequencies start at 5 MHz and go up to 1.8 GHz. Two types of magnetic field probe are used: one for the Hx and Hy component and another for the Hz component. The spatial resolution of the probes is 0.5 mm. They have been calibrated according to the methodology presented in annex A of the IEC TS 61967-3 standard [3]. The signal captured by the probe is amplified with a 47dB low-noise amplifier and measured by a FSP R&S receiver. The probes are moved by a 3D scanner system at 2.5 mm above the top PCB surface (0.6 mm above the top of FPGA package). All the equipments are controlled by BAT-Scan software from Nexio.

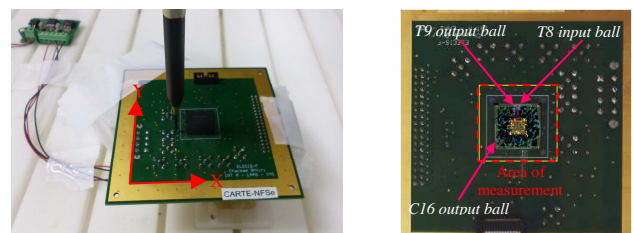


Fig. 1. Near Field measurement on FPGA board

Figs 2 to 4 present vertical magnetic field (Hz) maps measured with different configurations of the FPGA at different frequencies.

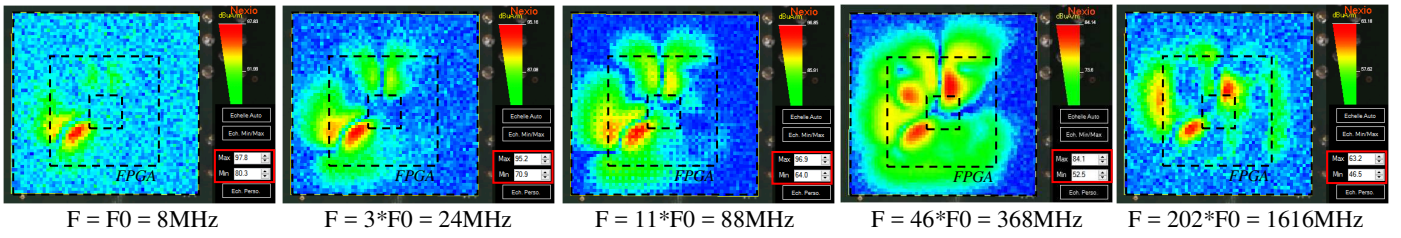


Fig. 2. Measurement of Hz component with configuration “Config 90% IOon”

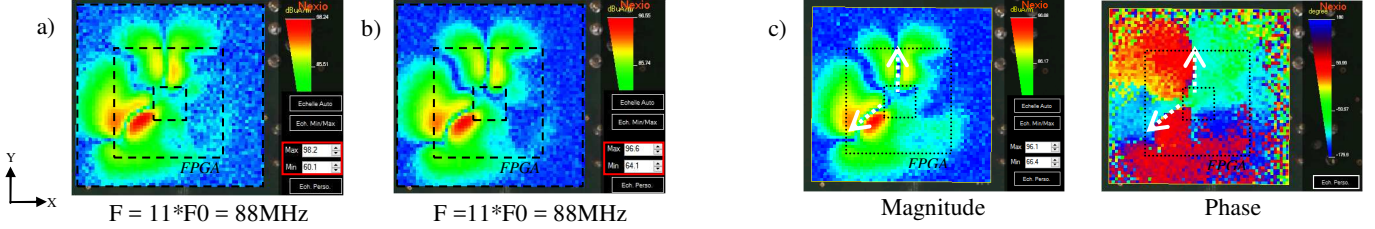


Fig. 3. Measurement of Hz component with configurations: a) “Config 40% IOon” b) “Config 20% IOon” c) “Config 90% IOon” at 72 MHz (vector)

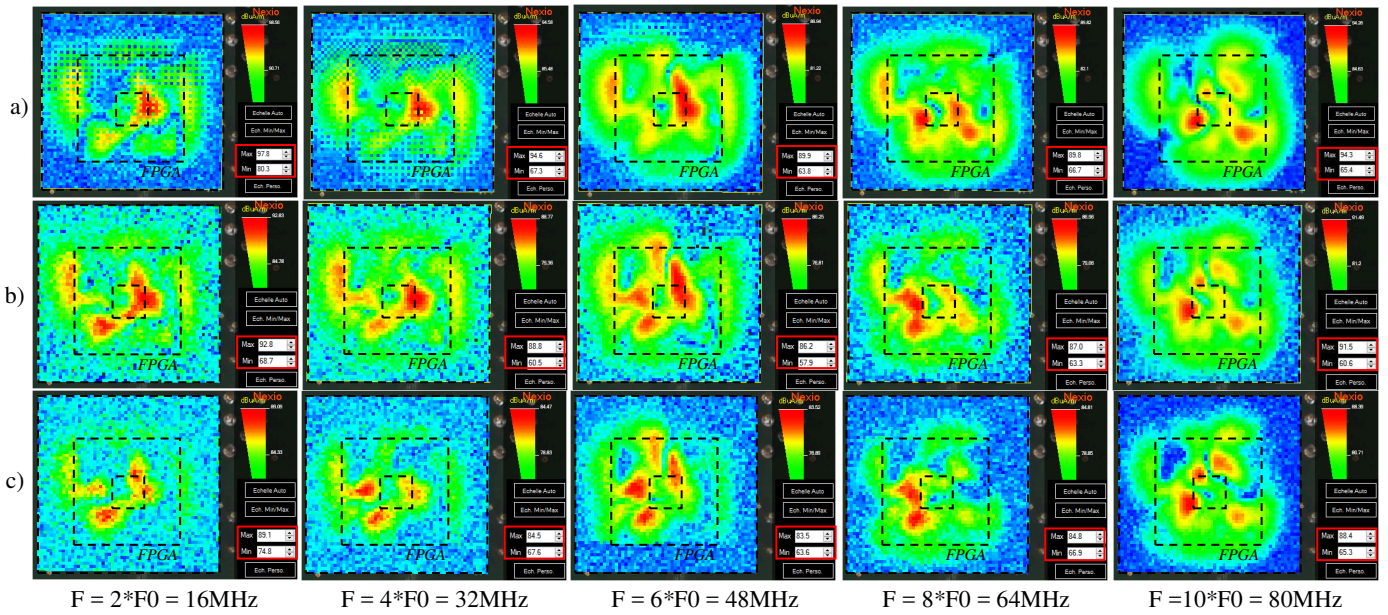


Fig. 4. Measurements of Hz component with configurations: a) “Config 90% IOon”, b) “Config 40% IOon”, c) “Config 20% IOon”

Three different activity areas are clearly visible on the near-field maps (see Fig. 10). The first area is above the input T8 and is related to the current that circulates along the input pin connected to the external oscillator. This activity is weak and often masked by other activities, but has a high frequency spectral content. The second area is due to the internal core activity of FPGA (see Fig. 4). The core activity is visible on IO connections and their power delivery banks (bank 2 for T8\_clk and T9\_out IOs and bank 1 for C16\_out IO). These two first areas produce emission at harmonic frequencies of 16 MHz. The last area is visible on the bottom left corner of the FPGA and is due to the switching of the I/O C16 (Fig. 2 and 3). It produces a significantly high emission at 8 MHz and its odd harmonics up to several hundreds of MHz.

The core activity emission is visible up to 100MHz. Above this frequency, only the IO activity is visible. Obviously, the magnitude of RE due to core activity is related to the activity

rate. The comparison between the near-field maps obtained with the different FPGA configurations presented in Fig. 4 shows a 3 dB attenuation between each program. A 6 dB attenuation is visible between the low (20%) and the high (90%) activity rate. The near-field emission produced by the IO activity is not affected by the activity rate used in the FPGA core, as shown in Figs. 2 and 3. This activity depends only of the internal IO driver characteristic and the external load connected to the IO.

All these information are very important to guide the development of the ICEM model. In the next paragraph, we will describe how to build an ICEM model of FPGA following different approaches.

### III. ICEM-RE MODEL

The conducted emission of an integrated circuit (IC) can be modeled according to the Integrated Circuit Emission Model for Conducted Emission (ICEM-CE) approach, standardized as IEC 62433-2 [1]. ICEM-CE proposes a generic model topology based on three main blocks.

The Power Distribution Network block (PDN) describes the propagation path of the transient current produced by the on-chip switching activity to the external part of device (pad or ball of the IC package). It consists of a passive element network and is often constructed from S-parameter measurements done between the power supply network terminals. The Internal Activity block (IA) is used to model the transient current produced by the digital and analog parts of the IC and its I/O buffers. It usually consists of current generators describing the different contributors to the internal activity of the IC. The noise produced by the switching of the IOs is called IA IO and can be modelled accurately by integrating an IBIS file. The last block is called Internal Block Connection (IBC). It is used to interconnect the IA and PDN blocks. It is often hidden in PDN block. Any changes in the internal configuration of device affects the IA block, the PDN is supposed to remain constant.

A new proposal, in 2016, defined the ICEM-RE standard for modeling Radiated Emission of IC [6]. The proposal describes a complete model based on dipole network extracted from NFS measurements. With this approach, the RE can be extrapolated at any farther distance from the IC very accurately. However, this model is completely separated from ICEM-CE and only representative of the configuration of the IC used during the NFS measurement. The influence of a change in circuit configuration, external loading or filtering cannot be predicted.

In this paper, we propose to build a common IC model for both conducted and radiated emission simulation. We proposed to add a new block for modeling the radiated emission to ICEM-CE model. The so-called Equivalent Antenna Network (EAN) block is connected to the PDN block. The EAN includes several wire network modeling the radiated emission due to the physical structure of package. All these equivalent dipoles are excited by the current predicted by ICEM-CE model. In the following parts, we present two approaches for ICEM-RE model construction. A final chapter discusses about the advantage and disadvantage of each proposed approaches.

#### A. Approach 1 : ICEM-RE model from ICEM-CE

In this approach the ICEM-CE model is reused to build the ICEM-RE model. The EAN block is added to model the radiated emission from package interconnects. All power and IO interconnects are modeled by thin wires. The current simulated by the ICEM-CE model is injected on each wires of the EAN block. The next paragraphs describes the approaches to extract all parts (IA, PDN, EAN) of this combined ICEM-CE/ICEM-RE model.

#### 1) PDN block extraction

The PDN block models the propagation path of current from IA generator to the PCB. An important part of the PDN is the modeling the IC package. Numerous papers such as [5] or [8] describe how to extract PDN model from S-Parameters measurements. This N-Port passive element model could be converted in Spice model or kept in Touchstone format depending on the used simulation software. In this paper, we reused PDN model developed in [5] for ICEM-CE of the tested FPGA. IA block extraction from FPGA information

The IA models the noise produced by the switching of the active logic blocks. It is constructed following the predictive approach proposed in [5]. It consists of a set of current source based on a simple waveform (e.g. triangular pulse). The amplitude  $I_0$  and the duration  $\tau$  of the pulse can be calculated when the dynamic power consumption, the toggle rate and the data path delay are known. Using the simulation tools of Xilinx, these parameters are estimated, and the characteristics of the equivalent current sources of the IA core can be deduced, as presented in the Table II for the different configurations of the FPGA core. The core activity is modeled by two current sources: one for the configurable logic block switching, the other for the clock tree.

TABLE II. ESTIMATED PARAMETERS OF IA CORE BLOCK ACCORDING TO THE ACTIVITY RATE OF THE FPGA

Activity rate	Logic cells activity		Clock tree activity	
	$I_0$ (mA)	$\tau_0$ (ns)	$I_1$ (mA)	$\tau_1$ (ns)
20 %	140	7,4	208	1,5
40 %	289	7,2		
90 %	482	10,8		

The same methodology could be used to extract equivalent current sources that models I/O switching. However, the IBIS model provided by the IC manufacturer offers a more accurate method to simulate the conducted noise produced by I/O switching. The power supply terminals of buffer models are connected to the PDN block of ICEM model. From SPICE simulations, the durations of the current pulses due to rising or falling transitions of an output buffer are 1.7 ns and 1.1 ns respectively.

Fig. 5. shows a comparison between the simulated external voltage using a  $1 \Omega$  probe in frequency domain for the 20% activity rate configuration with two switching output buffers. The simulated spectrum gives a good estimation of the generated harmonics. It shows a good correlation with the measured spectrum over a large frequency band.

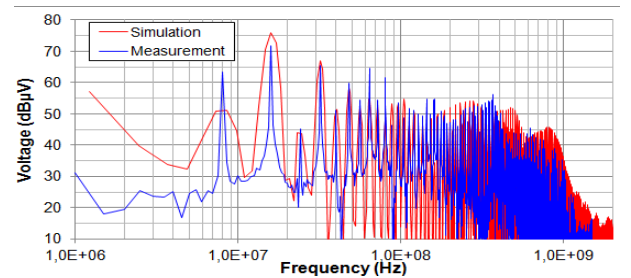


Fig. 5. IA measurement and simulation comparison for “Config 20% IOon”

## 2) EAN block extraction from FPGA information

Package interconnects are the main contributors of RE from ICs. They constitute a set of parasitic antennas excited by the transient current produced by IC core and I/O switching. The prediction of the RE from a circuit relies on the knowledge of the position of these antennas and the currents that excite them. The currents which flow along package interconnects can be simulated precisely from ICEM-CE model, if it includes an electrical model (e.g. as lumped RLC circuit) of these interconnects. Moreover, from an accurate geometrical model of the IC package, geometrical positions can be assigned to these interconnects, that form the source antennas of the IC radiated emission. With this geometrical coordinates assignation, an ICEM-RE model can be constructed from ICEM-CE.

A simple method to compute the electric and magnetic fields radiated by package interconnects is based on the thin wire approximation. Each interconnect is meshed into small elementary thin wires crossed by a current  $I$  that is supposed constant along the wire. This assumption remains valid until the interconnect length  $l$  is electrically short ( $l < \lambda/10$ ). The magnetic fields generated by each elementary wire oriented along  $z$  axis are calculated according to (1), where  $r$  is the distance to the observation point. If the package interconnect is longer than  $\lambda/10$ , it is split into elementary dipoles. The total magnetic field at the observation point is the sum of the contribution of all the elementary dipoles.

$$\vec{H} = \frac{1}{\mu} \nabla \times \vec{A} \quad (1)$$

With:

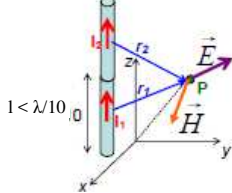
$$\vec{A} = \frac{\mu}{4\pi} \int_{-l/2}^{+l/2} I(z) \frac{e^{ij\beta r}}{r} dz \vec{z}$$


Fig. 6. Thin wire approximation for calculation of near-field emission from package interconnects

As described in Fig. 7, BGA package includes a build-up laminate substrate to route all die pads to the specific ball. This build-up laminate substrate is composed of traces, via and ground/power planes.

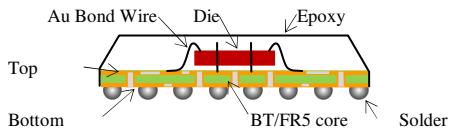


Fig. 7. Two-layer plastic BGA package

For reliability study, X-ray inspection is used to analyze the internal structure of IC packages. Fig. 8 shows the X-rays measurement of the FPGA.

From the X-Ray inspection and the pinout of FPGA, it is possible to build the PDN structure, identify the nature of the pin and finally associate a physical pin to an electrical element of the ICEM-CE model. In Fig. 9, all the power supply connections of the FPGA are drawn. The T8\_clk, T9\_out and C16\_out connections are marked in pink. The EAN block model built from this approach is presented in Fig. 14(a).

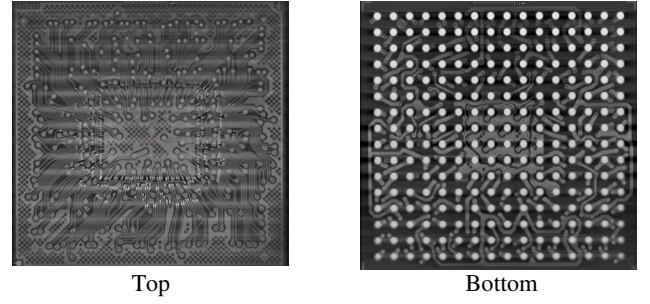


Fig. 8. 3D X-Ray view of FPGA (Spartan 6 family of Xilinx)

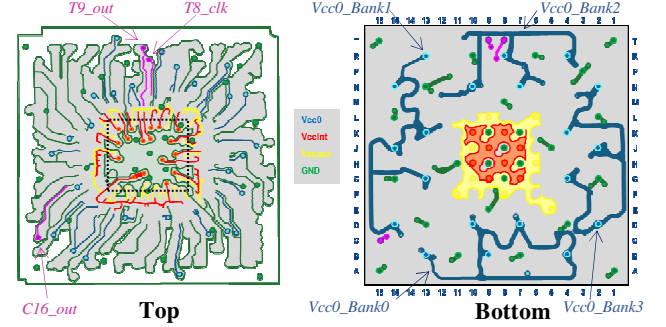


Fig. 9. PDN structure of FPGA (Spartan 6 family of Xilinx)

## B. Approach 2 : ICEM-RE model from NFS measurements

In this approach the ICEM-RE model is extracted from NFS measurement. IA block is built around several current generators modeling the different internal activity of FPGA. PDN block is not used in this approach. The EAN block of the model consists in several wires excited by IA generators.

### 1) IA block extraction from NFS measurements

The NFS measurements analysis allows to extract the radiated emission spectrum for various internal activity rate. Fig. 11 shows emission of internal activities versus the activity rate defined in the different FPGA configurations. Their RE spectra are picked in points marked in Fig. 10.

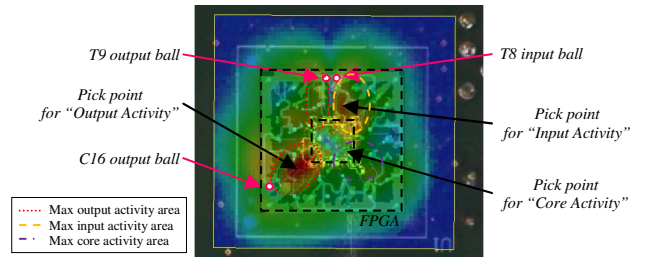


Fig. 10. Localization of magnetic field maxima at 0.6 mm above the FPGA package surface

The shape of the measured spectra is typical of the spectral envelop of repetitive trapezoidal pulse as presented in Fig. 12. The transient parameters (rise/fall time, pulse duration) can be estimated from the measured spectral envelop. The parameters extracted from the spectral envelop for radiated emission shape can be useful for defining the time domain parameters of each internal activities generator. The results are presented below in TABLE III.

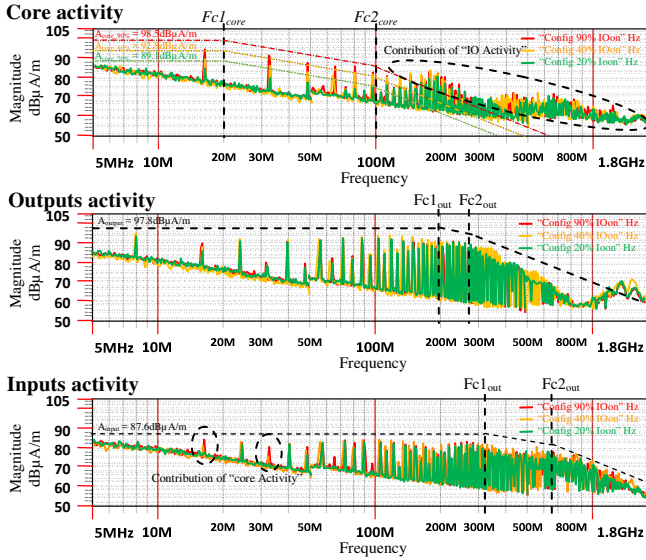


Fig. 11. Internal activities on measurement (HZ) vs activity rate of FPGA

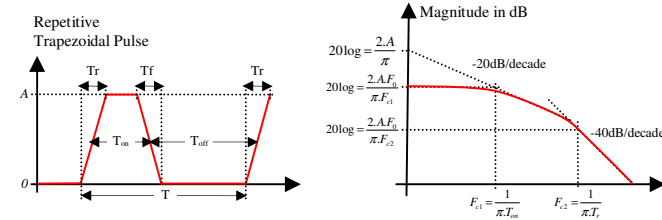


Fig. 12. Relation between trapezoidal pulse waveform and the envelop of its spectrum

TABLE III. ESTIMATED PARAMETERS OF IA CORE BLOCK EXTRACTED FROM NFS MEASUREMENT

Activity type	Frequency domain parameters				Time domain parameters		
	Htang  (dBμA/m)	F0 (MHz)	Fc1 (MHz)	Fc2 (MHz)	I  (mA)	T (ns)	Tr (ns)
Core <sub>90%</sub>	98.5	16	20	100	78	62.5	16
Core <sub>40%</sub>	92.8	16	20	100	41	62.5	16
Core <sub>20%</sub>	89.1	16	20	100	8.1	62.5	16
Input	87.6	16	310	550	6.4	62.5	1
Output	97.8	8	200	280	60	125	1.6

## 2) EAN block extraction from NFS measurements

The analysis of the near-field measurements shows some information that can be used to build EAN from wire elements. Fig. 13 shows vector radiated emission of wire (one dipole) for each Hx, Hy and Hz components. One dipole has a specific magnitude signature. The position of an isolated dipole can be localized with high precision from the Hz magnitude component. Coupling with the Hx and Hy components, the magnetic signature of a dipole can be help to build EAN block. Phase is also a precious information to localize the position and orientation of dipole. As shown in Fig. 13, the position of dipole is marked by a high variation of the H field phase ( $\pm\pi$ ). The sign of this variation defines the dipole orientation.

With this information, the analysis of near field measurement can help to build the EAN block. Fig. 3 shows

vector Hz near field scan for “Config 90% IOon” configuration measured at 72 MHz. Using the previous theory, two wires are clearly identified as illustrated in the Fig. 3(c).

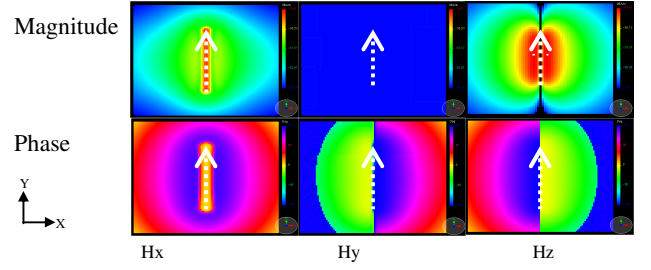


Fig. 13. wire simulation – Hx, Hy and Hz components in magnitude and phase

This PDN structure extraction method is relevant for simple package, for example for QFP package where all connections can be defined as a wire starting from the component center (the die) to the periphery of IC (the pad). Coupled with pinout of device, building the structure of the PDN is not a complex task. One wire is used to connect all balls with position of die pad for each interconnect which is taken into account. The EAN block model built from this approach is presented in Fig. 14(b).

## IV. SUMMARY ABOUT BOTH ICEM-RE EXTRACTION APPROACHES

We have described two different approaches to extract ICEM-RE model of an IC. The complexity level for both approach is different. As presented in Fig. 14, the EAN block of the full model extracted from Approach 1 (“model 1”) contains 178 dipoles where the EAN block of full model extracted from Approach 2 (“model 2”) contains only 76 dipoles. The “model 2” is a behavioral model resumed by the EAN block and activity generators. The “model 1”, presented in Fig. 15, described, with great precision, package and die of the device in SPICE format. Regarding the H field emission produced by the output buffer C16 switching (Fig. 16), both approaches give a good prediction of the radiated emission at 8 MHz. Simulations provide a correct prediction of the maximum H field and the overall distribution of the H field produced by C16 switching. Simulation at 16MHz is more difficult to validate due to low level of Output activity covered by the higher Core Activity visible on NFS measurements at this frequency. However, the simulation results confirm that the I/O switching does not contribute to the IC emission at 16 MHz. The final paper will provide more comparisons between NFS measurements and simulations with both modeling approaches.

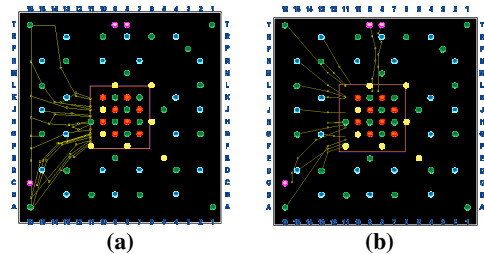


Fig. 14. EAN block models - (a) extracted from X-Ray (Approach1); (b) extracted from NFS measurement (Approach2)

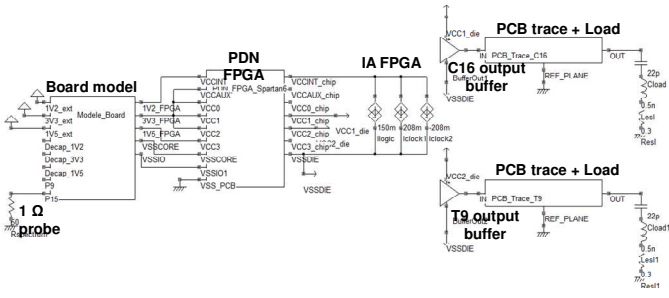


Fig. 15. ICEM-RE Model of FPGA from Approach 1 (Spartan 6 family of Xilinx) on IC-EMC software [6]

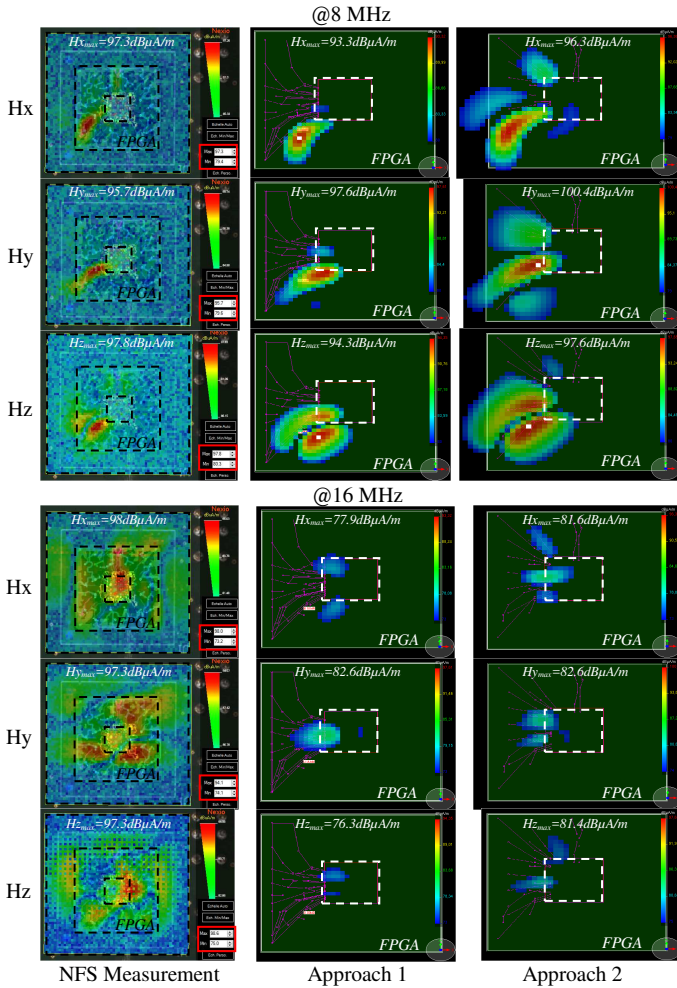


Fig. 16. Measurement (Config 20% IOon) vs. simulation (only C16 output buffer switching activity is taken into account)

## V. CONCLUSION

This paper has described two methodologies to build a radiated emission model for integrated circuits, which were tested on a FPGA. The first model describes very precisely the structure of the component. Information from FPGA development tool, S-parameters measurements and the X-ray inspection provides valuable information to build the structure of the model. No final application board is necessary to build a predictive model for various implementation of FPGA device. This model is very important to anticipate the EMC issues.

However this approach requires huge development work. Note that this model defined in SPICE format allows working at board level to optimize the design (e.g. signal integrity or decoupling capacitor network optimization) from to predictive numerical model of IC taking into account the specific user application behavior.

The second approach based on NFS measurement gives a simpler model. This model can be quickly built from NFS measurement on application board. Compared to the first approach, this one includes all unknowns relative to the electronic board fabrication process. But this approach needs a prototype to perform NFS measurement and is limited at one specific program implemented on IC. This model (as the "model 1") can be used to evaluate radiated emission in far field to improve EMC at system level.

We can conclude that both approaches are complementary and to summarize a large part of the EMC issues requiring to use an IC model.

## Acknowledgment

I would like to use some few lines to thank Continental Automotive France, Toulouse, for accepting to realize 3D X-Ray view of the FPGA.

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