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Methodology of modeling of the internal activity of a FPGA for conducted emission prediction purpose

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***Abstract*— This paper describes a new methodology of construction of the internal activity block of an ICEM-CE model of an FPGA based on a predictive approach using the estimation tools of the dynamic power and the static timing proposed by the manufacturer of the integrated circuit.**

Keywords*— *Integrated circuits; Internal Activity; Conducted emission; ICEM; FPGA, Dynamic power.

I. INTRODUCTION

The evolution of integrated circuits and their complexity through the increase of the number of transistors and the miniaturization of electronic components has a huge effect on the current density and the increase of parasitic emissions. Thus, there is a crucial need to construct EMC models to predict the noise generated by integrated circuits (IC). Existing standards propose EMC models for prediction of conducted emissions of IC, such as ICEM-CE (Integrated Circuit Emission Model – Conducted Emissions) known as IEC 62433-2 standard [1]. It is particularly adapted to IC end-user's needs about prediction of conducted emission (CE) at PCB level due to the switching of internal logic blocks (core) and IOs of ICs. ICEM-CE model is made of two main parts: the first one describes the switching or internal activity (IA) of the circuit, the second one the filtering effect brought by the die and package interconnects. In ICEM vocabulary, it is known as passive distribution network (PDN). The IA block mainly consists of a set of equivalent current sources that reproduces core and IO switching activity, although IO noise can also be accurately predicted by adding IBIS model to PDN block [2]. The construction of the IA block dedicated for core noise prediction remains a challenging task for IC end-users.

Several methods have been proposed for the construction of the IA block of the core. As suggested by the standard, it can be extracted from an inverse method based on the measurement of the external current flowing in the ground or power supply pins and the modelling of IC, package and PCB interconnects (PDN) [3]. The main drawback of this measurement-based approach is that the IA extraction result depends on the PDN measurement and is extremely sensitive to any measurement errors. The IA Core block can also be constructed from the simulation of the transistors netlist, the transistor model library and the standard cell models [4][5][6]. However, this approach requires considerable simulation time and relies on unavailable data for IC end-users.

The IA block may be estimated from basic technological information about the technology and IC characteristics (e.g. CMOS technological node, number of logic gates, die surface…), for example with tool like ICEM expert module in IC-EMC software [7]. The IA is estimated roughly from the floorplanning definition of the circuit or without exact information about the circuit, but the main drawbacks of this approach are the precision and the lack of consideration of the actual IC configuration made by the end-user (hardware or software).

For some IC families such as programmable hardware device (e.g. Field Programmable Gate Array (FPGA)), design tools provide to the end-users accurate estimation of the average dynamic power estimation from post-placement and routing simulations of a given configuration. Moreover, some advanced FPGA design tools are able to determine the instantaneous dynamic power consumption from a vector-based simulation, which allows the calculation of the time-domain profile of the dynamic current consumption and thus a precise extraction of IA core block [8]. However, this type of approach requires long simulation times, whose results are dependent on the input test vectors. To overcome this issue, we propose to estimate the IA block of a FPGA from vectorless power estimation and static timing analysis applied on post-placed and routed design. Compared to the vector-based approach, this solution is able to provide a good estimation of the IA block in a very short time, without additional steps in the FPGA design flow, and from a reduced set of data. Moreover, the proposed approach is able to take into account the random activity of the circuit. The proposed method can be applied by any FPGA end-user. Furthermore, it could be adapted to any circuit by extracting the IA parameters by measurements.

In this paper, the methodology of construction of the IA block of a FPGA (XC6SLX16-FT256 Spartan 6 from Xilinx) is presented, and validated through several case studies. Its accuracy is evaluated through comparison between measurements and simulations of the CE. The first chapter is devoted to the presentation of the methodology of construction of the IA core block. Secondly, the case studies are exposed.

Finally, the last chapter is dedicated to the validation of the methodology through the different case studies.

II. Internal Activity Construction Principle

The CE of a synchronous digital circuit is related to the instantaneous current consumption, i.e. the charge transfer from the power supply to internal logical gates synchronized by a clock signal. A straightforward approach to model the source of IC CE relies on one or several current sources connected to an equivalent model of the power distribution network of the circuit that filters the noise produced by the circuit switching activity. This is the approach proposed by ICEM standard to model the CE produced by an IC: the equivalent current sources belong to a block called Internal Activity (IA) while the power delivery network forms the block Passive Distribution Network (PDN). The relevance of the model depends on:

- The accuracy of the PDN block. This block is supposed independent of the instantaneous activity of the circuit. Numerous publications present reliable methods to extract a model of a circuit PDN so that we consider that the PDN is known in the following paragraphs.
- The accuracy of the IA block. Multiple variable parameters affect this block, such as the clock frequency, the power supply voltage or the internal activity of the circuit.

Before presenting our methodology of extraction of the IA block for FPGA circuit, a preliminary question is: is it necessary to determine precisely the time-domain waveform of the instantaneous current consumption to obtain an acceptable CE prediction? In the next paragraphs, we will show that it is not necessary and only two criteria must be respected to obtain a reliable prediction of CE.

A. *Influence of the instantaneus current consumption waveform on emission spectrum*

In digital synchronous circuits, current consumption appears mainly during transitions from logical state 0 to 1. Thus, the time domain profile of the instantaneous current is a periodic series of short pulses; its period is equal to the clock period Tc. As explained in [8], the power supply noise can be predicted if the charge consumed at each clock transition is determined correctly. The waveform of the current i(t) delivered by the IA block must reproduce this charge quantity, given by:

$$q = \int_0^{\tau} i(t)dt \tag{1}$$

Where q is the transferred charge during a clock cycle and τ is the duration of the charge transfer or the current pulse. Moreover, to reproduce the CE spectrum, the duration τ of the charge transfer must be also known. In order to illustrate this principle, let consider the three basic periodic pulsed waveforms presented in Fig. 1, which model the dynamic current consumption of a digital circuit. The clock frequency is 10 MHz. The pulse durations are identical; their amplitudes are chosen such as the transferred charge is identical. These current waveforms are generated by a current source and form an IA block which is connected to the PDN block representative of a large digital IC. The voltage across a 1 Ω resistor connected to the Vss pins of the circuit is simulated for each waveform. Fig. 2 presents a comparison of the simulated voltages using the different waveforms in frequency domain. In spite of some differences in high frequency (around the nulls of the spectral envelop), the envelopes of the spectra are very close, providing nearly identical estimation of the CE noise.

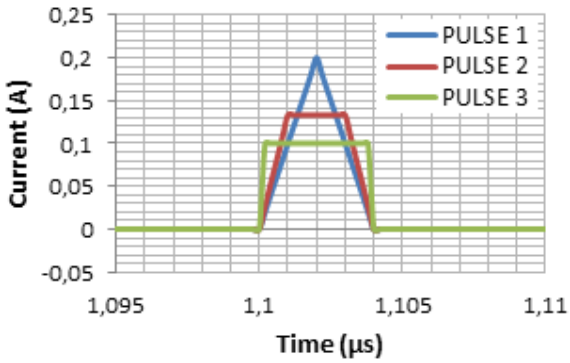

Fig. 1. Three basic pulsed waveforms to model the dynamic current consumption of a circuit

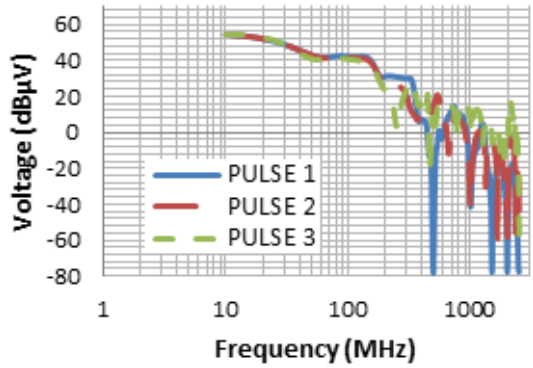

Fig. 2. Comparison between the simulations using the different shapes of IA with a 1 Ω probe

Whatever the waveform of the instantaneous current consumption, if the transferred charge and transfer duration are respected, an acceptable estimation of the CE can be obtained. This is the purpose of our methodology.

B. *Presentation of the IA construction methodology for a FPGA circuit*

The charge quantity transferred at each clock cycle can be determined from measurements or the evaluation of the average dynamic power consumption P_{dyn_avg} by a design tool. It is given by (2):

$$P_{dyn_avg} = F_C \sum_{i=1}^{N} \alpha(i) q_L(i) \cdot V_{DD} \tag{2}$$

where N is the number of internal logical nodes or signals in the circuit, α(i) is the average number of transitions on signal i per clock cycle (toggle rate), $q_L(i)$ is the quantity of the charge associated to signal i, V_{DD} is the power supply voltage and F_C is the clock frequency of the circuit. For the Spartan 6 family of Xilinx, the manufacturer puts in the ISE software the module Xilinx Power Analyzer (XPA) which gives a detailed estimation of the power consumption in the clock tree, the signals and logic blocks, and the IOs after a post-placement and routing simulation. XPA also gives a vectorless estimation

of the toggle rates and average dynamic power of all the internal logic signals. From these estimated parameters, the average quantity of charge transferred during a clock cycle Q_L can be calculated. For each clock period T_C, the internal activity produces the same quantity of the charge as given by the formula (3), where I_{avg} is the average dynamic current consumption.

$$Q_L = \sum_{i=1}^{N} \alpha(i) q_L(i) = I_{avg} \cdot T_C \tag{3}$$

ISE Xilinx tool performs a static timing analysis which gives a detailed report about the slack and the data path delays at the fast and slow PVT (Process/Voltage/Temperature) corners. For the construction of the IA, the pulse duration τ is considered to be the median value of the interval whose boundaries are the maximum data path τ_{max} and the minimum data path τ_{min} given by the static timing report (4). The average dynamic current associated to a periodic pulsed waveform i(t) is calculated using (5).

$$\tau = \frac{\tau_{\max} + \tau_{\min}}{2} \tag{4}$$

$$I_{avg} = \frac{1}{T_C} \cdot \int_0^{\tau} i(t) \cdot dt \tag{5}$$

In the next paragraphs, we consider that the dynamic current consumption waveform is a symmetrical triangular pulse. The peak amplitude of the pulse I_{max} is given by (6).

$$I_{\max} = 2 \cdot I_{avg} \cdot \frac{T_C}{\tau} \tag{6}$$

From the resolution of the equations (3), (5), and (6) the maximum amplitude of the IA is calculated using the formula (7). Fig. 3 summarizes the steps to get the required data from a FPGA design tool to solve the equation (7), which leads to the IA construction.

$$I_{\max} = \frac{2.P_{dyn_avg}}{F_C.\tau.V_{DD}} \tag{7}$$

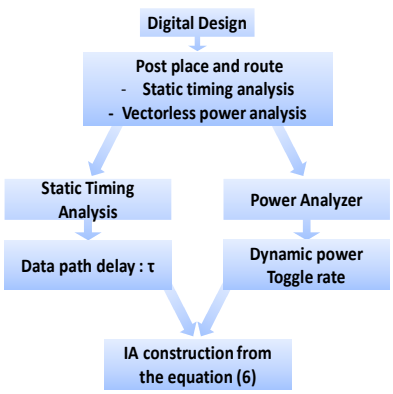

Fig. 3. Construction workflow of the Internal Activity block for FPGA circuit

The proposed workflow of construction of the IA is based on the average dynamic power consumption, hence, the approach proposed is deterministic; the amplitude of the IA is constant at each clock cycle. In practical cases, the IA profile is random due to the variation of the toggle rate and the power consumption of the active logic blocks. Thus, the peak-to-peak amplitude of the IA in the time domain could be under estimated and the envelope of the emission spectrum inaccurate. In the next part, an alternative approach is proposed for the construction of a random IA.

C. Statistical method for construction of a random IA

The construction of a random IA block is possible with a vector based simulation [8] but this may require long simulation time. However, the power analysis tool XPA gives the switching probability of each logic block of the circuit. The variability of the switching activity around its mean value can be estimated in a short time simulation. For the construction of a random IA, a methodology based on the statistical distribution of the transferred charge per clock cycle is proposed.

XPA tool gives a detailed report about the dynamic power consumption and the toggle rate for the routed signals and the logic blocks. With these data, it is possible to calculate the probability density function (pdf) of switching of each logic block of the circuit and thus the pdf of the transferred charge to each logic block per clock cycle. Although the logic states of each logic block are partially dependent, we neglect these interdependencies since they cannot be determined through the vectorless estimation of XPA. Considering that each logic block of the circuit switches independently from the others, the pdf of the transferred charge to the circuit is the convolution product of the pdf of the transferred charge of each logic block and the toggle rate. Statistical parameters such as the average and standard deviation can be calculated, and the most representative statistical law can be determined. In practice, due to the large number of switching logic nodes, the distribution tends to be Gaussian. Under this assumption, the probability that a logic block i transfers a charge quantity q(i) per clock cycle is given by the toggle rate α(i). Hence, the average transferred charge quantity $\overline{q}(i)$ for each logic block is calculated using the equation (8). Considering the charge quantity q(i) as a random variable, the expected variance σ_i^2 is given by the formula (9), allowing the calculation of the pdf of each logic block i, where N is the number of logic states, for a binary case N=2.

$$\overline{q_L}(i) = \alpha(i) \cdot q_L(i) \tag{8}$$

$$\sigma_i^2 = \sum_{j=1}^{N} \alpha(j) \cdot \left(q_L(j) - \overline{q_L}(i)\right)^2 \tag{9}$$

The pdf of the transferred charge to the circuit follows the normal distribution $N(Q_L, \sigma^2)$, where Q_L is the average transferred charge quantity (10) and σ^2 its variance (11).

$$Q_L = \sum_{i=1}^{N} \overline{q_L}(i) \tag{10}$$

$$\sigma^2 = \sum_{i=1}^{N} \sigma_i^2 \tag{11}$$

Finally, in order to generate a SPICE compatible IA source, a series of random charge quantity Q(k) is generated at

each clock cycle according to the previous pdf. Considering a symmetric triangular pulse, the amplitude $I_{\max}(k)$ of the IA is given by the expression (12), where k is the number of generated points. The IA is then modelled using a current source based on PWL file. Fig. 4 summarizes the approach of construction of the IA using the statistical distribution.

$$I_{\max}(k) = \frac{2 \cdot Q(k)}{\tau} \tag{12}$$

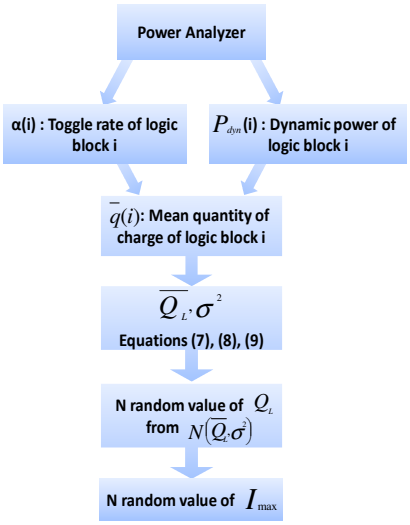

Fig. 4. Workflow of the IA construction using the statistical approach

III. Presentation of the Case Studies

A. The circuit under test

The circuit under test is a XC6SLX16-FT256 Spartan 6 Xilinx FPGA, manufactured with a CMOS 45-nm process. The circuit includes 9152 configurable logic blocks (CLB) and up to 186 user IOs, it is mounted in a Fine pitch Thin Ball Grid Array 256 balls (FTBGA256). The internal structure of this component is complex; it comprises six different power supply planes: V_{CCINT} dedicated to the CLB (1.2 V), V_{CCOx} (x = 1 to 4) dedicated to the I/O organized in four banks (3.3 V), and V_{CCAUX} dedicated to the JTAG configuration (3.3 V), and a ground plane for the VSS pins.

B. Description of the test board

A specific test board has been designed for the external voltage measurements and the validation of the constructed Internal Activity. It consists of a six layer board with complete power and ground planes in a 10x10 cm format for radiated emission measurements in TEM cell. Several test points have been placed for CE measurements and characterization of the board impedance. A 1 Ω probe, as defined by the IEC 61967-4 [11], has been placed between the ground pins of the FPGA and the ground reference of the test board in order to measure the return current flowing outside the circuit. Models of the PDN of the FPGA and the test board have been constructed from S parameter measurements and electromagnetic simulations and validated previously [3].

C. Configurations

The construction of a predictive internal activity of the FPGA is performed for a given activity. The workflows presented in part II are verified for different case studies of basic synchronous digital designs. . The clock frequency is set to 16 MHz for the different case studies. Fig. 5 shows the structure of the first case study: a delay line. For optimum dynamic power consumption, 90 delay lines have been cascaded in series, each delay line has N = 100 inverters. Due to its regular structure, its dynamic power consumption is deterministic; i.e. the number of switching gates remains identical at each clock transition.

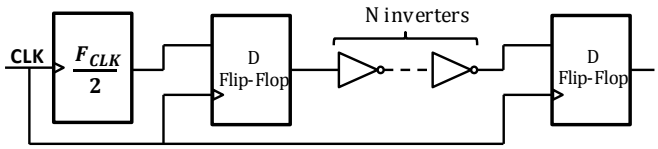

Fig. 5. Structure of a delay line

As another validation case, the 7-bits counter is a good example of synchronous circuit for which the internal signals present different toggle rates. In this case, 800 7-bits counters have been cascaded in parallel. For the different cases, no output buffer is switching, hence, the 1 Ω measurements and simulations shows only the contribution of the internal logic blocks and the clock tree activity of the FPGA. Table 1 summarizes the dynamic power consumption, data path delay and the average toggle rate collected from the estimation tools of Xilinx.

TABLE I. Estimated parameters for the different configurations

Configuration	Dynamic Power (mW)		Data path delay (ns)		Average toggle rate (%)
	Logic	Clock	Logic	Clock	
Delay Line	24	1,5	40	0,75	100
7-bits counter	9,60	1,5	3,8	0,75	28,35

IV. Construction of the Internal Activity Block

A. Case study 1: delay line

The first case study (delay line) has a toggle rate of 100 % because all the signals are switching at the rising edge of the clock. The clock tree presents non-negligible dynamic power consumption, its toggle rate is about 200 %, and hence, the signals representing the clock tree consumes energy at both rising and falling transitions of clock signal. Therefore, the internal activity of the clock tree is separated from the internal activity of the signals and the logic blocks. As shown in Fig. 6, two current sources are used to represent the activity of the clock, and one current source represents the activity of the signals and logic blocks. The IA waveform is supposed as a symmetric triangular pulse. The parameters are calculated from the resolution of the equations given in the previous chapter.

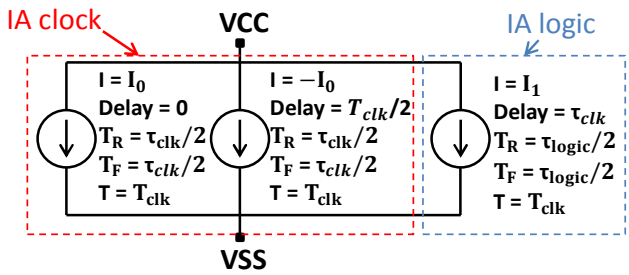

Fig. 6. Internal Activity of the core block

The constructed internal activity block is combined to the PDN and the board equivalent model. A transient simulation using ADS is performed to simulate the CE produced by the FPGA and measured through a 1 Ω probe. The time-domain simulation and measurement results are compared in Fig. 7. The simulated peak-to-peak amplitude of the voltage fluctuation is equal to 9 mV and presents a good correlation with the measured amplitude equal to 11 mV.

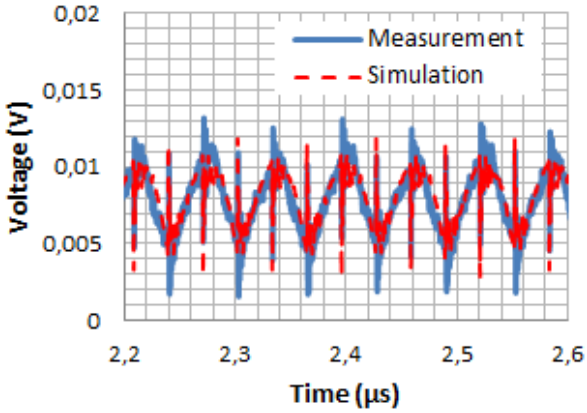

Fig. 7. Comparison between the measured and simulated external voltage using a 1 Ω probe in the time domain generated by the delay line configuration

Fig. 8 shows a comparison between the measured and simulated external voltages with a 1 Ω probe in the frequency domain. In general, the comparison presents a good correlation between the measured and the simulated spectrum with a RMS error of 5,15 dB. Simulation predicts that the frequency content of CE falls down above 1.2 GHz. This is confirmed by measurements.

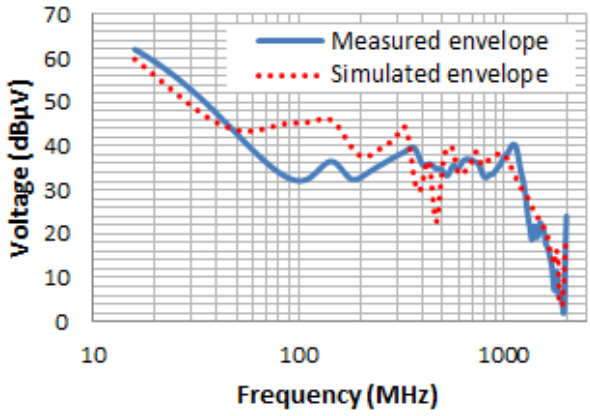

Fig. 8. Comparison between the measured and simulated external voltage using a 1 Ω probe in the frequency domain of the delay line configuration

B. Case study 2: 7-bits counter

1) Modelling with the deterministic approach

The case of the 7-bits counter is particularly different from the previous case. The signals representing every bit of the counter have different toggle rates. Firstly, the IA is constructed following the deterministic approach. Fig. 9 presents a comparison between the measured and simulated external voltage using a 1 Ω probe in the time domain. The simulated peak-to-peak amplitude of the voltage fluctuation reaches 13 mV and is underestimated compared to the maximum measured peak-to-peak amplitude of 21 mV because we consider that the instantaneous transferred charge at each clock cycle is constant and equal to the average transferred charge per clock cycle. However, if the activity is random, the instantaneous transferred charge varies around the average value.

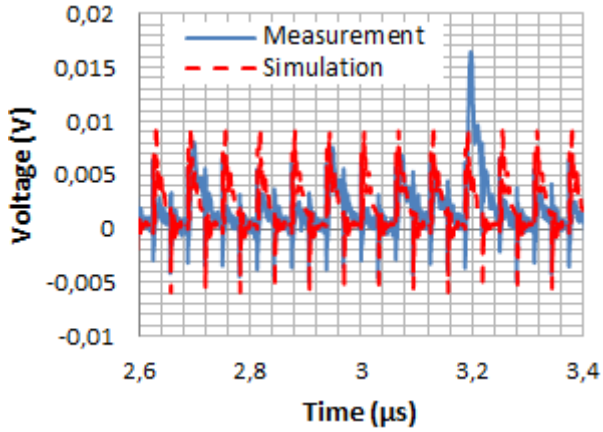

Fig. 9. Comparison between the measured and simulated external voltage using a 1 Ω probe in the time domain of the 7-bits counter configuration using the deterministic approach

Fig. 10 presents the Fast Fourier Transform (FFT) of the previous comparison. The sub-harmonics of the clock frequency are not represented, but globally, the simulated CE shows a good correlation with the measurement, the RMS error is 5,19 dB.

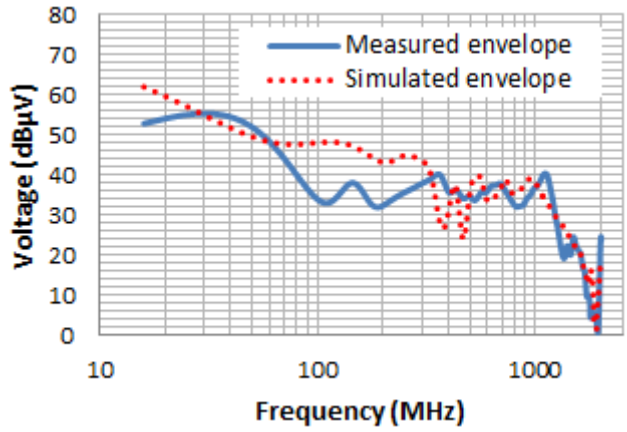

Fig. 10. Comparison between the measured and simulated external voltage using a 1 Ω probe in the frequency domain of the 7-bits counter using the deterministic approach

2) Modelling with the random approach

In this part, a random IA is constructed from the approach based on the statistical distribution for the case of the 7-bits counter. Fig. 11 shows the simulated and the measured external voltages using a 1 Ω probe. The simulated maximum peak-to-peak amplitude of the voltage fluctuation of 22 mV allows the prediction of the maximum peak-to-peak amplitude of 21 mV with a good precision. In general, the simulated time domain profile reproduces the random character of the CE with a good approximation when the statistical method is used to construct the IA.

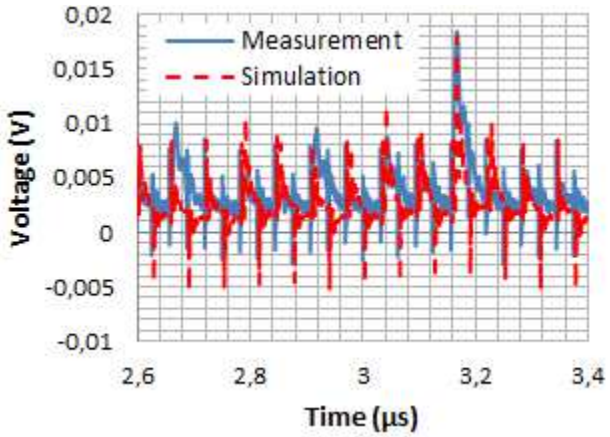

Fig. 11. Comparison between the measured and simulated external voltage using a 1 Ω probe in the time domain of the 7-bits counter using the random approach

Fig. 12 presents the comparison of the measured and simulated external voltages using a 1 Ω probe in the frequency domain. Not all the harmonics produced by the configuration are represented in the simulation, but an energy gain is visible bellow the clock frequency. Overall, the envelope of the simulated CE shows a good correlation with the measured envelop. The RMS error in this case is about 4,86 dB.

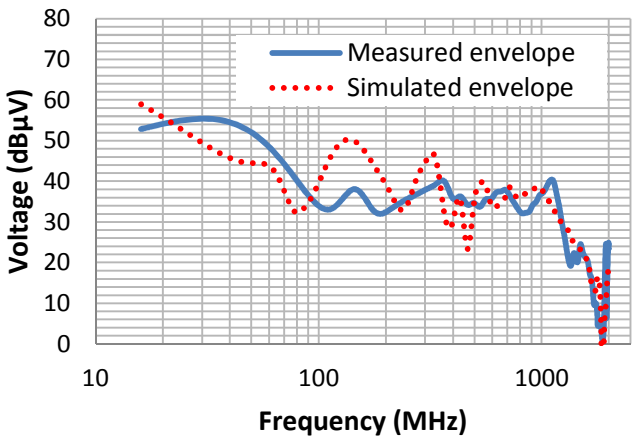

Fig. 12. Comparison between the measured and simulated external voltage using a 1 Ω probe in the frequency domain of the 7-bits counter using the random approach

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V. Conclusion

In this paper, a new methodology of construction of the IA block for ICEM-CE model of FPGA circuits has been presented. The main idea is that whatever the internal dynamic current waveform is, the simulated conducted noise will not vary much if the transferred charge and the pulse duration are determined correctly. Also, the dynamic current of an integrated circuit depends mainly on three parameters: the dynamic power consumption, the toggle rate and the clock and data path delay. Using the estimation tools given by the manufacturers of FPGA, these parameters can be extracted rapidly and without extra steps in the FPGA design flow, and allow the modelling of the IA following two different approaches: The deterministic approach and the random approach. Different validation cases have been discussed and generally the comparisons between the measured and simulated CE spectrum present a RMS error calculated for the clock harmonics less than 6 dB, and globally the envelope of the spectrum is predicted with a good approximation. This error can be related to the extraction of the PDN block of ICEM-CE model, the assumptions of our proposed methodology and to measurement accuracy. Future works will be carried out to better evaluate the intrinsic error of the proposed method.

The methodology presented in this paper is adapted to FPGA and other integrated circuits when the manufacturer provides power and delay estimation tools to IC end-users. On the other hand, the principle is still adapted to ICs when the manufacturers do not provide estimation tools but the needed parameter should be extracted from the measurement. This methodology can be proposed within the ICEM standard as user guidelines.

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