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Statistical Methods Applied to CMOS Reliability Analysis - A Survey

Hao Cai, Jean-François Naviner, Hervé Petit
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1 Introduction

The design of integrated circuits (ICs) and systems in sub-90nm CMOS technology is very challenging [1]. The scaling down of technology not only caused an unbalanced relationship between supply voltage and transistor threshold voltage (V_{th}), but also induced ageing effects and variability problems [2, 3]. In semiconductor manufacturing, systematic and random variations exist during different fabrication steps. Moreover, once ICs are fully functional, both ageing and variability degrade ICs performance and lead to uncertainty performance distribution. In this paper, we analysis process variations based on BSIM4 transistor model.

1.1 Traditional methods

From the perspective of designers, in order to know the variability and yield information, One traditional method is to setup guardband with worst-case corner-based analysis. In SPICE-like simulator, NMOS and PMOS type transistors are defined with letter acronyms (F: fast, S: slow and T: typical). For example, NMOS and PMOS transistors with low oxide thickness (T_{ox}), threshold voltage (V_{th}) is represented with 'FF' type (fast NMOS, fast PMOS). The other widely applied method is Monte-carlo analysis (see Figure 1). The performance distribution can be evaluated through a large amount of simulations.

However, traditional methods have limitations. The corner-based analysis with one standard case (type 'TT') and four extreme ones (type 'FF', 'FS', 'SF' and 'SS') evaluates circuit variability at the risk of over-estimation. The intrinsic accuracy of MC analysis is achieved with repeatedly simulations. Due to these drawbacks, statistical methods have been proposed to have an efficiency-accuracy tradeoff during variability assessment.

1.2 Current research and highlight

Over a period of last ten years, statistical modeling of CMOS variability has been continuously concerned both from academic research and industry manufacturing. Figure 1 shows the approximate number of publications from IEEE digital database every year. A state-of-the-art summary of this topic is presented in this subsection. According to the International Technology Roadmap for Semiconductors (ITRS) report 2011 edition, continuously CMOS technology scaling down results in increasing process variations.

2 Statistical analysis of CMOS variability

In this section, statistical CMOS variability is studied based on BSIM4 model. BSIM4 model is a physics-based, accurate, scalable, robust and predictive MOSFET SPICE model for circuit simulation and CMOS technology development. The impact of process variation at physical level can be investigated.

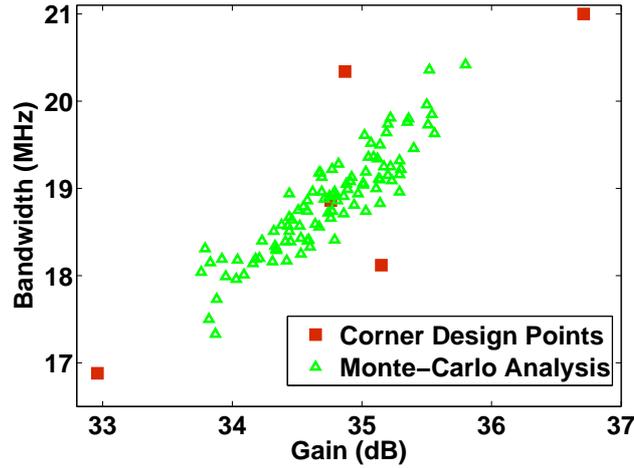


Figure 1: A comparison between MC and corner analysis on an Op-amp, performance parameters: DC gain and Gain-bandwidth (GBW)

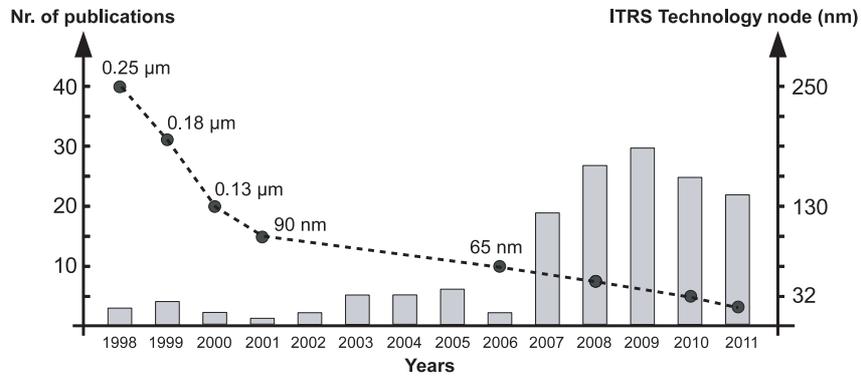


Figure 2: Approximation IEEE publications in the field of statistical CMOS variability, ITRS technology node 45 nm (2008), 32 nm (2010), 22 nm (2011)

2.1 Design of experiments

Design of experiments (DoEs) is an information-gathering procedure in statistical analysis. In CMOS circuits and systems design, the purpose of statistical DoEs is to help designers to characterize the impact of the input factors on the output parameters []. We can use it to select and compare process factors (e.g.,BSIM4 parameters) and predict objectives (e.g.,performance parameters). Figure 3 illustrates the detail steps of DoEs. Table 1 shows common applied DoEs in screening and prediction.

DoEs provide several solutions to generate experimental designs for various situations. Commonly used design are the two-level full factorial (contains all combination of different levels of the factors) and the two-level fractional factorial design (with a fraction such as $\frac{1}{2}$, $\frac{1}{4}$ of the full factorial case, or other type, e.g.,Plackett-Burman (PB) designs, central composite designs (CCD)).

	$2 \leq \text{Number of factors} \leq 4$	Number of factors ≥ 5
Screening	Full factorial, fractional factorial	Fractional factorial, Plackett-Burman
Prediction	Central composite, Box-Behnken	N/A

Table 1: Different DoEs used in screening and prediction

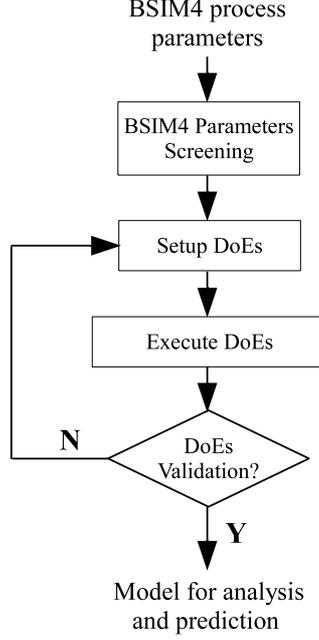


Figure 3: DoEs flow: parameter screening, DoEs setup and performance prediction

2.1.1 Parameter screening technology

Screening is used to minimize the number of process parameters. Correlation analysis and stepwise regression analysis (execute by Plackett-Burman design) are discussed in this subsection. More than 800 process parameters exist in BSIM4 model (version 4.5). As shown in Figure 4, the total number of parameters in Part C and D is 39. Screening analysis is implemented with:

- Correlation analysis filters out correlated BSIM4 parameters.
- Stepwise regression analysis (Plackett-Burman design) determines the significant order of left BSIM4 parameters.

Correlation refers to the linear dependence between two variables (or two sets of data). In statistical BSIM4 parameter modeling, correlation analysis is used to filter out correlated BSIM4 parameters. The correlation coefficient ρ_{B_i, B_j} between two BSIM4 parameters B_i and B_j with expected values μ_{B_i} , μ_{B_j} and standard deviations σ_{B_i} and σ_{B_j} is defined as:

$$\rho_{B_i, B_j} = \frac{cov(B_i, B_j)}{\sigma_{B_i} \sigma_{B_j}} = \frac{E[(B_i - \mu_{B_i})(B_j - \mu_{B_j})]}{\sigma_{B_i} \sigma_{B_j}} \quad (1)$$

where E is the expected value operator, cov means covariance. If ρ_{B_i, B_j} is +1 or -1, the selected two BSIM4 parameters show a positive (-1 with negative) linear dependence to each other. One of these two BSIM4 parameters can be moved out from model. After correlation analysis, a design of experiments (DoEs) should be selected to verify this new model. To simplify this model, stepwise regression analysis can be applied, results such as p-value from hypothesis testing are evaluated to determine the significant sequence of left BSIM4 parameters.

Stepwise regression is used to further minimize the BSIM4 process parameters. According to Table 1, A two level Plackett-Burman design is selected to execute stepwise regression. Hadamard matrix can generate an orthogonal matrix for input parameters whose elements are all either plus signs or minus signs (Plus signs (+) represent factors with maximum values; minus signs (-) for minimum values). In this case (see Table 2), only 12 runs are needed with Plackett-Burman designs. A full factorial design would require $2^{11} = 128$ runs.

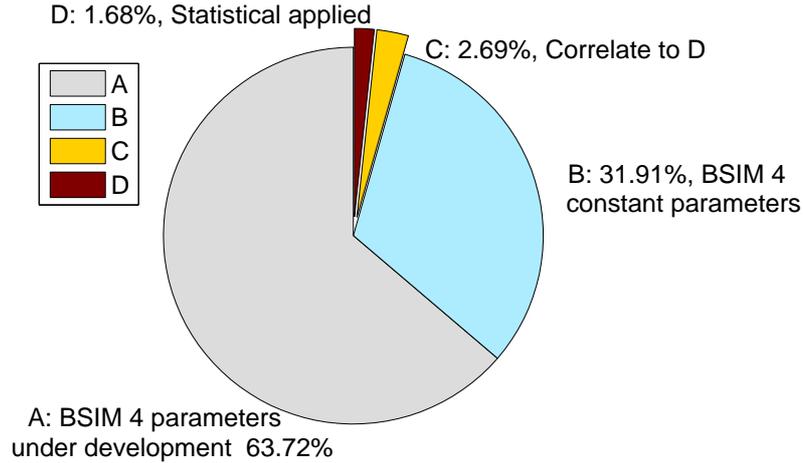


Figure 4: The total number of BSIM4 parameters is 893, some parameters (Part A) are still under development (currently equal to 0 or set to NaN), Part B represents constant BSIM4 parameters which are not influenced by process variations. BSIM4 parameters in Part C and D are proceeded with screening analysis.

In detail, stepwise regression is to build regression models between BSIM4 process parameters (input factors) and performance parameters (objectives) which can make hypothesis testing for models and every independent input factors. The p-value, partial F-values and R^2 value can be used to set a certain threshold to test the hypothesis of regression model. At each step, the p value of an F-statistic is computed to test models with or without a potential BSIM4 parameter. If a parameter is not currently in the model, the null hypothesis is that the parameter would have a zero coefficient if added to the model. If there is sufficient evidence to reject the null hypothesis, this parameter is enrolled. Conversely, the parameter is removed from the model. Finally, the most optimum regression equation is built with the most significant BSIM4 parameters.

2.1.2 Performance prediction with RSMs

Response surface method (RSM) is another important statistical method to build relationship between input factors (BSIM4 process parameters) and objectives (circuit performance). According to BSIM4 factors distribution, experimental runs are performed with circuit simulator. Central composite design (CCD) is a type of factorial factorial design can be applied to RSMs. CCD such as circumscribed (CCC), inscribed (CCI) and face centered (CCF) are different in range and rotation of factors. Figure 5 illustrates the distribution of different CCDs with two design factors. Besides three types CCDs, the Box-Behnken design (BBD) is an independent quadratic design which does not contain an embedded factorial or fractional factorial design. Since BBD does not have any combination point at some corner, some applications can benefit from it and avoid some extreme cases.

The simulated performance parameter is used to generate RSMs with BSIM4 parameters [4]. The response surface model can be used for displaying graphically the mathematical model between BSIM4 process parameters and circuit performance. Successive building of RSMs can help designers estimate varied and aged circuit performance efficiently. Sometimes, using linear model is hard to achieve adequate accuracy because of exponential complexity, quadratic model or even cubic model is required. The accuracy of RSMs can be evaluated by root-relative-square error (RMSE). It is a measurement for differences between model predicted value ($Y_{predicted,n}$) and simulated value ($Y_{simulated,n}$), where:

	x_1	x_2	x_3	x_4	x_5	x_6	x_7	x_8	x_9	x_{10}	x_{11}
1	+	+	+	+	+	+	+	+	+	+	+
2	+	-	+	-	+	+	-	-	-	+	-
3	+	-	-	+	-	+	+	-	-	-	+
4	+	+	-	-	+	-	+	+	-	-	-
5	+	-	+	-	-	+	-	+	+	-	-
6	+	-	-	+	-	-	+	-	+	+	-
7	+	-	-	-	+	-	-	+	-	+	+
8	+	+	-	-	-	+	-	-	+	-	+
9	+	+	+	-	-	-	+	-	-	+	+
10	+	+	+	+	-	-	-	+	-	-	-
11	+	-	+	+	+	-	-	-	+	-	+
12	+	+	-	+	+	+	-	-	-	+	-

Table 2: Screening experiments with Plackett-Burman design: 11 two-level factors for 12 runs.

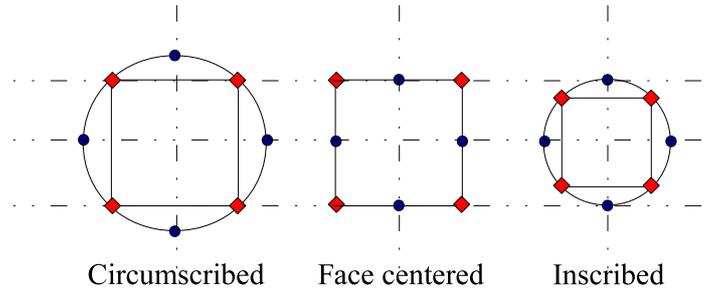


Figure 5: Comparison of the three type central composite designs

$$RMSE = \sqrt{\frac{\sum_{n=1}^N (Y_{predicted,n} - Y_{simulated,n})^2}{N}} \quad (2)$$

$$Y_{linear} = \beta_0 + \beta_1 X_1 + \beta_2 X_2 \quad (3)$$

$$Y_{quad} = Y_{linear} + \beta_{12} X_1 X_2 + \beta_{11} X_1^2 + \beta_{22} X_2^2 \quad (4)$$

$$Y_{cubic} = Y_{quad} + \beta_{112} X_1^2 X_2 + \beta_{122} X_1 X_2^2 + \beta_{111} X_1^3 + \beta_{222} X_2^3 \quad (5)$$

Number of factor	2	3	4	5	6	7
Full factorial	4	8	16	32	64	128
Fractional factorial ($\frac{1}{2}$)	2	4	8	16	32	64
Central composite	9/9	15/15	25/25	25/43	45/77	79/143
Box-Behnken	N/A	13	25	41	49	57

Table 3: Number of runs in each DoEs. Central composite: full/ $\frac{1}{2}$ fractional

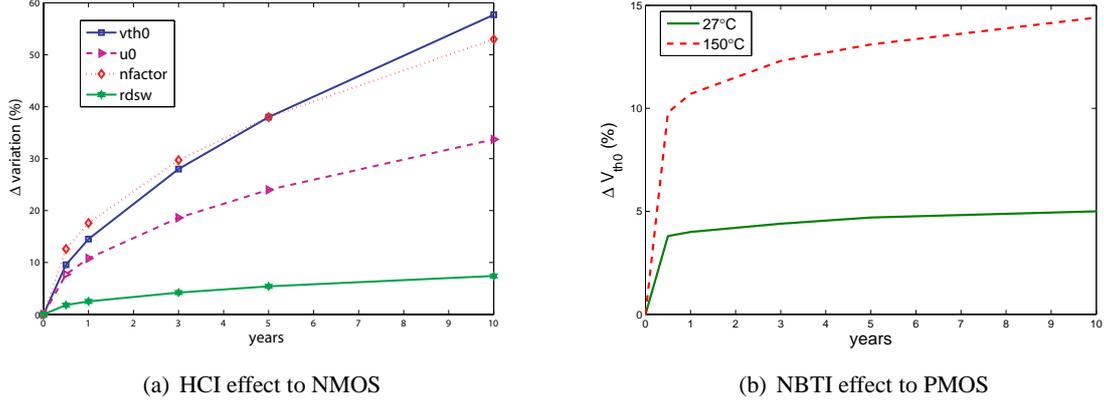


Figure 6: Parameters degradation by ageing effects in NMOS/PMOS transistor, simulating with ELDO.

2.2 Simulation flow

2.2.1 Ageing effects and process variations

In 65nm CMOS technology, ageing effects can degrade some BSIM4 parameters and influence the transistor performance. As shown in Figure 6(a), Hot carrier injection (HCI) can influence sub-threshold swing coefficient (n_{fac}), intrinsic threshold voltage (v_{th0}), intrinsic mobility (μ_0), saturation velocity (v_{sat}), drain source resistance per width (r_{dsw}), subthreshold region DIBL coefficient (eta_0) and threshold voltage offset (v_{off}). The correlation analysis is used to filter out some correlated parameter. v_{th0} , μ_0 , n_{fac} and r_{dsw} are selected as the main degraded parameters of NMOS transistor. Besides, the only BSIM4 parameter affected by negative bias temperature instability (NBTI) is v_{th0} of PMOS transistor (see Figure 6(b)). More severe v_{th0} degradation is observed when PMOS transistor work at high temperature. In Table 4, eight crucial BSIM4 parameters are sorted out as ageing sensitive and non-sensitive. In NMOS transistor, the dominant ageing nonsensitive BSIM4 parameters include: length variation (x_l), width variation (x_w), gate oxide thickness (t_{ox}) and channel doping concentration (n_{dep}). In PMOS transistor, except v_{th0} , other parameters mentioned above are ageing non-sensitive.

	Ageing sensitive	Ageing non-sensitive
HCI	$v_{th0}, u_0, n_{fac}, r_{dsw}$	$x_l, x_w, t_{ox}, n_{dep}$
NBTI	v_{th0}	$u_0, n_{fac}, r_{dsw}, x_l, x_w, t_{ox}, n_{dep}$

Table 4: Ageing effect to eight BSIM4 parameters

2.2.2 The co-evaluation flow

As shown in Figure 7, this methodology aims to:

- Judge the circuit ageing-immune or ageing-sensitive;
- Estimate degradation of circuit performance due to process variation and ageing effects;
- Find the most critical process parameters.

The flow begins with ageing model selection (HCI and NBTI). The schematic of designed circuit and the stress time are the input of the ageing simulation process. With ageing degradation models, after extracting fresh netlist of designed circuits, a transient simulation is performed to generate a aged circuit netlist. On the branch of process variation, after filter out less important BSIM4 parameters, selected

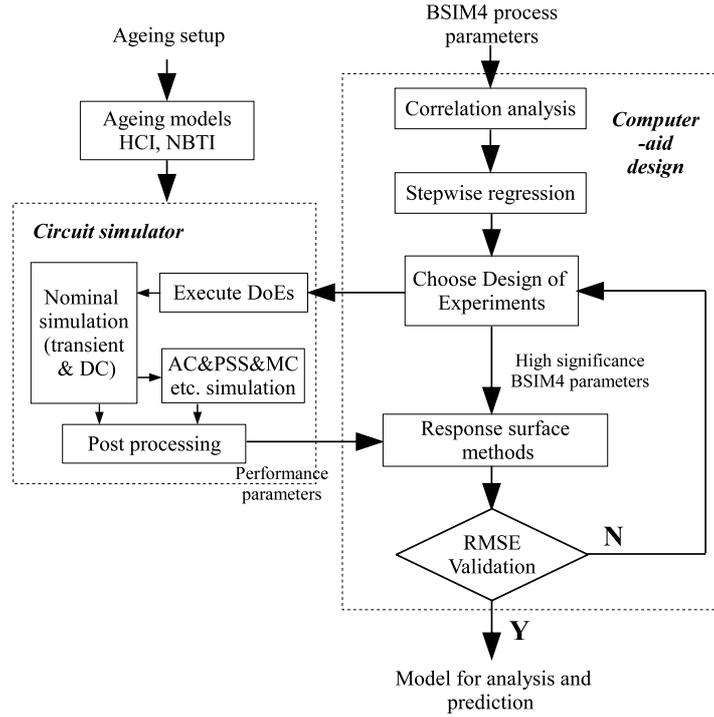


Figure 7: The co-evaluation flow of ageing effects and process variations

parameters are set up with a proper DoE mode. Ageing effect and process variation are evaluated by circuit simulator. Nominal simulation with transient and DC analysis is performed at transistor level. Other analysis such as AC, PSS and Monte-Carlo can be performed with saved aged circuit netlist (degradation information included). Simulation data processing is followed in order to plot response surface. RSMs is used to help designers to obtain intuitionistic reliability information at circuit design phase. For ageing-sensitive circuits, varied RSMs are used to estimate ageing and variability. Meanwhile, for ageing-immune circuits, a fixed RSM can supply variability information to designers [5, 6].

3 Case study

The proposed methodology is applied to two simple current mirrors (NMOS and PMOS type) and dynamic comparator (see Figure 8). Test circuits are implemented with 65nm CMOS process technology. Minimum transistor dimension is used. Reliability simulation is performed with ELDO simulator (maximum ageing time = 20 years). HCI and NBTI are considered as the main ageing effects. The statistical flow is carried out with Matlab statistics toolbox. Circuit process variation analysis is based on BSIM4 transistor model.

The result from correlation analysis is shown in Table 5. The significant orders determined by regression analysis are shown in Table 6. RMSEs between simulation result and RSMs' estimation are verified for different models (see Table 7). According to the RMSE results, quadratic model is used to plot RSMs.

Both NMOS and PMOS simple current mirror have been simulated. The most significant parameters: v_{th0} and u_0 are selected and normalized as the representative of process variations. The RSMs are built between v_{th0} , u_0 and output current (I_{out} as the circuit performance). The ageing analysis indicated that both HCI and NBTI can degrade output current. Varied response surfaces (see Figure 9(a) and Figure 9(b)) are used to estimate ageing degradation and process variations (v_{th0} and u_0). Comparing to HCI induced degradation in NMOS current mirror, the degree of NBTI induced degradation (PMOS current mirror) is lower than HCI.

	t_{oxe}	n_{dep}	r_{sh}	r_{shg}	v_{tho}	u_0	n_{factor}	r_{dsw}	c_f	x_l	x_w	j_{sws}	c_j	c_{jsw}	c_{jswg}
1	+	+	+	+	+	+	+	+	+	+	+	+	+	+	+
2	-	+	-	+	-	+	-	+	-	+	-	+	-	+	-
3	+	-	-	+	+	-	-	+	+	-	-	+	+	-	-
4	-	-	+	+	-	-	+	+	-	-	+	+	-	-	+
5	+	+	+	-	-	-	-	+	+	+	+	-	-	-	-
6	-	+	-	-	+	-	+	+	-	+	-	-	+	-	+
7	+	-	-	-	-	+	+	+	+	-	-	-	-	+	+
8	-	-	+	-	+	+	-	+	-	-	+	-	+	+	-
9	+	+	+	+	+	+	+	-	-	-	-	-	-	-	-
10	-	+	-	+	-	+	-	-	+	-	+	-	+	-	+
11	+	-	-	+	+	-	-	-	-	+	+	-	-	+	+
12	-	-	+	+	-	-	+	-	+	+	-	-	+	+	-
13	+	+	+	-	-	-	-	-	-	-	-	+	+	+	+
14	-	+	-	-	+	-	+	-	+	-	+	+	-	+	-
15	+	-	-	-	-	+	+	-	-	+	+	+	+	-	-
16	-	-	+	-	+	+	-	-	+	+	-	+	-	-	+

- t_{oxe} : Electrical gate equivalent oxide thickness
 n_{dep} : Channel doping concentration at depletion edge for zero body bias
 r_{sh} : Source/drain sheet resistance
 r_{shg} : Gate electrode sheet resistance
 v_{tho} : Threshold voltage at $v_{bs}=0$ for long-channel devices
 u_0 : Low-field surface mobility at t_{nom}
 n_{factor} : Subthreshold swing coefficient
 r_{dsw} : Zero bias LDD resistance per unit width for $RDSMOD=0$
 c_f : Fringing field capacitance
 x_l : Length variation due to masking and etching
 x_w : Width variation due to masking and etching
 j_{sws} : Isolation-edge sidewall source junction reverse saturation current density
 c_j : Zero bias bottom junction capacitance per unit area.
 c_{jsw} : Sidewall junction capacitance per unit periphery.
 c_{jswg} : Gate-side junction capacitance per unit width.

Table 5: Plackett Burman design: 15 two-level factors for 16 runs with BSIM4 parameters

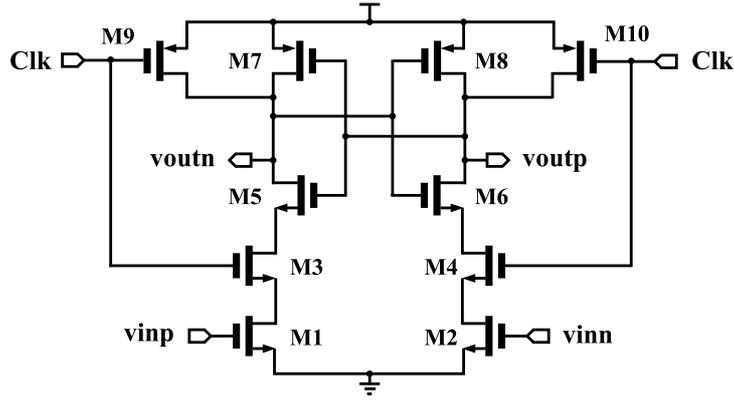


Figure 8: Dynamic comparator, transistor dimension $W/L = 0.36\mu\text{m}/0.06\mu\text{m}$

Table 6: The significant orders of BSIM4 parameters in test circuits

	1	2	3	4	5	6	7	8
NMOS Current Mirror	u_0	v_{th0}	t_{ox}	x_l	n_{fac}	n_{dep}	x_w	r_{dsw}
PMOS Current Mirror	v_{th0}	u_0	x_l	t_{ox}	n_{dep}	r_{dsw}	n_{fac}	x_w
Comparator (NMOS)	v_{th0}	t_{ox}	u_0	x_w	r_{dsw}	x_l	n_{fac}	n_{dep}
Comparator (PMOS)	v_{th0}	u_0	x_l	t_{ox}	r_{dsw}	x_w	n_{dep}	n_{fac}

From the simulation of dynamic comparator, we find the comparator can achieve ageing-immunity with HCI and NBTI stress, not only in offset voltage, also in slew rate and propagation delay of the circuit. Therefore, fixed response surface is used to illustrate the process variation only. The offset voltage is chosen as the circuit performance (see Figure 10(a)). From the regression analysis, we find that the variations of other parameters except v_{th0} have little or no influence on comparator offset voltage. Thus, the v_{th0} is the dominant parameter (see Table 6), in both NMOS and PMOS transistor). Figure 10(b) shows the fixed response surface which reflect v_{th0n} and v_{th0p} to comparator offset voltage.

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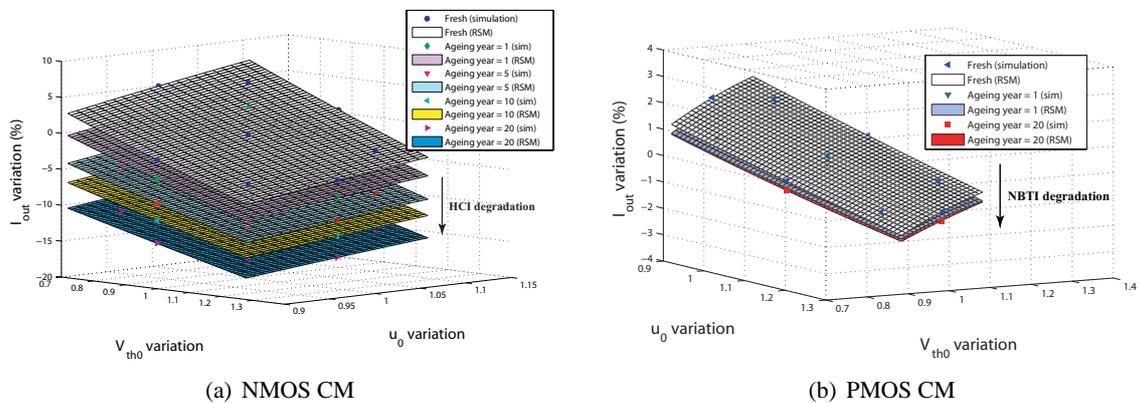


Figure 9: NMOS/PMOS Current mirror: varied RSMs between BSIM4 parameters and performance

Table 7: RMSE between simulation and RSMs' estimation

	Current Mirror (N)	Current Mirror (P)	Comparator
Linear	0.041	0.038	0.068
Quadratic	0.002	0.003	0.046
Cubic	0.0001	0.0016	0.007

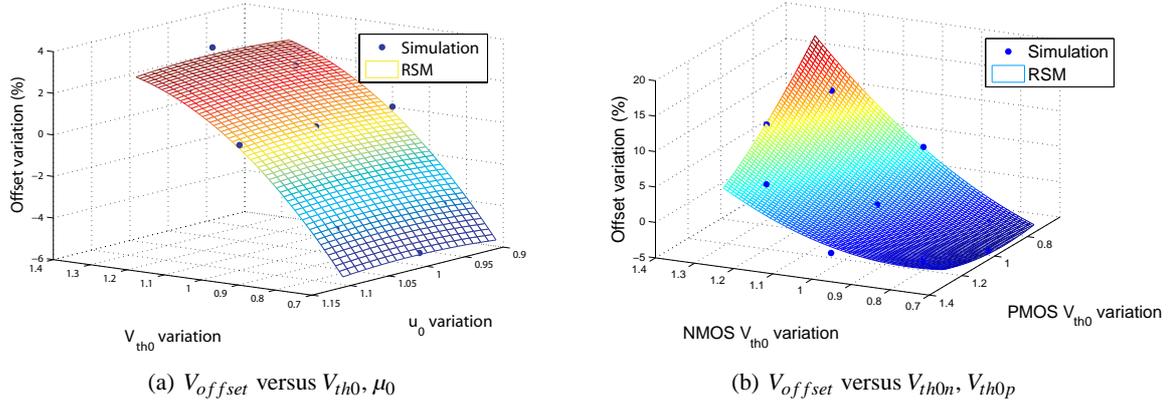


Figure 10: Comparator: fixed RSM between BSIM4 parameters and performance

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Appendix A Correlation analysis of BSIM4 parameters

	t_{oxe}	n_{dep}	r_{sh}	r_{shg}	v_{tho}	u_0	n_{factor}	r_{dsw}	c_f	x_l	x_w	j_{sws}	c_j	c_{jsw}	c_{jswg}
t_{oxe}	NaN	0	0	-0.022	0	-0.0045	-0.0197	0	0.0005	0	0	0	0	0	0
n_{dep}	0	NaN	0	-0.016	0	-0.0035	-0.0038	0	-0.1171	0	0	0	0	0	0
r_{sh}	0	0	NaN	0.036	0	-0.0045	0.0378	0	-0.0024	0	0	0	0	0	0
r_{shg}	-0.022	-0.016	0.036	NaN	0.0526	0.0065	-0.024	-0.0223	0.1359	-0.0126	-0.0479	0.0129	-0.041	-0.0156	0.0322
v_{tho}	0	0	0	0.0526	NaN	-0.0045	0.0226	0	0.0024	0	0	0	0	0	0
u_0	-0.0045	-0.0035	-0.0045	0.0065	-0.0045	NaN	0.0205	-0.0125	-0.0908	0.05	0.0045	-0.0125	0.0045	-0.0125	0.0045
n_{factor}	-0.0197	-0.0038	0.0378	-0.024	0.0226	0.0205	NaN	0.0351	0.0892	0.0575	-0.041	-0.0168	-0.0361	-0.0355	0.0226
r_{dsw}	0	0	0	-0.0223	0	-0.0125	0.0351	NaN	0.0226	0	0	0	0	0	0
c_f	0.0005	-0.1171	-0.0024	0.1359	0.0024	-0.0908	0.0892	0.0226	NaN	0.3866	-0.2304	-0.0024	0.1219	-0.2366	0.1175
x_l	0	0	0	-0.0126	0	0.05	0.0575	0	0.3866	NaN	0	0	0	0	0
x_w	0	0	0	-0.0479	0	0.0045	-0.041	0	-0.2304	0	NaN	0	0	0	-0.0018
j_{sws}	0	0	0	0.0129	0	-0.0125	-0.0168	0	-0.0024	0	0	NaN	0	0	0
c_j	0	0	0	-0.041	0	0.0045	-0.0361	0	0.1219	0	0	0	NaN	0	0
c_{jsw}	0	0	0	-0.0156	0	-0.0125	-0.0355	0	-0.2366	0	0	0	0	NaN	0
c_{jswg}	0	0	0	0.0322	0	0.0045	0.0226	0	0.1175	0	-0.0018	0	0	0	NaN

Appendix B Matlab subscripts

```
uiopen('INPUT.dat');
Vth0=INPUT(:,1)
X1=INPUT(:,2)
Tox=INPUT(:,3)
A0=INPUT(:,4)
one=ones(length(A0),1)
X=[Vth0,X1,Tox,one]
x1=Vth0
x2=X1
x3=Tox
X1=[x1,x2,x3,one];
X2=[x1.*x1,x1.*x2,x1.*x3,x2.*x2,x2.*x3,x3.*x3,X1];
X3=[x1.^3,x1.^2.*x2,x2.^2.*x1,x2.^3,x1.^2.*x3,
x3.*x2.*x1,x2.^2.*x3,x3.^2.*x1,x3.^2.*x2,x3.^3,X2];
[B,BINT,R,RINT,STATS] = regress(A0,X3)
plot(X3*B, A0,'o')
table = [X3*B,A0,(A0-X3*B)./A0];
x1fit = min(x1):0.01:max(x1);
x2fit = min(x2):1E-10:max(x2);
[X1FIT,X2FIT] = meshgrid(x1fit,x2fit);

X = [ones(size(x1)) x1 x2 x1.*x2 x1.^2 x2.^2];
b = regress(A0,X)
YFIT = b(1)+b(2)*X1FIT+b(3)*X2FIT+b(4)*X1FIT.*X2FIT+b(5)*X1FIT.^2+b(6)*X2FIT.^2

scatter3(x1,x2,A0,'filled')
hold on

mesh(X1FIT,X2FIT,YFIT)
xlabel('Vth0')
ylabel('length variation')
zlabel('A0')
```