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Active devices choice and design of an all cryogenic superconductor resonator oscillator

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Abstract—Several silicon-germanium bipolar transistors have been measured at cryogenic temperature regarding their gain and phase noise performance. The electrical model of the chosen device has been extracted. Using this model, the phase noise performance of a cryogenic superconductor oscillator has been simulated. The results are very promising, with a phase noise level of -155 dBc/Hz at 1 kHz offset from of a 1 GHz carrier.

Keywords—Microwave oscillator; phase noise; SiGe transistor; nonlinear modeling; superconductors; cryogenics

I. INTRODUCTION

Recent research on high-temperature superconductors (HTS) has led to the development of very high Q planar resonators. Associated with a well-chosen amplifier, those resonators would make a very efficient low phase noise oscillator. This device could outperform the performance of the best quartz referenced oscillators in the low microwave range (near 1 GHz). Indeed, high quality factors of 250 000 have been demonstrated around 1 GHz [1,2,3] with those HTS planar resonators. However, no oscillator with HTS resonators has yet included a low-temperature RF amplifier.

In this paper, the selection and modeling of transistors that can be used to design a low-temperature low phase noise amplifier is described. Then, a fully integrated 1 GHz oscillator working at 60 Kelvin is simulated. The goal is to outperform by 10 dB at least the best commercially available 1 GHz sources, which generally feature a phase noise level in the range of -140 dBc/Hz at 1 kHz offset from 1 GHz carrier.

II. DEVICES SELECTION

Bipolar SiGe-heterojunction transistors are known for their low 1/f noise properties at ambient temperature. Also, contrarily to all-silicon devices, they keep their current and gain performance at low temperature [4,5]. For this reason, four SiGe transistors have been chosen and characterized both at 300 K and at cryogenic temperature. A first test campaign has been conducted at 80 K, using liquid nitrogen, to simplify the experimental procedure. A second campaign at 60 K is scheduled to fully validate the model of the selected transistor.

Indeed, the oscillator operation temperature will be 60 K, which ensures an optimized performance of the resonator. All transistors have been measured in common emitter topologies, between two 50 Ω isolators and submitted to a 1 GHz signal. The selection has been based on the combination of two RF parameters: the residual phase noise at the 1-dB compression point and the 50 Ω gain (S_{21}) at 1 GHz.

All measurements have been conducted on a phase noise test bench (Fig. 1) which has been specially optimized for 1 GHz operation. It is based on an ultra-low phase noise 1 GHz source (a multiplied OCXO), uses two phase detectors to benefit from the correlation approach and a search for an optimized rejection of the source AM noise [6] (fine tuning of the quadrature condition).

Specific transistor test fixtures have been used to perform precise RF measurements at low temperature. Indeed, a TRL calibration set for S parameters measurements has been designed with the same test fixtures. Gain (S_{21}) and phase noise results are summarized in Table 1 and 2, for respectively 300 K and 80 K performance.

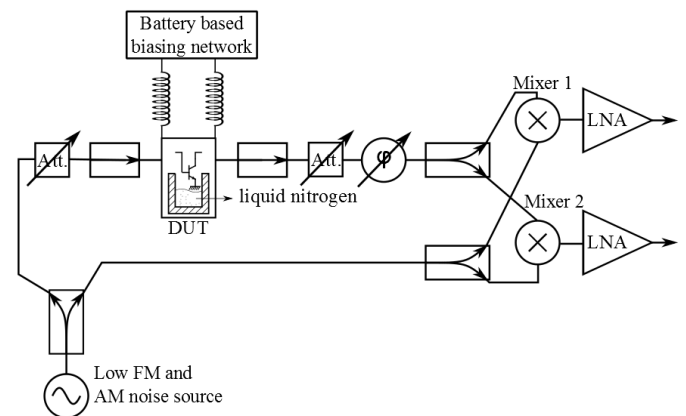


Fig. 1. Test bench for the residual phase noise measurement of a device in liquid nitrogen.

TABLE I. PHASE NOISE AND RF GAIN AT AMBIENT TEMPERATURE.

Phase noise (dBrad ² /Hz) and S ₂₁ at 1 GHz and 300K	100 Hz	1 kHz	100 kHz	Gain (dB)
TR-1	-149	-157	-166	21.5
TR-2	-156	-164	-169	20.0
TR-3	-136	-157	-164	21.3
TR-4	-163	-170	-175	14.7

TABLE II. PHASE NOISE AND RF GAIN AT LOW TEMPERATURE.

Phase noise (dBrad ² /Hz) and S ₂₁ at 1 GHz and 80 K	100 Hz	1 kHz	100 kHz	Gain (dB)
TR-1	-130	-155	-162	19.0
TR-2	-155	-162	-169	21.4
TR-3	-134	-144	-158	24.4
TR-4	-147	-156	-169	15.6

TR-2 transistor has been chosen among the tested devices. As illustrated in Fig. 2, this transistor features a good residual phase noise level and almost the same performance at ambient and cryogenic temperature.

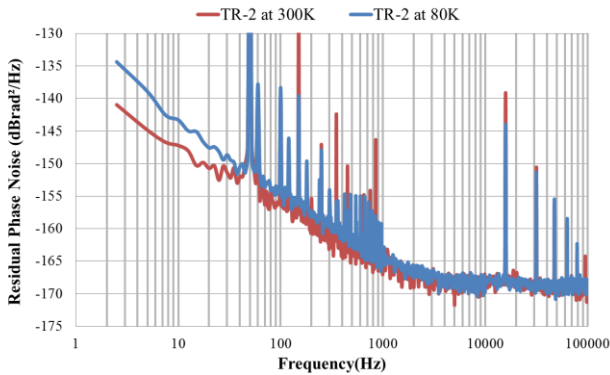


Fig. 2. Measured of TR-2 residual phase noise at 1GHz. Low and ambient temperature measurements with $I_C = 30$ mA and $V_{CE} = 2$ V.

By using the same test bench, a second investigation has been performed. This time, two silicon phase tuning diodes (varactor diodes) have been tested. Both were measured at ambient and low temperature (60K), and their electrical behavior was unchanged, as illustrated Fig 3. Used in series connected between two 50 Ω loads, these diodes do not add significant phase noise to a 1 GHz RF loop. We tried to measure this phase noise contribution, both at ambient temperature and 80 K, both at low RF input power (0 dBm) or high RF input power (10 dBm), but it was in each case lower than our phase noise measurement bench capabilities, i.e. -171 dBrad²/Hz at 1 kHz offset.

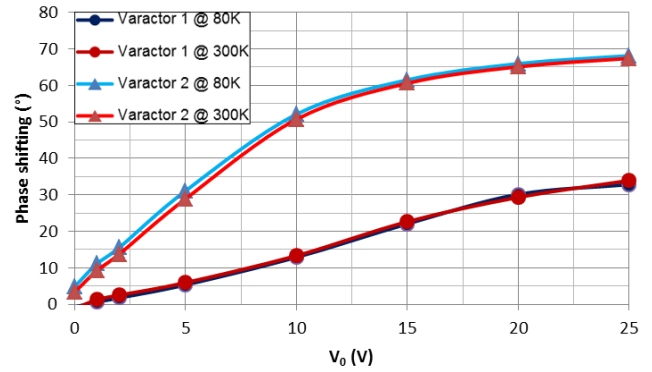


Fig. 3. Phase variation at 1 GHz induced by two in-series connected varactor diodes at low temperature and ambient temperature.

III. LOW-TEMPERATURE NON-LINEAR MODEL

To perform the oscillator design, the physical and electrical characteristics of the active device must be known. Therefore DC, dynamic, low-frequency noise and phase noise measurements have been performed at 80 K. Thanks to those measurements the transistor non-linear model (Gummel-Poon model) has been extracted using Keysight ADS software. Moreover several TR-2 transistors have been tested to validate this model.

This model allows us to fit simulations and measurements for DC-characteristics and S parameters (cf Fig. 4 to Fig. 7 for I(V), S-parameters and output power versus input power). However, concerning the noise, the problem is more complex: an accurate model of the transistor intrinsic noise sources need to be used. Several existing methods and models have already proven their accuracy for SiGe HBT phase noise modeling at ambient temperature. The one we have used is described in the reference [7]. Fig. 8 shows that the implemented model fit the measured residual phase noise.

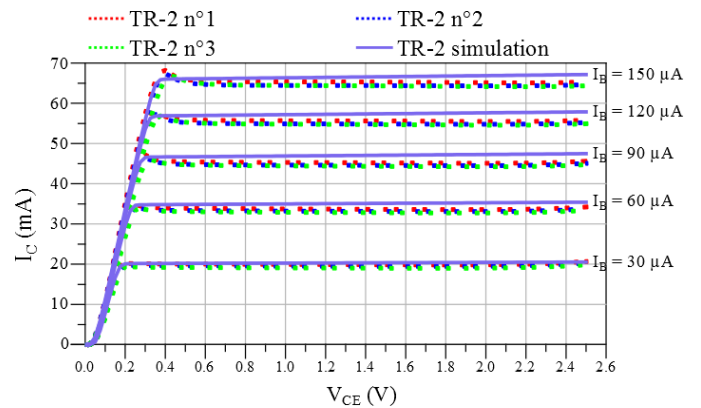


Fig. 4. Simulated and measured DC current-voltage curves at 80 K for 3 different TR-2 transistors.

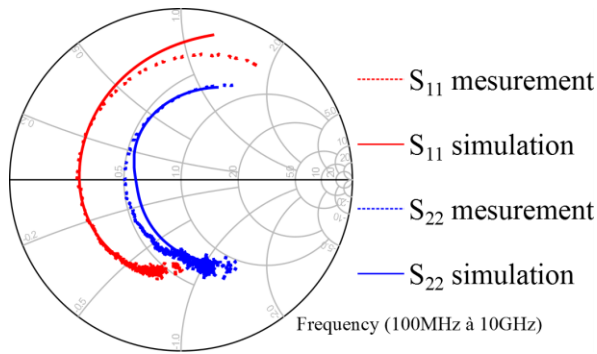


Fig. 5. Simulated and measured S_{11} and S_{22} parameters curves at 80 K for a TR-2 transistor.

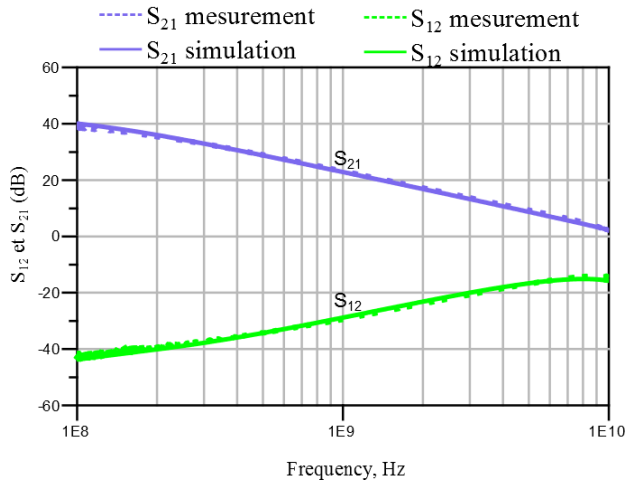


Fig. 6. Simulated and measured S_{21} and S_{12} parameters curves at 80 K for a TR-2 transistor.

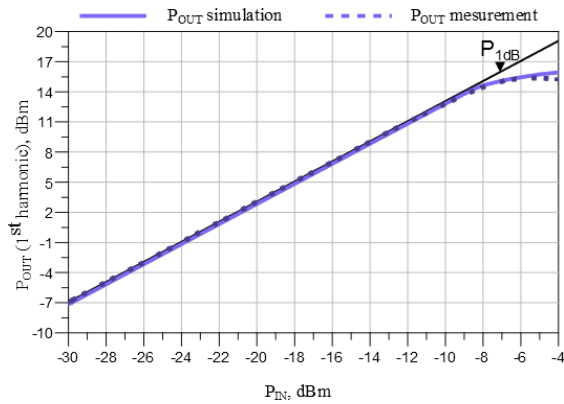


Fig. 7. Simulated and measured power characteristics at 80 K for a TR-2 transistor.

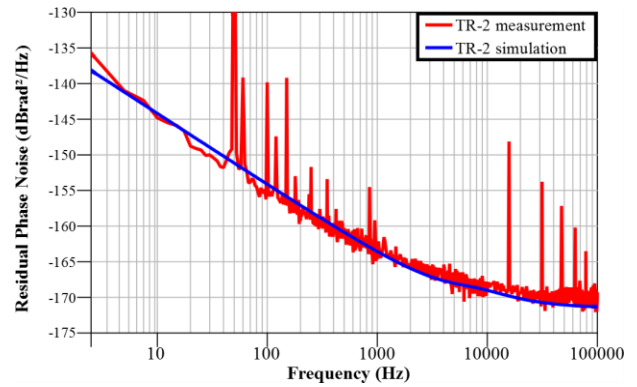


Fig. 8. Simulated and measured TR-2 residual phase noise at 1 GHz. $I_C = 30$ mA, $V_{CE} = 2$ V, $T = 80$ K.

IV. OSCILLATOR SIMULATION

An oscillator has been designed using TR-2 device and a planar HTS resonator model. The oscillation loop is presented in Fig. 9. The active part of the oscillator is realized on an alumina substrate and link by wire bonding to the HTS-resonator. Apart from the low phase noise amplifier, the coupler, the varactor and the lines that adjust the 2π phase loop are also realized on the alumina substrate. To stabilize, match the amplifier and optimize its residual phase noise, several resistances and capacitors were added (Fig. 10). Then the all integrated oscillator is implemented on the top of the cryocooler's cold finger.

The simulated phase noise is depicted in Fig. 11 and features -155 dBc/Hz at 1 kHz offset. This phase noise level has been obtained with an HTS resonator featuring an unloaded Q of 290 000 at 1 GHz and a loaded Q of 110 000.

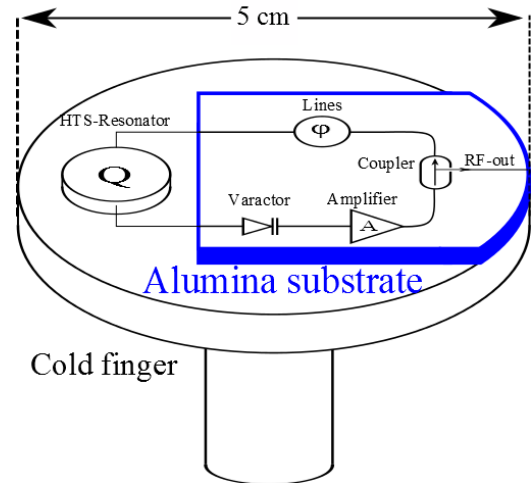


Fig. 9. Picture of the oscillator topology and of its implementation on the cold finger of the cryostat.

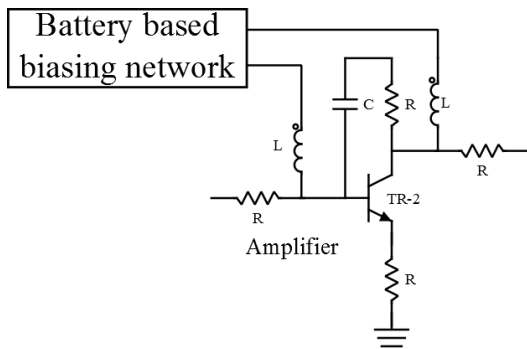


Fig. 10. Amplifier based on TR-2 transistor.

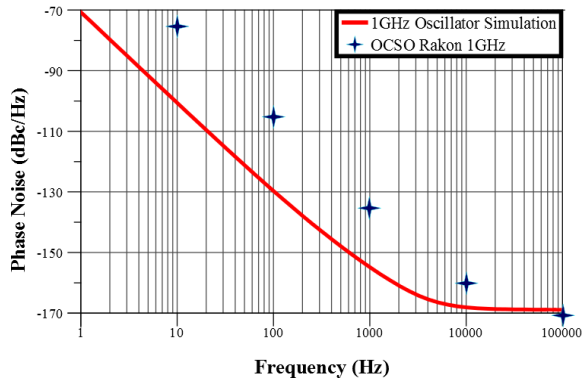


Fig. 11. Simulated 1 GHz oscillator phase noise with TR-2 transistor model and HTS resonator ($Q_L = 110000$).

V. CONCLUSION

Characterization of SiGe devices at low temperature for oscillator design has been presented. A nonlinear model extraction has been performed on one of these devices at 80 K. The model is able to predict the phase noise performance in amplifier configuration. A superconductor cavity oscillator has been designed using this model and the simulation shows very promising phase noise results. This oscillator will be soon realized on an alumina substrate.

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