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Lifetime of Power Electronics Interconnections in Accelerated Test Conditions: High Temperature Storage and Thermal Cycling.

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Abstract

We investigate the effect of three testing conditions (thermal shock, Rapid Temperature Changes – RTC – and high temperature storage) on the interconnects of a power electronic module. In particular, the mechanical strength of thick aluminium wirebonds is investigated and shows that while it is not affected by storage at 230 °C, it is much more sensitive to thermal cycling. Shock tests are found to be especially severe, despite having a smaller temperature swing than RTC. Regarding the die attach, no noticeable reduction in mechanical strength is found, regardless of the ageing conditions, and despite clear micro-structural evolutions.

1. Introduction

In many applications, such as aerospace or automotive, power electronics systems are expected to operate over a wide ambient temperature range (more than 200 °C temperature swings, [1]). This is especially true for silicon-carbide (SiC) devices, as their maximum junction temperature is usually higher than that of their silicon counterparts.

Deep thermal cycling causes a high level of thermo-mechanical stresses in the packaging of these systems. Also, the high temperature encountered during the thermal cycle accelerates mechanisms such as the diffusion of chemical species at the interfaces, which in turn may cause weaknesses in the packaging.

As the reliability of power electronic modules was found to be unsatisfactory [2, 3], and as the thermal stresses are only expected to increase in the foreseeable future, there is a need to improve the current packaging technologies.

For example, regarding the die attach, many solutions are available, from Au or Zn-based solder to glasses or silver sintering [4, 5]. Silver sintering is a promising technology, but it uses a very different process compared to soldering. Among solders, AuSn is an attractive lead-free replacement for High Melting Point (HMP) solders (which contain 95 % lead). The melting point of AuSn is limited (281 °C), but it is easier to implement than more demanding alloys such as AuGe or AuSi [4].

Regarding the ceramic substrates, Si₃N₄ has been identified as the most attractive material for reliable substrates [5, 6]. Indeed, its flexural strength (700 MPa) is almost double of that of Al₂O₃ (450 MPa) or AlN (350 MPa) [7]. On the contrary, AlN is attractive for its high thermal conductivity.

Another weak point is the die topside interconnection, usually based on aluminium wirebonds. Aluminium is chosen because it is cheap (wires used in power electronics are much

thicker than in microelectronics, 200-500 µm vs. 25-50 µm in diameter), it does not harden when cycled, and it is a good electrical conductor. There are, however, concerns regarding the reliability of the wires: the wire/die interface, in particular, generates thermo-mechanical stresses due to the mismatch in coefficient of thermal expansion (CTE) between a SiC die (≈ 4 ppm/K) and the aluminium wire (≈ 23 ppm/K). Thermal cycling tests listed in the literature range from 10 cycles between -196 and 500 °C [8] to 12000 cycles between 45 and 175 °C [9]. Another concern is the evolution of the micro-structure at the interface between the wire and the copper layers of the ceramic substrate. Usually, these copper layers receive a Ni/Au finish. Au is often mentioned as causing kirkendall voiding with Al [5]. However, some experimental tests [10] with Al wires bonded on NiAu-finished tracks only detected the occurrence of Al/Au Intermetallic Compound (IMC) after more than 7000 h at 250 °C.

In this paper, we focus on AuSn die attaches and aluminium wires. These interconnection technologies were selected for an aircraft application where reliability is the main concern. AuSn was chosen as a lead-free alternative to HMP solder alloys. The reliability of these interconnection technologies is evaluated in thermal cycling conditions as well as in high temperature storage (isothermal conditions). In the next section, we detail the test protocol. Then, in sections 3 and 4 we present the results regarding the wirebonds and die attach respectively. Our conclusions are given in section 5.

2. Test protocol

2.1. Preparation of the test vehicles

The test vehicles used in this article were prepared by Microsemi, using silicon carbide diodes (also from Microsemi, 4.79×4.79 mm², 380 µm-thick with 5.7 µm Al as the top metal) and ceramic substrates sourced from two manufacturers:

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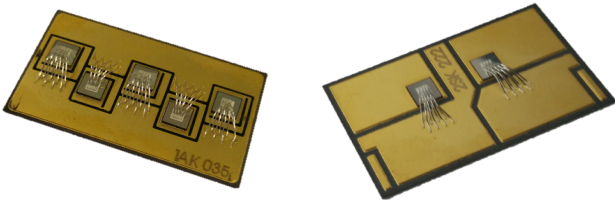


Figure 1: Photograph of the test vehicles. Two configurations were used (based on the same substrate, the dice being mounted on one side or the other): 5 dice or 2 dice.

- Si_3N_4 , Active Metal Braze (AMB) substrates from the company Kyocera (referenced to as “K” in the remaining of the article), with a 320 μm -thick ceramic layer, 300 μm -thick copper on one side and 200 μm on the other side;
- AlN AMB Substrates from the company Dowa (referenced to as “D”), with 300 μm -thick copper layers (both sides) and 635 μm -thick ceramic.

In both cases, the substrate pattern is identical (see fig. 1), and a Ni/Au ENIG plating was applied by the manufacturer (5 μm Ni and 50 nm Au). The SiC dice are soldered onto the substrates using Au80Sn20 solder alloy (melting point 281 $^\circ\text{C}$).

Each diode is connected using 8 aluminium wirebonds (diameter 254 μm). In some cases (175 $^\circ\text{C}$ storage, described below), the test vehicles were split into 5 samples using a low speed diamond saw (Escil Labcut 150, with a Presi LM+ blade) to allow for more tests.

2.2. Accelerated Test Conditions

Two kinds of accelerated tests were performed:

- Storage tests (isothermal tests), in which the samples are exposed to a constant, elevated temperature over a long period of time. These tests are expected to trigger temperature-sensitive phenomena such as diffusion of chemical species.
- Temperature cycling tests, where the samples are exposed to large temperature swings. This generates thermo-mechanical stresses in the samples, which trigger fatigue mechanisms.

For the thermal cycling tests, two temperature profiles were chosen, to provide two largely different testing conditions:

- Rapid Temperature Change (RTC): -55 $^\circ\text{C}$, maintained for 15 min, ramp-up at 10 $^\circ\text{C}/\text{min}$ up to 175 $^\circ\text{C}$, 15 min at 175 $^\circ\text{C}$ and ramp-down at 10 $^\circ\text{C}/\text{min}$, in a Climats Excal 1423-TE chamber. Each cycle lasts for 76 min.
- Shock: -40/+125 $^\circ\text{C}$ temperature swing, in a two-chamber system (Climats CTr series) which generates very fast temperature changes (estimated at 65 $^\circ\text{C}/\text{min}$). The samples are moved every 15 min.

Regarding the storage conditions, a preliminary test was performed: some test vehicles were submitted to a “step stress”, during which the temperature was increased from 170 to 270 $^\circ\text{C}$ by 20 $^\circ\text{C}$ steps every 24h. For each step, two samples were removed from the oven, and characterized (die shear test, wires

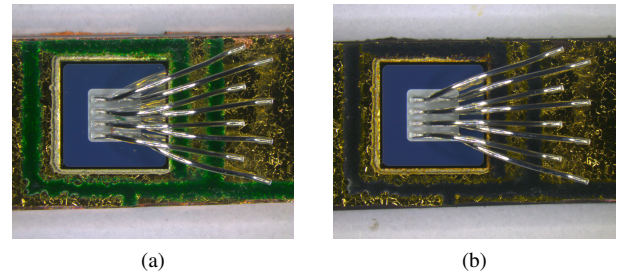


Figure 2: Photographs of one of the test samples before storage and after 672 h at 175 $^\circ\text{C}$ in air. The only visible change is the darkening of the green marking. No change in appearance is noticeable on the die or on the substrate finish.

pull and shear test, and microsections). No evolution could be detected from these mechanical tests. The micro-structure followed a classical evolution, with a coarsening of the phases, and the thickening of the interfacial intermetallic compounds of the solder joint, but no indication of advanced degradation was found. As the melting point of the AuSn alloy is 281 $^\circ\text{C}$, it was decided to perform the ageing at a noticeably lower temperature: 230 $^\circ\text{C}$. In parallel, a series of samples was stored at 175 $^\circ\text{C}$ to provide a comparison with the RTC cycling tests. For practical reasons, the 230 $^\circ\text{C}$ -storage tests were performed in a nitrogen atmosphere, while all the other tests (175 $^\circ\text{C}$ storage and all cycling tests) were performed in air. The composition of the atmosphere (air or nitrogen) was not found to have any particular consequence on the results.

D-Type substrates failed early during the cycling tests (before the first 500 cycles for RTC and 2500 cycles for shock). This is not surprising, as AlN ceramic (used in D-type) is not as tough as Si_3N_4 (used in K-type) [11]. As a consequence, and because this article focuses on investigating the interconnections (die attach and wirebond), we only present cycling results for the K-type substrates. D-type and K-type results are presented for storage, as it induced no substrate failure.

2.3. Characterization

The tests and corresponding characterization were performed in two laboratories: Laboratoire Ampère (Lyon, France) for the storage tests, and IMS (Bordeaux, France), for the cycling tests. As a consequence, a special care was taken to ensure consistent results between both teams.

For each data point presented below, the samples were characterized as follows. At IMS, a sample with 5 dice was removed from the cycling chambers for mechanical testing, and a sample with two dice was taken for for microsection. At Ampère, only one sample was used, with 4 dice used for mechanical tests, and one for microsection.

For mechanical characterization, a Dage 3000 was used at IMS, with the following parameters: for die shear, a 100 kgf load cell, a tool speed of 100 $\mu\text{m}/\text{s}$, and a tool height of 70 μm ; for the wire pull, a 1 kgf load cell and a tool speed of 250 $\mu\text{m}/\text{s}$. At Laboratoire Ampère, the test system was a XYZTEC Sigma Condor, with a 200 kgf load cell for die shear, a tool height of 80 μm , and a tool speed of 200 $\mu\text{m}/\text{s}$; for wire pull, a tool

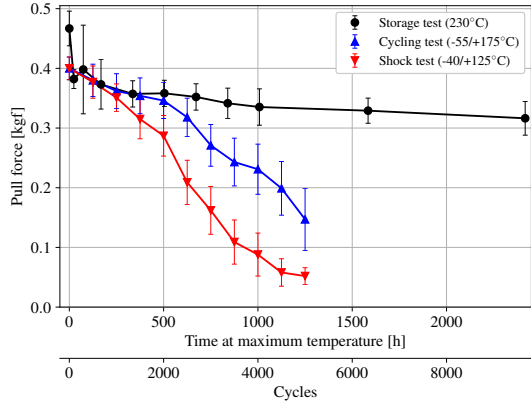


Figure 3: Wire pull strength as a function of time spent at maximum temperature. The error bars correspond to the standard deviation of the measurements.

speed of $600 \mu\text{m/s}$ and a 10 kgf load cell. At Ampère, pull tests were performed on half of the wires only, the remaining half being submitted to wire shear test with the following parameters: 10 kgf load cell, tool speed $200 \mu\text{m/s}$, tool height $50 \mu\text{m}$.

3. Wirebonds

The evolution of the pull strength of the aluminium wires during the tests is presented in Fig. 3. It appears that while the strength drops rapidly for the cycling tests, it only shows a moderate reduction during the storage tests (except a 0.1 kgf drop in the first 24 h). The actual pull strength for the cycled samples is even lower than plotted in Fig. 3, as some wires detached in the cycling chamber and could not be pulled (these wires were taken into account in the evaluation of the failure modes, below).

This is summarized in Fig. 4. This figure represents the distribution of the failure modes of the pulled wires, for each test condition (shock, RTC, 230°C storage). For the shock tests, a clear shift is visible: at the beginning, most ruptures occur in the wire. Then, the attach of the wire becomes weaker, and finally it is so weak that the wires even detach before the pull test. These are marked as “Failed” in Fig. 4b.

For the RTC tests, the trend is similar, albeit slower, and with a period where “Foot” failures are predominant. For storage, however, no failure of the attach (or failure in the oven) has been observed yet. Storage results show little evolution between $t=0$ and 2400 h. Pull failure modes in storage conditions are distributed between “Wire” and “Foot” failures. As most of the failures occur close to the “ankle” of the wire, it can sometimes be difficult to discriminate between “Foot” and “Wire” failure modes. Nevertheless, the trend seems to be a shift towards more “wire” failures as the storage test progresses (the same trend is observed for sample types D and K, which are considered together in Figs 3 and 4).

The stability of the wire/die and wire/substrate interfaces in conditions of thermal storage is demonstrated in Fig. 5, which presents the shear strength of the wire feet, either on die, K-type substrate or D-type substrate. Except a $\approx 20\%$ drop in shear strength at the beginning of the test for wire attaches on type-D

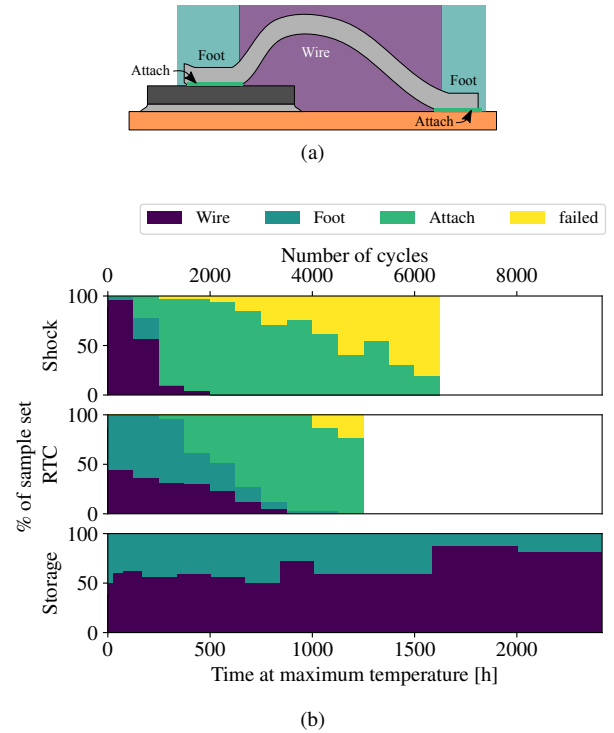


Figure 4: Failure mode for the pulled wires. (a) location of the failure: “Foot” failmode corresponds to a rupture within the aluminium wire, at the ankle (or foot) area. “Attach” corresponds to a rupture of the die/wire or the substrate/wire interface. Tests marked as “Failed” correspond to wires which were no longer attached after cycling, and therefore could not be pulled. (b) results obtained after cycling (shock and RTC) and storage (230°C) tests.

substrate, there is no noticeable evolution of the shear strength over time. Furthermore, all ruptures occur in the wirebond material rather than at the wire/die interface (“Attach”) as depicted in Fig. 6. This indicates that in the absence of thermal cycling, the attach remains strong.

4. Die Attach

Regarding the die attach, no obvious drop in mechanical strength has been observed: in cycling test (shock and RTC), the die shear strength exceeded the tester capability (100 kgf) for all samples. The shear tester used for the stored samples has a higher capability (200 kgf). A few failures were observed (Fig. 7), but in all cases, the initial failure mode was related to a fracture of the die. Therefore, it is difficult to conclude whether the observed failures are related to ageing.

Some cross-sections of K-type samples before testing and during ageing are presented in Figs. 8 and 9. They show that the solder layer is uniform. Only a few voids could be seen in the solder joint, which is consistent with the X-ray analyses of the same samples presented in [12]. The composition of the various phases was obtained by comparing EDS measurements with the phase diagrams in [13]. The evolution of the microstructure with time is consistent with [13]: a thick interfacial IMC forms at the bottom, in contact with the Ni layer. The fine microstructure visible in Fig. 8a coarsens with ageing, with a clear phase growth in Fig. 8b and c.

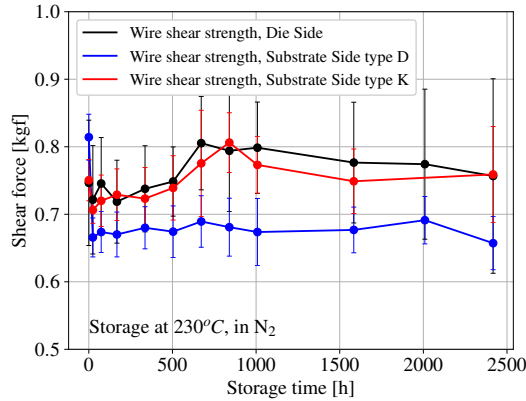


Figure 5: Wire shear strength as a function of storage time (at 230 °C). The error bars correspond to the standard deviation of the measurements. No clear evolution is visible, except a small drop at the beginning for the substrate side on substrate type D.

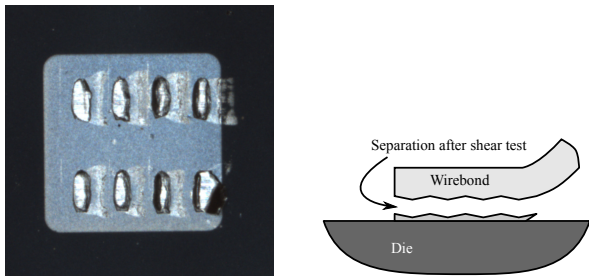


Figure 6: Surface of one of the dice after shear testing. The rupture occurred within the wirebond material, indicating a good interface quality.

Cross sections of a sample which underwent 3000 RTC cycles are given in Fig. 10. They show some noticeable difference with the stored samples: many cracks have developed in the solder layer, and some of them tend to propagate in the Ni and Cu layers; hillocks form at the copper/solder interface (Fig. 10a), which is no longer flat as for stored samples (Fig. 9).

5. Discussion and Conclusion

5.1. Wirebonds

The storage tests, although performed at high temperature (230 °C) did not demonstrate a reduction in mechanical strength. This was expected on the die side, where the Al wires are bonded to a Al pad. The same results are observed on the substrate side, despite the different metals in contact (NiAu finish on copper). The pull tests (Fig. 3) show a slow reduction in breaking force, which is most likely associated with a reduction in the wire tensile strength (increase of “wire” failures in Fig. 4).

For cycled samples, the reduction in mechanical strength is much faster and much more dramatic, with most wires eventually falling before the pull test. Furthermore, after an initial distribution of failure modes comparable to that of stored samples (“Wire” and “Foot” failures, see Fig. 4), the failures concentrate at the wire attaches. Because this is not observed on stored sam-

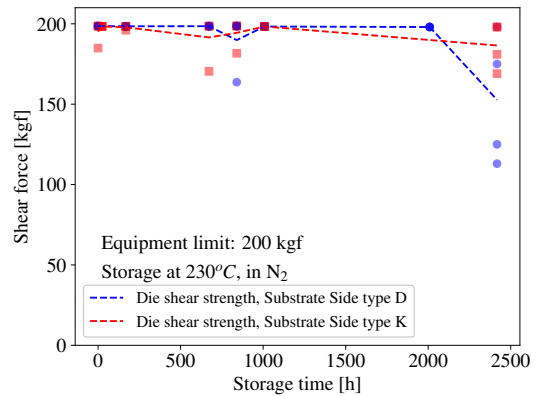


Figure 7: Die shear strength as a function of storage time. The test equipment used for cycled samples is limited to 100 kgf, and no failure could be measured. For stored samples, the test were performed up to 200 kgf, but that was still insufficient to remove most of the dies; all of the failures were due to die fracture, not to the solder layer. Dots plotted at 200 kgf correspond to dies which survived the test.

ples, it can be concluded that the thermo-mechanical stresses are the main cause for the reduction in mechanical strength.

Furthermore, samples submitted to shock cycling degrade much faster than those submitted to RTC, despite the smaller temperature swing (-40/+125 °C for shocks vs. -55/175 °C for RTC). This means that the rate of the temperature change is very important. Either time-dependent phenomena are involved (visco-plastic deformation), or the rate in temperature change is high enough with the shock tests to cause inhomogeneous temperature distribution in the sample (for example, the wires could heat and cool faster than the dies and substrates, which would amplify the thermo-mechanical stresses). Finite-Elements simulations would be needed to validate or invalidate these hypotheses. A comparison with active power cycling, which generates even faster temperature changes (but with a lower amplitude) might also help. This kind of cycling is often used to assess the reliability of the wirebonds, as it concentrates the thermo-mechanical stresses around the die (which dissipates the power). Based on the results presented in [14], failure is expected to occur for around 10000 cycles with a temperature swing of $\Delta T = 160$ °C, which is consistent with the 6500 cycles observed in our case for the shock tests ($\Delta T = 165$ °C).

In any case, reducing the sensitivity of the interconnections to the thermal cycling would involve the standard techniques [15]: using a larger number of smaller-diameter wires, to reduce the stresses at the wire attach area; place a spacer with a CTE closer to that of Al on top of the die (for example with a NiAu finish, as it was found to produce reliable attaches); use a “glob top” to encapsulate the wire foot. The wire could also be changed for AlCu wire [14] or ribbon.

5.2. Die Attach

No significant variation of the mechanical strength of the die attach was observed during any of the tests: for cycling tests, all attaches exceeded the capability of the equipment (100 kgf, equivalent to 43 MPa for a 4.79×4.79 mm² die). For storage tests, a few samples did not sustain 200 kgf (the limit of

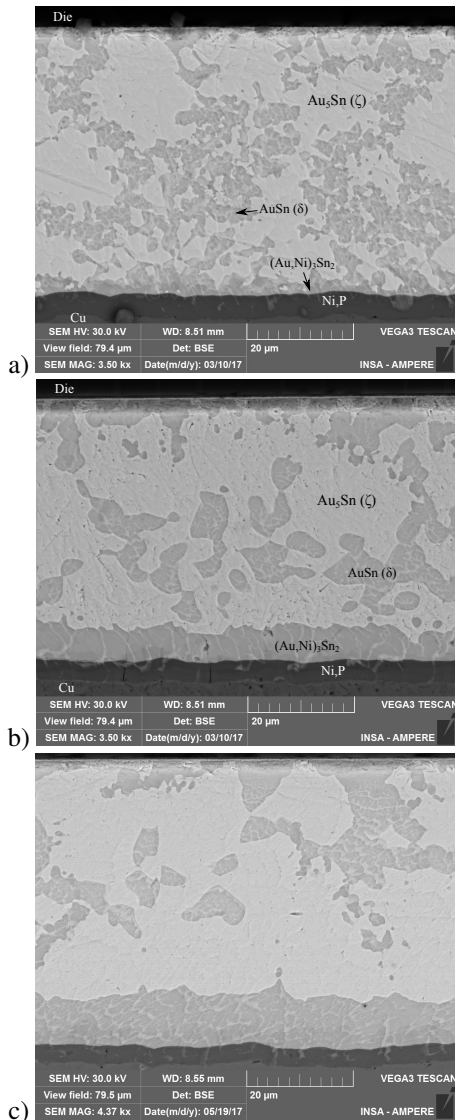


Figure 8: Cross sections of the die attach before testing (a), after 672 h (b), after 2417 h (c) at 230 °C. Phase compositions were identified using EDS spot measurements

the second shear tester), but all failure cases occurred above 100 kgf, with a fracture of the die (which might have been caused by slight misalignment or denting of the shear tool, chipping of the die, or actual ageing of the assembly).

Microsections were found to be much more instructive. As expected, the microstructure coarsens with storage time (Fig. 8). No continuous interfacial IMC appears to form at the solder/die interface. A much thicker, continuous IMC forms at the solder/substrate interface, but it does not cause any voiding or delamination (which is consistent with the shear test results).

Although they remain strong, the solder joints of cycled samples are very different (Fig. 10: they contain many voids and cracks, some extending to the copper layer of the substrate; their copper layer exhibits “hillocks” (Fig. 10a), while that of stored samples (Fig. 9) remains flat. Such hillocks have been reported to appear during thermal cycling for DBA substrates, which use Aluminium instead of copper [9]. As AuSn solder

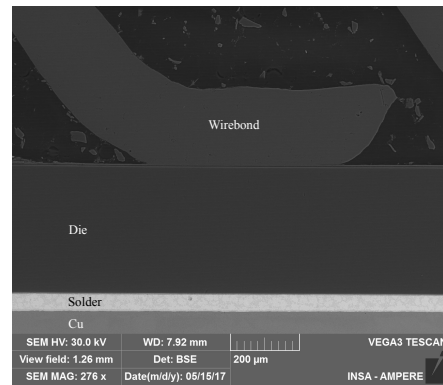


Figure 9: Low-magnification cross-section of the die attach, showing the flat copper/solder interface (a wirebond attach is also visible in this image). This sample was stored at 230 °C for 504 h.

is harder than the classical HMP alloys, it can be assumed that a large part of the thermo-mechanical stresses caused by thermal cycling is transferred to the copper, resulting in its plastic deformation. On the contrary, Figs. 10b and 10c show that the size and distribution of the phases in the solder layer are not noticeably affected by cycling, as they are similar for a cycled and stored sample which spent approximately the same time at 175 °C. Obviously, the temperature has a much more pronounced effect, as can be seen in Fig. 8b, which has a coarser microstructure and thicker interfacial IMCs after 672 h at 230 °C.

5.3. Conclusion

The structure investigated in this paper (SiC dice soldered on a substrate using AuSn, and connected with thick Al wirebonds) was found to have an excellent reliability regarding continuous operation at high (230 °C) temperature. Regarding thermal cycling, the weakest point was found to be the wirebonds, which started failing after only 1000 thermal shocks (-40/+125 °C). The comparison with wider but slower thermal cycles indicates that wirebonds are very sensitive to the rate of temperature change. On the contrary, thermal cycling caused visible damage in the solder layer, but we observed no reduction in its mechanical strength. Providing its thermal resistance remains low enough for the application, this solder attach is expected to survive many more cycles before failure.

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6. References

- [1] C. Buttay, D. Planson, B. Allard, D. Bergogne, P. Bevilacqua, C. Joubert, M. Lazar, C. Martin, H. Morel, D. Tournier, C. Raynaud, *State of the art of high temperature power electronics*, Materials Science and Engineering: B 176 (4) (2011) 283–288, microtechnology and Thermal Problems in Electronics. doi:10.1016/j.mseb.2010.10.003.

- [2] C. M. Johnson, P. J. Palmer, *A Joint IeMRC-EEPKTN Power-electronics Roadmap 2007*, Wolfson School of Mechanical and Manufacturing Engineering, Loughborough University, Loughborough, Leics LE11 3TU (2008).
- [3] S. Yang, A. Bryant, P. Mawby, D. Xiang, L. Ran, P. Tavner, *An Industry-Based Survey of Reliability in Power Electronic Converters*, IEEE transactions on industry applications 47 (3) (2011) 1441–1451. doi:10.1109/TIA.2011.2124436.
- [4] V. Manikam, K. Y. Cheong, *Die Attach Materials for High Temperature Applications: A Review*, Components, Packaging and Manufacturing Technology, IEEE Transactions on 1 (4) (2011) 457–478. doi:10.1109/TCPMT.2010.2100432.
- [5] R. Khazaka, L. Mendizabal, D. Henry, R. Hanna, *Survey of High-Temperature Reliability of Power Electronics Packaging Components*, Power Electronics, IEEE Transactions on 30 (5) (2015) 2456–2464. doi:10.1109/TPEL.2014.2357836.
- [6] S. Pietranico, S. Pommier, S. Lefebvre, Z. Khatir, S. Bontemps, *Characterisation of power modules ceramic substrates for reliability aspects*, Microelectronics Reliability (49) (2009) 1260–1266. doi:10.1016/j.microrel.2009.06.026.
- [7] *Bending strength of ceramics for curamik substrates*, Technical note, Rogers Corporation (2016).
- [8] H. A. Mustain, A. B. Lostetter, W. D. Brown, *Evaluation of Gold and Aluminum Wire Bond Performance for High Temperature (500 degC) Silicon Carbide (SiC) Power Modules*, in: Proceedings of the 2005 Electronic Components and Technology Conference (ECTC05), IEEE, 2005, pp. 1623–1628. doi:10.1109/ECTC.2005.1442008.
- [9] S. Kraft, A. Schletz, M. März, *Reliability of Silver Sintering on DBC and DBA Substrates for Power Electronic Applications*, in: Integrated Power Electronics Systems (CIPS), 2012 7th International Conference on, IEEE, 2012, pp. 1–6.
- [10] S. Riches, C. Johnston, A. Lui, *Effectiveness of barrier layer metallisations in long term high temperature endurance tests on wire bond interconnections*, in: Proceedings of the High Temperature Electronics Network (HiTEN) Conference, 2013, Vol. 2013, International Microelectronics Assembly and Packaging Society, 2013, pp. 229–236. doi:10.4071/HITEN-WA14.
- [11] L. Dupont, Z. Khatir, S. Lefebvre, S. Bontemps, *Effects of metallization thickness of ceramic substrates on the reliability of power assemblies under high temperature cycling*, Microelectronics Reliability 46 (9) (2006) 1766 – 1771. doi:10.1016/j.microrel.2006.07.057.
- [12] F. Arabi, L. Theolier, D. Martineau, J.-Y. Deletage, M. Medina, E. Woizard, *Power electronic assemblies: Thermo-mechanical degradations of gold-tin solder for attaching devices*, Microelectronics Reliability 64 (2016) 409 – 414. doi:http://dx.doi.org/10.1016/j.microrel.2016.07.028.
- [13] Z. Zhu, C. Li, L. Liao, C. Liu, C. Kao, *Au–sn bonding material for the assembly of power integrated circuit module*, Journal of Alloys and Compounds 671 (2016) 340 – 345. doi:http://dx.doi.org/10.1016/j.jallcom.2016.02.065.
- [14] R. Schmidt, C. König, P. Prenosil, *Novel wire bond material for advanced power module packages*, Microelectronics Reliability 52 (2012) 2283–2288. doi:10.1016/j.microrel.2012.06.139.
- [15] M. Ciappa, *Selected failure mechanisms of modern power modules*, Microelectronics Reliability 42 (4-5) (2002) 653–667. doi:DOI:10.1016/S0026-2714(02)00042-2.

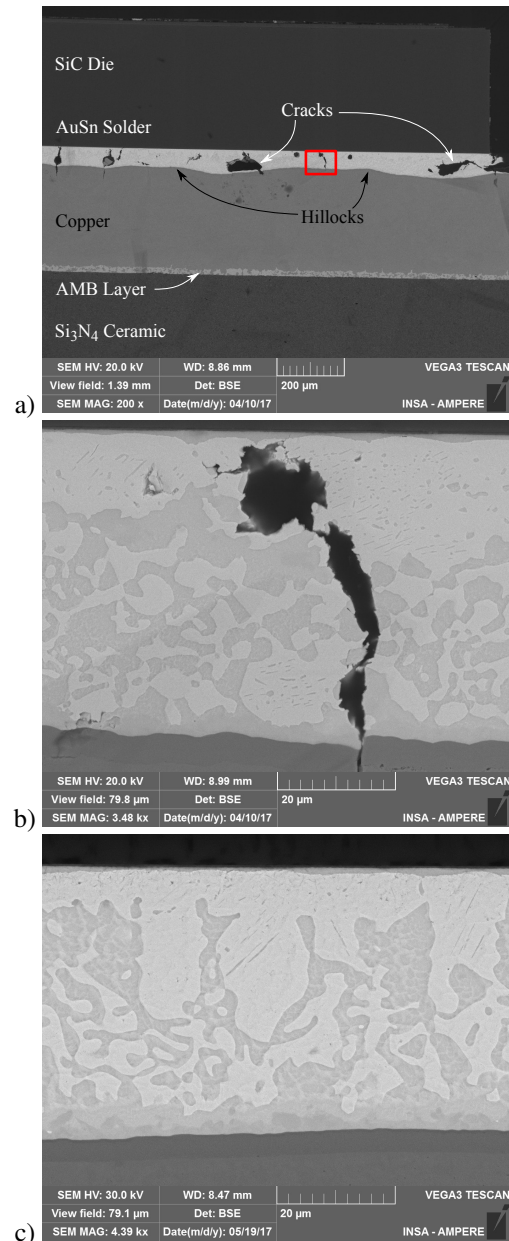


Figure 10: Cross section of the die attach after 3000 RTC cycles (corresponding to 750 h at 175 °C). A clear coarsening of the copper surface is visible, forming hillocks. Many cracks are visible in the AuSn layer. (b) is an enlargement of the area highlighted in (a). (c) is a cross section of a sample stored at 175°C for 840 h (approximately the same time spent at 175 °C as 3000 RTC), which shows a microstructure which is comparable with (b).