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Impact of Gate–Drain Spacing on Low-Frequency Noise Performance of *In Situ* SiN Passivated InAlGaN/GaN MIS-HEMTs

Mehdi Rzin, Jean-Marc Routoure, Bruno Guillet, Laurence Méchin, Magali Morales, Cédric Lacam, Piero Gamarra, Pierre Ruterana, and Farid Medjdoub

Abstract—In this paper we investigated the gate–drain access region spacing (L_{GD}) effect on electrical and noise performance of InAlGaN/GaN metal–insulator–semiconductor high electron mobility transistors (MIS-HEMTs) using *in situ* SiN cap layer as gate insulator. Different L_{GD} of InAlGaN/GaN MIS-HEMTs using sub-10 nm barrier layer are studied. Low-frequency noise measurements have been carried out for the first time in order to analyze the impact of the gate–drain spacing on the electrical characteristics. The noise of the channel under the gate has been identified as the dominant channel noise source for $L_{GD} < 10 \mu\text{m}$. Finally, the calculated Hooge parameter (α_H) is equal to 3.1×10^{-4} . It reflects the high material quality while using sub-10 nm InAlGaN layer, which is promising for high-frequency applications.

Index Terms—Channel resistance, gate–drain spacing, *in situ* sin passivation, InAlGaN/GaN, low-frequency noise (LFN), metal–insulator–semiconductor high electron mobility transistor (MIS-HEMT).

I. INTRODUCTION

GaN-based high electron mobility transistors (HEMTs) have demonstrated their potential for telecommunication and power applications owing to the high electrical breakdown field (3.3 MV/cm) and the high electron mobility ($2 \times 10^3 \text{ cm}^2 \cdot \text{V}^{-1} \cdot \text{s}^{-1}$) of GaN material [1]. Extensive research and technology development enabled GaN-based HEMTs to significantly improve over the last two decades.

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Highly scaled GaN devices using the standard AlGaN barrier layer are inherently limited by short-channel effects due to low aspect ratio of the gate length to barrier layer thickness [3]. Moreover, the Al content and the thickness of AlGaN layer are limited by strain relaxation issues inducing cracks [4]. Lattice-matched AlInN has emerged as a promising alternative to AlGaN barrier layer due to the absence of stress and piezoelectric polarization [5]. AlInN spontaneous polarization is higher compared to AlGaN, allowing higher 2-DEG sheet carrier density. Also, AlInN has less surface depletion effects than AlGaN, which allows thinner barrier layers to be used while maintaining high aspect ratio down to short gate lengths with high 2-DEG charge density. The combination of AlGaN and AlInN as a quaternary (InAlGaN) allows to independently adjusting the bandgap and lattice constant to avoid the formation of cracks by controlling the built-in strain [6]. Also, the use of Al-rich InAlGaN layers has a great potential to enhance the carrier density and achieve high-frequency performances due to the increase of the spontaneous polarization [7]–[14].

One of the major factors hindering dynamic and power performance as well as the electrical reliability of GaN-based HEMTs is the gate leakage current that might increase under high electric field. In order to reduce the leakage current under the gate and/or in the gate–drain access region, the deposition of an *in situ* SiN passivation layer in the metal organic vapor phase epitaxy (MOVPE) reactor has been proposed and successfully applied. The insulator layer deposited in the same growth run as the III-N heterostructure reduces the relaxation, cracking and surface roughness of the barrier layer [15]. Moreover, the low growth rate and the high growth temperature of *in situ* SiN layer reduce the formation of surface states and improve the performance of the 2-DEG properties. The thickness of *in situ* SiN gate dielectric has a significant impact on the leakage current and may also affect the drain current.

Low-frequency noise (LFN) measurements are an effective tool to investigate the material/device quality and allows to study material defects [16], trapping effects and also to investigate the reliability of GaN-based HEMTs, especially when performed at various temperatures [17], [18].

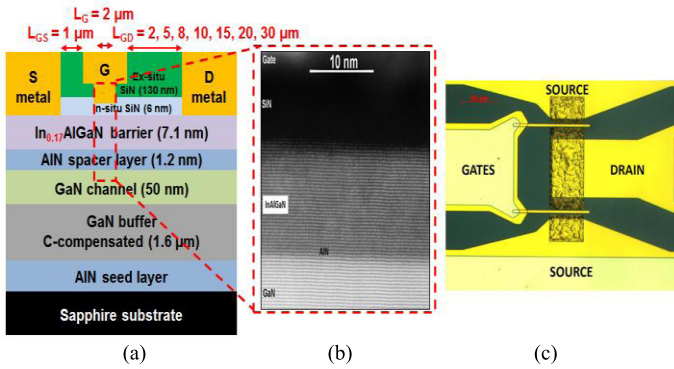


Fig. 1. (a) Schematic cross-sectional view. (b) TEM image. (c) Optical microscope image of $\text{Si}_x\text{N}_y/\text{InAlGaN}/\text{AlN}/\text{GaN}$ HEMTs with two finger gates.

Besides, the *in situ* SiN passivation layer not only reduces significantly the gate leakage current but also potentially improves the low-frequency device noise performance [19].

In this paper, we report on the impact of the increase of gate–drain spacing (L_{GD}) on the performance of *in situ* SiN passivated InAlGaN/GaN MIS-HEMTs, grown on sapphire substrate.

A study of drain current LFN spectral density S_{ID} is performed to identify the possible noise sources in the channel. By correlating the channel LFN contributions and the electrical parameters (maximum drain current, threshold voltage, transconductance, and leakage current), we point out that the *ex situ/in situ* SiN passivation layers interface is problematic for large L_{GD} due to contaminants that induce trapping effects.

II. SAMPLE DETAILS

The InAlGaN/GaN heterostructure was grown by low-pressure MOVPE (LP-MOVPE) deposition on sapphire substrate. The devices under test have an average electron mobility of $1060 \text{ cm}^2 \cdot \text{V}^{-1} \cdot \text{s}^{-1}$ and a sheet carrier density of $1.74 \times 10^{13} \text{ cm}^{-2}$, resulting in a sheet resistance of $340 \text{ } \Omega/\square$.

The heterostructure consists of a low-temperature GaN nucleation layer, a 1.6- μm -thick highly resistive carbon-compensated GaN buffer layer, a 50-nm-thick nonintentionally doped GaN channel, followed by a 1.2-nm-thick AlN interlayer, and a 7.1-nm-thick-undoped InAlGaN layer. The given thicknesses are nominal values.

Ohmic contacts were formed directly on the top of the InAlGaN barrier layer by etching the *in situ* layer. A Ti/Al/Ni/Au metal stack was used, followed by a rapid thermal annealing at $875 \text{ }^\circ\text{C}$. Device isolation was achieved by nitrogen implantation. A Ni/Au T-gate of $2 \text{ } \mu\text{m}$ length (L_G) was defined by optical lithography. An additional *ex situ* SiN passivation layer of 130 nm is then deposited by plasma-enhanced chemical vapor deposition.

The device has two finger gates with a total gate width of $W_G = 100 \text{ } \mu\text{m}$. In this paper, different gate–drain spacing from 2 to $30 \text{ } \mu\text{m}$ was studied [Fig. 1(c)]. The schematic of the HEMT heterostructure is displayed in Fig. 1(a).

High resolution annular dark field scanning transmission micrograph [Fig. 1(b)] exhibits chemical contrast and the

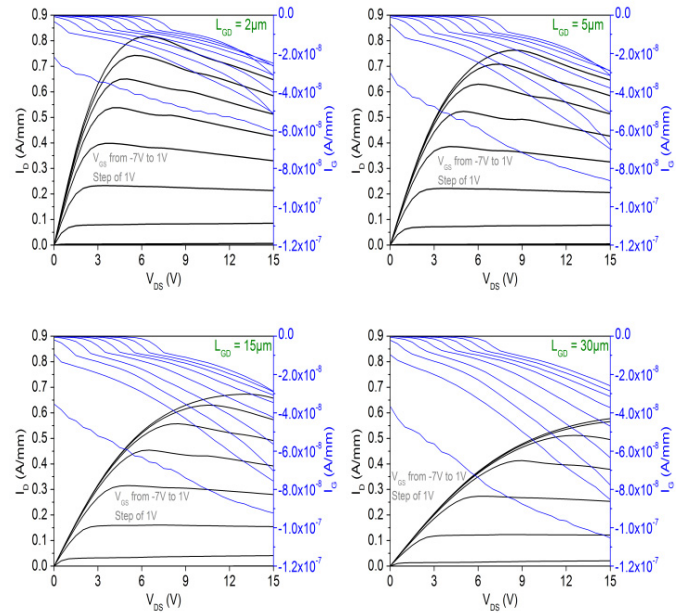


Fig. 2. Output characteristics of InAlGaN/GaN HEMTs with $L_{GD} = 2, 5, 15,$ and $30 \text{ } \mu\text{m}$ for V_{GS} from -7 to 1 V .

low- z materials show a darker contrast, the observed areas are of extremely good crystalline quality with no defects [20]. As measured directly in this figure, the thickness of the layers is obtained by counting the visible (0002) lattice fringes (0.25 nm), and the agreement with the nominal thickness is attested with 1.2–1.3 nm of AlN, and 7.1–7.2 nm for the InAlGaN top layer.

III. RESULTS AND DISCUSSION

A. DC Measurements

Fig. 2 shows the output I_D – V_{DS} and I_G – V_{DS} characteristics of InAlGaN/GaN HEMTs with $L_{GD} = 2, 5, 15,$ and $30 \text{ } \mu\text{m}$ for V_{GS} from -7 to 1 V .

The output characteristics of InAlGaN/GaN MIS-HEMTs with $L_{GD} = 2 \text{ } \mu\text{m}$ show a maximum drain current $I_{D\text{max}}$ (I_D at $V_{GS} = 0 \text{ V}$ and $V_{DS} = 10 \text{ V}$) of about 800 mA/mm and drain–source resistance $R_{DS} = 4 \text{ } \Omega \cdot \text{mm}$ at $V_{GS} = 1 \text{ V}$. The increase of L_{GD} from 2 to $30 \text{ } \mu\text{m}$ induces a decrease of $I_{D\text{max}}$ and an increase of R_{DS} . The degradation of I_D and R_{DS} achieves, respectively 25% and 70% for $L_{GD} = 30 \text{ } \mu\text{m}$ compared to $L_{GD} = 2 \text{ } \mu\text{m}$.

The gate leakage current (I_G) increases with L_{GD} as well, but not significantly and remains much lower than in devices with Schottky gate contact. For example, $I_G = 100 \text{ nA/mm}$ at $V_{GS} = -10 \text{ V}$ and $V_{DS} = 15 \text{ V}$.

The drain–source resistance (R_{DS}) can be described as the sum of the source (R_S) and drain (R_D) contact resistances, the gate–source (R_{GS}) and gate–drain (R_{GD}) access region resistances, and the channel resistance under the gate R_{CH} as shown in Fig. 3 and described in (1). Hereafter the resistance values are given in $\Omega \cdot \text{mm}$ (normalized with 1-mm gate width)

$$R_{DS} = R_S + R_{GD} + R_{CH} + R_{GS} + R_D. \quad (1)$$

Fig. 4 shows I_D – V_{DS} characteristics of InAlGaN/GaN HEMTs with $L_{GD} = 2, 5, 15,$ and $30 \text{ } \mu\text{m}$ at $V_{GS} = 0 \text{ V}$ and

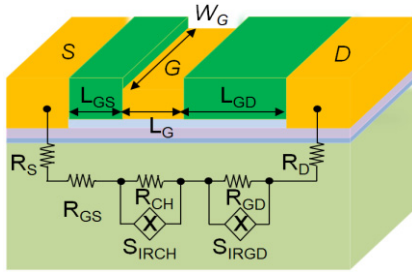


Fig. 3. Schematic of the SiN/InAlGaN/AlN/GaN HEMT showing R_S and R_D contact resistances, channel resistance under the gate R_{CH} and in access regions R_{GS} and R_{GD} , and current source noise of the channel under the gate S_{IRCH} and in gate–drain access region S_{IRGD} .

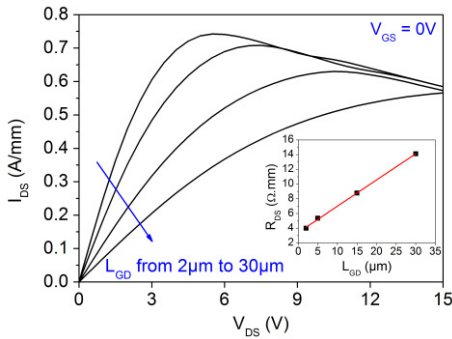


Fig. 4. I_D – V_{DS} of InAlGaN/GaN HEMTs at $V_{GS} = 0$ V with $L_{GD} = 2, 5, 15,$ and $30 \mu\text{m}$. Inset: R_{DS} as function of L_{GD} .

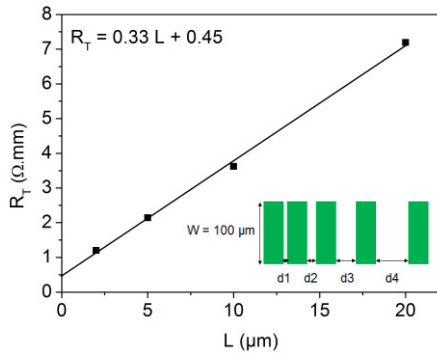


Fig. 5. Normalized TLM total resistance R_T versus lead separation L .

the inset shows the linear dependence of the drain–source resistance (R_{DS}) on the gate–drain spacing (L_{GD}) as follows:

$$R_{DS} = \beta L_{GD} + \gamma. \quad (2)$$

R_S , R_D , and R_{GS} are extracted from transmission line model (TLM) structures with $W = 100 \mu\text{m}$ and four lengths ($L = 2, 5, 10,$ and $20 \mu\text{m}$) as shown in Fig. 5.

From the fitting of experimental data (see dotted line in the inset of Fig. 4)

$$R_{DS} = 0.35 L_{GD} + 3.42(\Omega \cdot \text{mm}). \quad (3)$$

The total TLM resistance R_T in ohm is described by (4) having two terms. The first term is directly proportional to L , the separation between leads, and accounts for the contribution of the sheet resistance R_{sheet} . The second term is twice the

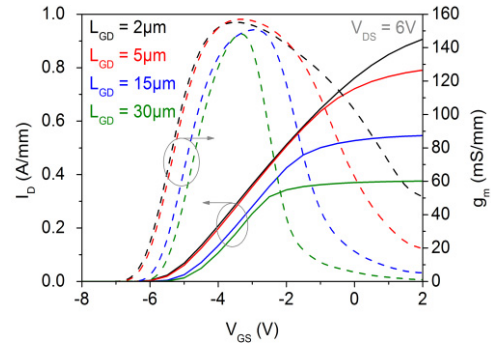


Fig. 6. I_D – V_{GS} and g_m – V_{GS} of InAlGaN/GaN HEMTs with $L_{GD} = 2, 5, 15,$ and $30 \mu\text{m}$ at $V_{DS} = 6$ V.

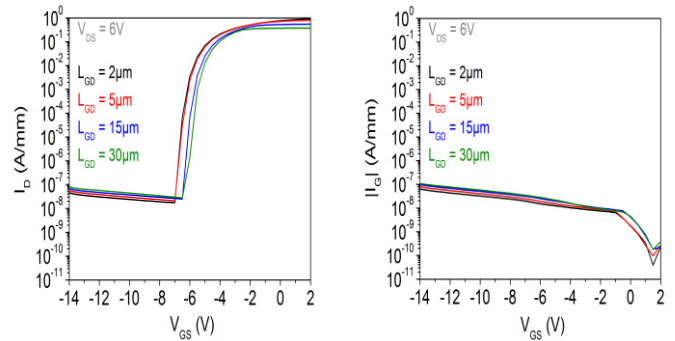


Fig. 7. I_D – V_{GS} and $|I_G|$ – V_{GS} in logarithmic scale of InAlGaN/GaN HEMTs with $L_{GD} = 2, 5, 15,$ and $30 \mu\text{m}$ at $V_{DS} = 6$ V.

contact resistance R_C

$$R_T = \frac{R_{\text{sheet}}}{W} L + 2R_C. \quad (4)$$

From the fitting of experimental data (see dotted line showed in Fig. 5) the normalized R_T is as follows:

$$R_T = 0.33L + 0.45(\Omega \cdot \text{mm}). \quad (5)$$

From (4) and (5), $R_C = R_S = R_D = 0.22 (\Omega \cdot \text{mm})$ and the sheet resistance $R_{\text{sheet}} = 333 \Omega/\square$ similar to the value obtained by Hall measurements.

Gate–source resistance is obtained by the following equation with $L_{GS} = 1 \mu\text{m}$:

$$R_{GS} = 0.35 L_{GS}(\Omega \cdot \text{mm}). \quad (6)$$

From (3), (5), and (6), we extract the values of $R_{GS} = 0.35 \Omega \cdot \text{mm}$ and $R_{CH} = 2.63 \Omega \cdot \text{mm}$.

I_D – V_{GS} and g_m – V_{GS} characteristics of MIS-HEMTs with L_{GD} from 2 to 30 μm at $V_{DS} = 6$ V are reported in Fig. 6. Devices with $L_{GD} = 2 \mu\text{m}$ show a threshold voltage of -5.4 V. The threshold voltage is shifted to positive values by increasing L_{GD} to achieve -4.7 V for $L_{GD} = 30 \mu\text{m}$. This shift occurs also at very low V_{DS} ($V_{DS} < 0.3$ V) at which trapping effects are minimal. Moreover, the peak transconductance and the transconductance width decrease by increasing L_{GD} . The gate and drain subthreshold leakage currents remain below 100 nA/mm for all the gate–drain spacing (Fig. 7), which show the efficiency of the *in situ* SiN passivation.

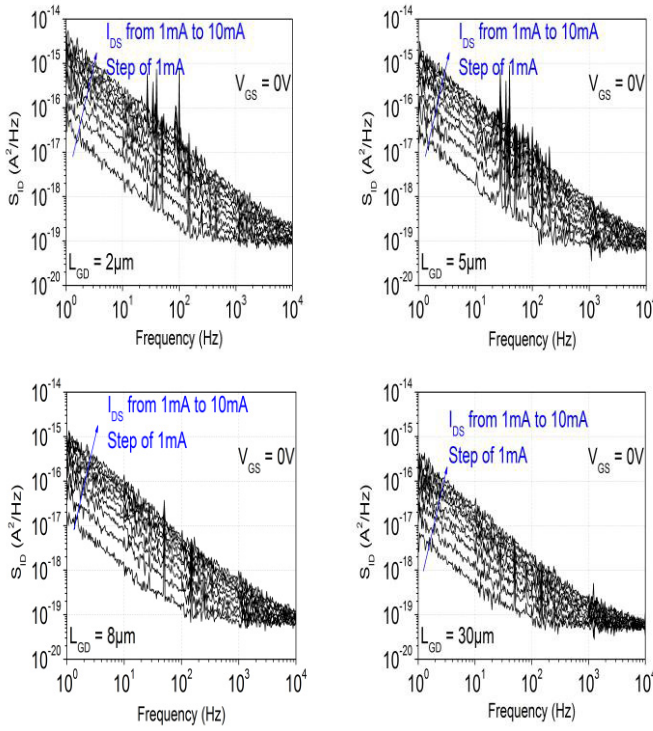


Fig. 8. PSD of the drain current S_{ID} of InAlGaN/GaN HEMTs with $L_{GD} = 2, 5, 8,$ and $30 \mu\text{m}$ at $V_{GS} = 0 \text{ V}$ and for I_{DS} from 1 to 10 mA at room temperature.

The increase of L_{GD} induces the rise of the 2-DEG channel resistance which causes the decrease of the output current and the peak transconductance. Since *in situ* SiN/InAlGaN interface is considered of high quality [21], we assume that the increase of the drain-source resistance is caused by the increase of gate-drain access resistance.

B. Low-Frequency Noise Measurements

The LFN measurement is used first as a figure of merit to investigate the material and device quality. By using the measurements performed on various gate-drain spacing, it has been possible to distinguish channel and access region noise and thus to calculate the Hooge figure of merit for the channel contribution. The power spectral density (PSD) of the drain current S_{ID} was measured in the linear regime at $V_{GS} = 0 \text{ V}$ for I_D from 1 to 10 mA to identify the dominant noise sources in the channel with different gate-drain spacing (L_{GD}).

The PSD of the drain current (S_{ID}) is shown in Fig. 8 for different L_{GD} . S_{ID} varies as $1/f^\gamma$ type spectra with γ close to 1. It is worth mentioning that the noise measurements were carried out on fresh devices under stationary conditions and were reproducible. No distinct generation-recombination noise components were identified.

The PSD of the drain current decreases by increasing L_{GD} from 2 to $30 \mu\text{m}$. Chiu *et al.* [22] have reported on an increase of S_{ID}/I_D^2 with L_{GD} extension of AlGaIn/GaN HEMTs and associated the enhancement of LFN to the increase of R_{on} .

The $1/f^\gamma$ noise of S_{ID} is extracted from the spectrum at $f = 1 \text{ Hz}$ and plotted as function of the square of

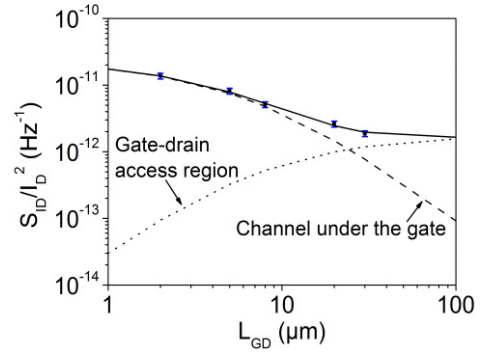


Fig. 9. Dependence of the relative PSD of the drain current S_{ID}/I_D^2 on the gate-drain spacing L_{GD} in the linear regime at $f = 1 \text{ Hz}$, $V_{GS} = 0 \text{ V}$, and $T = 300 \text{ K}$. Dashed line represents the channel noise contribution under the gate. Dotted line shows the noise channel contribution in gate-drain access region. Solid line shows total channel noise.

the drain current (I_D^2). The experimental points representing the normalized PSD (S_{ID}/I_D^2) of the drain current are plotted against the gate-drain spacing in the linear regime at $V_{GS} = 0 \text{ V}$ at 300 K in Fig. 9.

The S_{ID}/I_D^2 dependence on L_{GD} is analyzed by considering two noise sources in the channel: channel noise under the gate and channel noise in the gate-drain access region.

The source noise of the gate-source access region is not considered in our model since it is not dominant. Since, $L_{GS} = 1 \mu\text{m}$, the gate-source noise contribution is similar to the one of gate-drain access region for $L_{GD} = 1 \mu\text{m}$ (Fig. 9).

Based on the assumptions considered above and that the noises originating from these regions are uncorrelated, the relative PSD of the drain current can be presented as follows:

$$\frac{S_{ID}}{I_D^2} = \frac{R_{CH}^2}{R_{DS}^2} \frac{S_{IRCH}}{I_D^2} + \frac{R_{GD}^2}{R_{DS}^2} \frac{S_{IRGD}}{I_D^2} \quad (7)$$

where S_{IRCH} , S_{IRGD} are the drain current source noise of the channel under the gate and in the gate-drain access region, respectively.

By replacing R_{GD} with its dependence on L_{GD} from (3), (7) becomes

$$\frac{S_{ID}}{I_D^2} = \frac{R_{CH}^2}{(\beta L_{GD} + \gamma)^2} \frac{S_{IRCH}}{I_D^2} + \frac{\beta L_{GD}^2}{(\beta L_{GD} + \gamma)^2} \frac{S_{IRGD}}{I_D^2}. \quad (8)$$

Dashed line in Fig. 9 represents the channel noise contribution under the gate calculated by the first term of (8). The experimental points fit well this contribution for $L_{GD} < 10 \mu\text{m}$. The dotted line corresponding to the channel noise contribution in the gate-drain access region is obtained from the second term of (8). It allows to compensate the slight difference between the experimental points and the channel under the gate contribution for $L_{GD} > 10 \mu\text{m}$.

Solid line representing the total channel noise fits well the experimental points. This result shows that the dominant channel source noise contribution at $V_{GS} = 0 \text{ V}$ is located under the gate and a slight contribution of gate-drain access region is noticed for $L_{GD} > 10 \mu\text{m}$.

A dependence of S_{ID} proportional to I_D^2 is seen for the different L_{GD} in Fig. 10. The Hooge parameter (α_H) associated

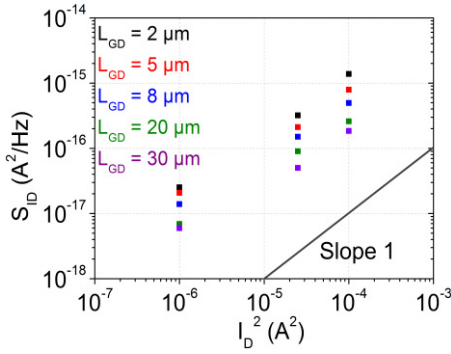


Fig. 10. PSD of the drain current S_{ID} at 1 Hz as function of drain current square with $L_{GD} = 2, 5, 8, 20,$ and $30 \mu\text{m}$.

with the channel noise under the gate can be written as

$$\frac{S_{ID}}{I_D^2} = \frac{\alpha_H}{Nf} \quad (9)$$

where f is the frequency and N is the total number of carriers in the channel under the gate.

The number of carriers is given by

$$N = \frac{L_{CH}^2}{q\mu R_{CH}} \quad (10)$$

where q is the electron charge, μ is the mobility in the channel, R_{CH} is the channel resistance under the gate and L_{CH} is the channel length.

The Hooge parameter has been calculated for the smallest L_{DS} device for which the access region noise is negligible. It is equal to 3.1×10^{-4} . The value of this parameter, considered as a figure of merit for the InAlGaN/GaN interface quality, is in the range of $10^{-3} - 10^{-4}$, pointing out the good quality of InAlGaN/GaN interface [23]–[25]. This paper shows the first LFN measurements on InAlGaN/GaN HEMTs using sub-10 nm InAlGaN layer and *in situ* SiN passivation layer. Sub-10 nm InAlGaN quaternary barrier combined with *in situ* SiN passivation layer are promising to enhance the performance of GaN-based HEMTs.

IV. CONCLUSION

The effect of gate–drain spacing on the electrical and noise performance of InAlGaN/GaN MIS-HEMTs by using *in situ* SiN passivation layer was investigated by dc and LFN measurements.

The increase of L_{GD} induces the degradation of the maximum drain current and the transconductance and a positive shift of the threshold voltage. The subthreshold leakage current remains very low ($<100 \text{ nA/mm}$) and does not increase significantly with L_{GD} which demonstrates the efficiency of the *in situ* SiN passivation.

The PSD of the drain current varies as $1/f^2$ noise without distinct generation–recombination noise components. The noise level decreases with L_{GD} . The channel noise under the gate is the main contribution of the total channel noise for $L_{GD} < 10 \mu\text{m}$ while a nonnegligible contribution of the gate–drain access region is noticed for $L_{GD} > 10 \mu\text{m}$. The low value of the Hooge parameter of the dominant channel noise (3.1×10^{-4}) indicates a high InAlGaN/GaN interface quality while using sub-10 nm InAlGaN barrier layer.

In order to use $L_{GD} > 10 \mu\text{m}$ to enhance the breakdown voltage of this process, a careful engineering of the *in situ* SiN/*ex situ* passivation layers interface is needed.

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