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Etienne Sicard. Introducing 10-nm FinFET technology in Microwind. 2017. ⟨hal-01551695⟩

HAL Id: hal-01551695

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Introducing 10-nm FinFET technology in Microwind

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This paper describes the implementation of a high performance FinFET-based 10-nm CMOS Technology in Microwind. New concepts related to the design of FinFET and design for manufacturing are also described. The performances of a ring oscillator layout and a 6-transistor RAM memory layout are also analyzed.

1. Technology Roadmap

Several companies and research centers have released details on the 14-nm CMOS technology, as a major step for improved integration and performances, with the target of 7-nm process by 2020. We recall in table 1 the main innovations over the past recent years.

Technology node	Year of introduction	Key Innovations	Application note
180nm	2000	Cu interconnect, MOS options, 6 metal layers	
130nm	2002	Low-k dielectric, 8 metal layers	
90nm	2003	SOI substrate	[Sicard2005]
65nm	2004	Strain silicon	[Sicard2006]
45nm	2008	2nd generation strain, 10 metal layers	[Sicard2008]
32nm	2010	High-K metal gate	[Sicard2010]
20nm	2013	Replacement metal gate, Double patterning, 12 metal layers	[Sicard2014]
14nm	2015	FinFET	[Sicard2017]
10nm	2017	FinFET, double patterning	This application note
7nm	2019	FinFET, quadruple patterning	

Table 1: Most significant technology nodes over the past 15 years

Improved performances

The power, performance and area gains are an important metric for justifying a shift from older technology nodes to new ones.

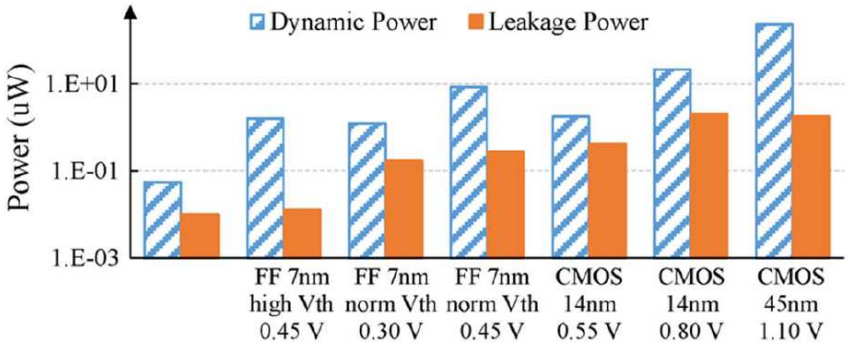


Figure 1: The reduction of feature sizes from 45 to 7nm may induce drastic gains in power consumption and leakage power [Xie2015]

As compared to 14-nm technology node, the 10-nm technology offers [Brain2017, Mistry2017]:

- 30 % less power consumption. This is a key feature for mobile industry for which the battery life is the top one problem.
- 10 to 20 % increase in switching performance. This is equally important in server applications and smartphones, which use faster processors and higher resolution screens.
- 2 times higher density. This is a key advantage to produce the lightest and thinnest possible smartphones.

A comparison between 45nm, 32, 22, 14 and 10nm technologies in terms of density is proposed by [Brain2017] are reported in Fig. 2. The IC surface is shrunk by a factor of 13 between 45-nm and 10-nm nodes.

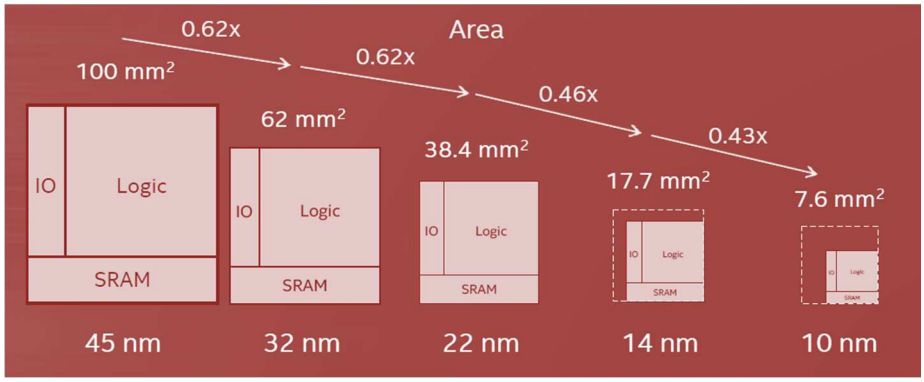


Figure 2: The evolution of silicon area with the technology nodes as presented by Intel [Brain2017]

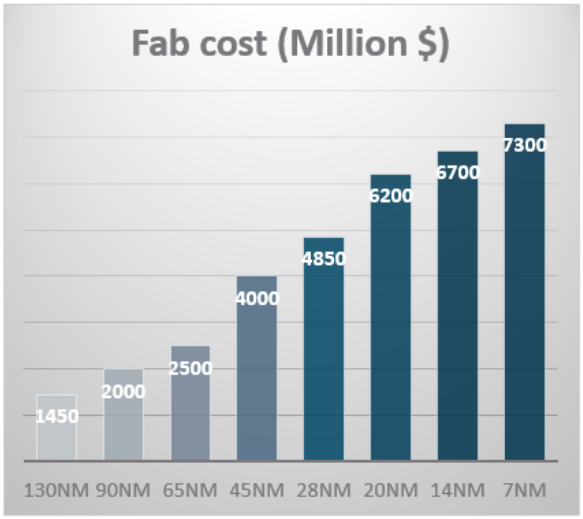
The giant cost of fab and IC design in 10-nm

The consequences of the fab and chip design cost explosion is the drastic decrease of foundries. While more than 20 foundries existed for 130nm technology, only four major companies are providing the 10-7nm processes (Table 2). One reason is the extraordinary fab and IC design cost, as illustrated in Figure 4.

Company	Logo	Technology name
Intel		10nm, 10nm+, 10nm++
Samsung		10nm
TSMC		10nm, 7nm, 5nm
GlobalFoudries		7nm

Table 2: 4 major players in the 10/7/5-nm chip manufacturing

Figure 3: Examples of 10-nm processors and prototype 7-nm circuit by IBM



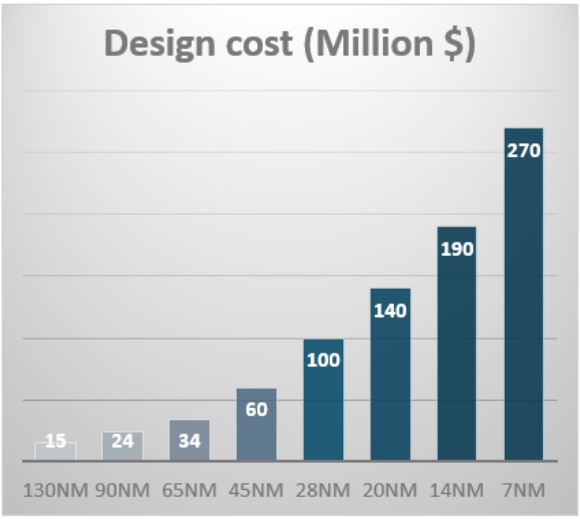


Figure 4: The extraordinary increase of the fab cost: more than 7 billion $ for a 10-7-nm process, and associated chip design cost as high as 270M$ for a run in 7-nm.

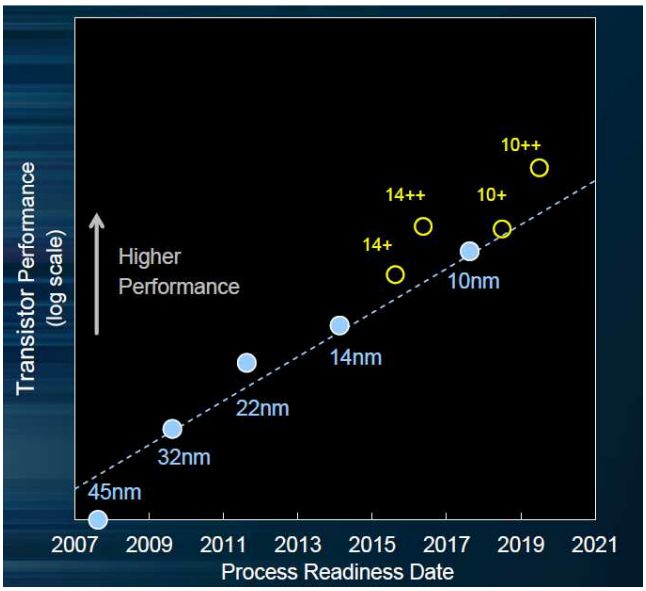


Figure 5: Examples of multi-giga-transistor processors used in mobiles, laptops and servers from various companies [Mistry2017].

Some examples of processors used in mobile phones, laptops and servers are reported in Fig. 3, with complexity approaching 10 Billion devices. Within a same technology node, improvements are made over the years, such as Intel who plans to improve its original process “10nm” with the "10nm+" offering 10% higher drive current, followed by "10nm++" process with supplementary 10% higher drive current [Mistry2017]. Similar trends were observed for Intel’s 14nm, 14nm+ and 14++ technology as illustrated in Fig. 5 [Mistry2017].

A continuous increase in switching performance has been made possible thanks to several innovations, as shown in Figure 6. Starting 14-nm, the MosFET is replaced by the FinFET, for improved current capabilities.

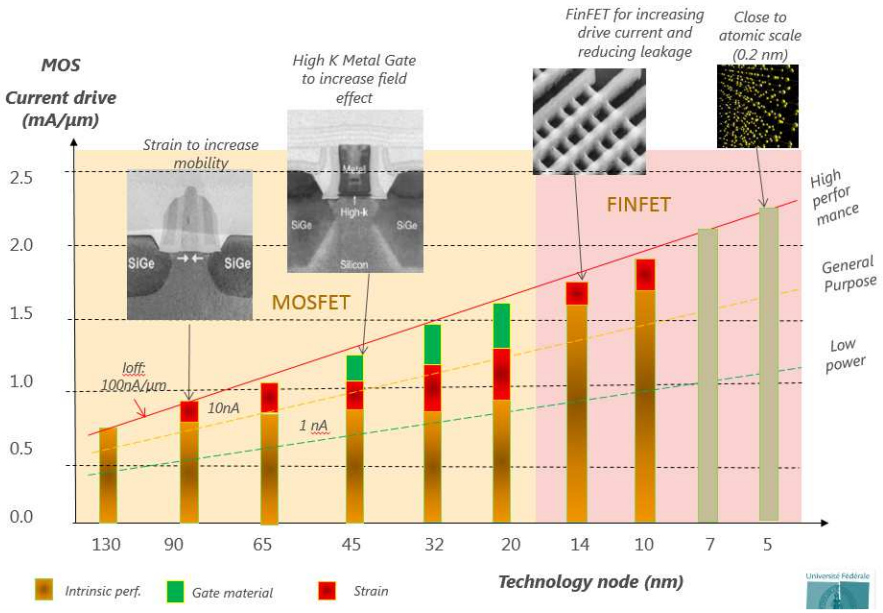


Figure 6: Increased switching speed capabilities over technology nodes

10-nm Process variants

Within the same "10-nm" label, we may observe a wide variety of performances, depending whether the IC fabrication process is targeted to "high performance" (HP) devices (speed whatever the power consumption), "general purpose" (GP) or "Low Power" (LP) (lower speed but power-efficient), as summarized in Table 3. We implement in Microwind the general purpose 10-nm process.

10-nm Technology variant	Pros	Cons	Target application	Typical Ion/Ioff
General purpose	Medium speed	Medium consumption	Laptops	1.4 mA/µm 10 nA/µm
High performance	Fast speed	High consumption	Servers	1.8 mA/µm 100nA/µm
Low power	Low speed	Low consumption	Smartphones	1.1 mA/µm 1 nA/µm

Table 3: technology variants within the same node

Power supply operation

The supply voltage, both internal to the cores and the external I/O supply have been continuously decreased due to the thinning of the gate oxide and faster switching rates thanks to reduced voltage swings. The 10-nm technology operates around 0.7V, while I/Os are supplied at 1.2, 1.5 or 1.8 V (Fig. 5).

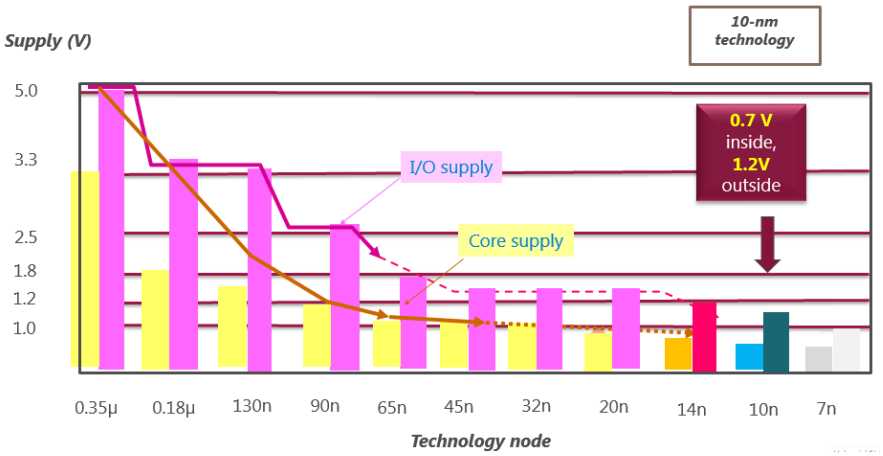


Figure 7: The core supply voltage in 10nm technology is 0.7 V, with typical IO voltage of 1.2 V

2. Key features of the 10-nm technology

Introducing the FinFET

The FinFET device has a different layout style than the MOS device. Instead of a continuous channel, the FinFET uses fins (Figure 8), which provide the same current at a smaller size. FinFET also provides a lower leakage current (Ioff) at the same (Ion) [Fischer2017]. High density (HD) designs use 2 fins, high performance (HP) designs 4 fins or more.

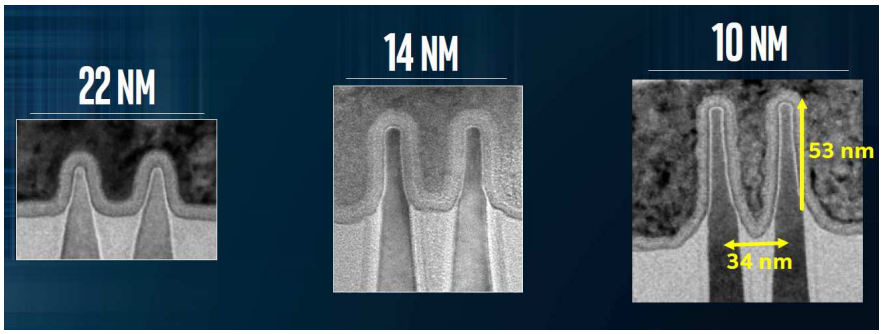
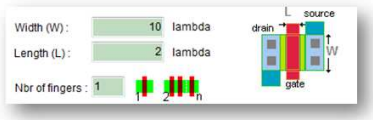


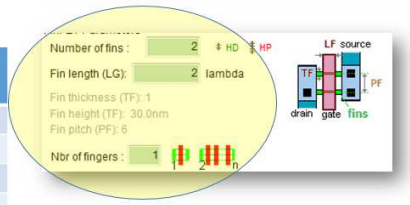
Figure 8: FinFet technology from Intel [Mistry2017] with increased fin height to improve the current drive.

MOS Parameter	Typical value
Width (W)	6 - 12 λ
Length (L)	2 λ



MosFET screen in Microwind

FinFET Parameter	Typical value
Number of fins (NF)	2 - 5
Fin pitch (PF)	6 λ
Fin thickness (TF)	1 λ
Fin length or gate length (LG)	2 λ



FinFET screen in Microwind

Figure 9: The introduction of the FinFET in Microwind, and comparison with traditional MosFET

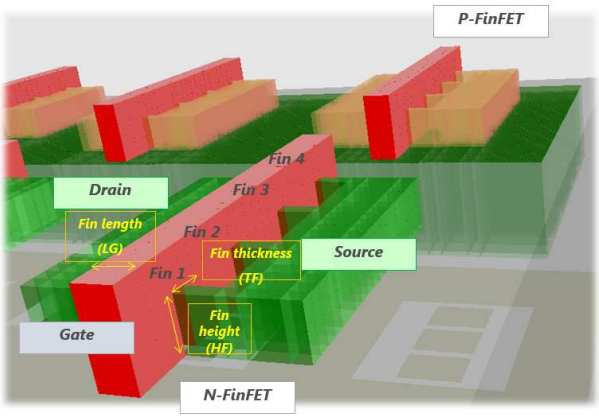


Figure 10: 3D view of the FinFET and illustrations of the Fin height (HF), Fin Thickness (TF) and Fin Length (LG).

Built on more than 15 years of FinFET research & development and solid foundation of high-K metal gate production experience, the 14 & 10-nm FinFET device reuses an important part of process elements from the previous 28-nm and 20-nm nodes, so that planar designs may be partially reused starting 14-nm and below. However, the Fin design is a totally new feature which contrasts with the traditional MOS design. This leads to new screens and new acronyms such as “Fin Pitch”, “Fin thickness”, etc, as shown in Figures 9 and 10.

Lambda

In Microwind, we use an integer unit for drawing, which is fixed to 6 nm for 10-nm CMOS process (Table 4).

- The drawn gate length is 2 λ that is 12 nm.
- The fin width is 1 λ that is 6 nm.
- The lower metal pitch is 36 nm.

Microwind parameter	Unit	Code	Name in rule file	10-nm process
Lambda	nm	λ	lambda	6
Core supply	V	VDD	Vdd	0.7
Fin Width	λ	WF	R301	1
Fin pitch	λ	FP	R308	6
Fin Height	nm	HF	thdn	40
Gate height	nm	GH	thpoly	60
Gate length	λ	GL	R302	2
Gate pitch	λ	GP		6
Spacer width	nm	SW		8
Contact size	λ	CS	R401	2
EOT	Nm	EOT	b4toxe	0.8
M1 pitch	λ		R501+R502	6

Table 4: key parameters of the 14-nm processes used to configure Microwind rule file Cmos10n.RUL

Core MOS devices

Table 4 gives an overview of the key parameters for the 10-nm technological node concerning the internal MOS devices and layers. Commercial 10-nm processes propose up to 3 threshold options, namely high-Vt (HVT), regular Vt (RVT), and low Vt (LVT).

- HVT – High Threshold Voltage causes less power consumption, but switching is slow. HVT are used in power critical functions.
- LVT – Low Threshold Voltage causes more power consumption and switching timing is optimized. LVT are used in time critical functions.
- RVT – Regular Threshold Voltage (sometimes called Standard VT or SVT) offers trade-off between HVT and LVT i.e., moderate delay and moderate power consumption.

In Microwind, we only use 2 types of MOS devices for the core and reuse the same name as for previous nano-CMOS technologies:

- Low leakage MOS (LL), close to RVT
- High Speed MOS (HS), close to LVT

Parameter	In Microwind
$V_{DD\ core}$ (V)	0.7
Effective gate length (nm)	12
MOS variants	2
Ion N (mA/µm) at 0.7V	1.3 (LL) 1.7 (HS)
Ion P (mA/µm) at 0.7V	1.1 (LL) 1.4 (HS)
Ioff N (nA/µm)	1 (LL) 10 (HS)
Ioff P (nA/µm)	1 (LL) 10 (HS)
Gate dielectric	HfO_2
Gate stack	Al/TiN
Equivalent oxide thickness (nm)	0.8

Table 4: Key features of the core devices proposed in the 10-nm technology

IO MOS devices

Table 5 gives an overview of the key parameters for the 14-nm technological concerning the Input/output MOS devices and associated supply voltage. In Microwind, we only consider 1.2V I/O supply and tune the "High-Voltage" (HV) MOS device on the median performances. Other standards usually supported in commercial 14-nm process include 1.2, 1.5 and 1.8V I/O supply.

Parameter	High Voltage (HV) MOS in Microwind
VDD IOs (V)	1.2
Effective gate length (nm)	100
Ion N (mA/µm)	0.3

IonP (mA/µm)	0.22
Ioff N (nA/µm)	0.1
Ioff P (nA/µm)	**0.1**

Table 5: Key features of the I/O devices proposed in the 10- nm technology and corresponding values in Microwind

3. Transistor performances in 10-nm technology

Designing a 1µm-width FinFET

The evaluation of the equivalent FinFET channel width corresponds to the following formulation (Eq. 1). The evaluation of the current is usually expressed in mA/µm, meaning that a 1-µm equivalent width FinFET design is needed to evaluate the current. In the proposed 10-nm technology, HFIN is 40nm, WFIN 6nm, so one fin has an equivalent width of 86 nm (Figure 11).

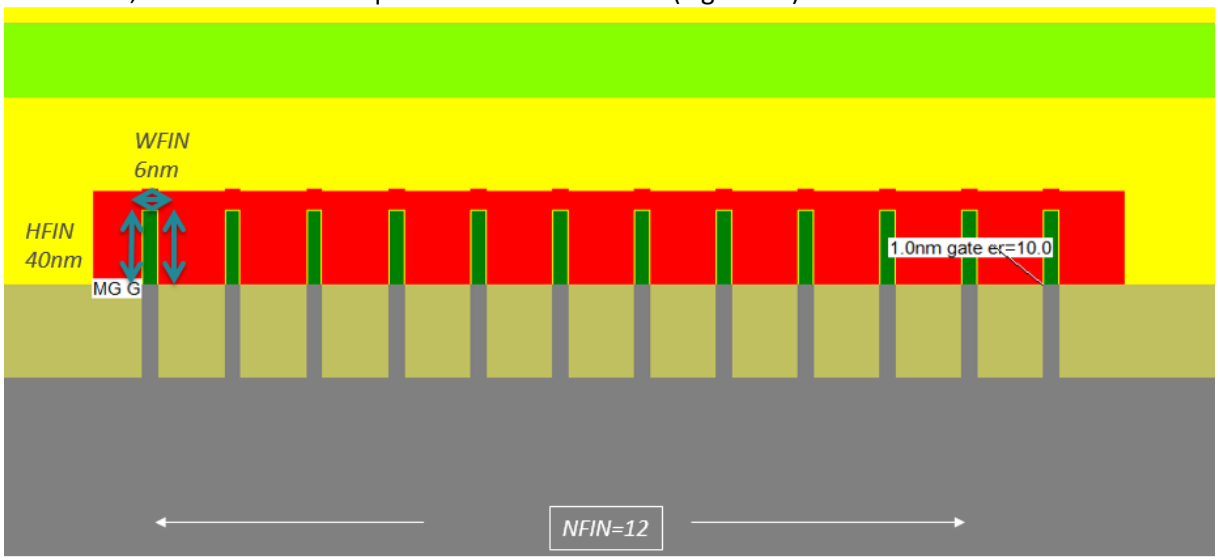


Figure 11: The equivalent width of a multi-fin FET

$$Weq = (2 \times H_{FIN} + W_{FIN}) \times N_{FIN} \qquad \text{Eq. 1}$$

$$Weq = (2 \times 40 + 6) \times 12 = 1032\ nm \approx 1\ \mu m \qquad \text{Eq. 2}$$

An equivalent width of 1µm, as it would be designed using MosFET's, corresponds to around 12 fins in 10-nm technology. As seen in Fig. 12, the FinFET with a 1-µm width is twice smaller than a MosFET with the same width. We get the following I/V characteristics (Fig. 12) for n-channel FinFET and p-channel FinFET.

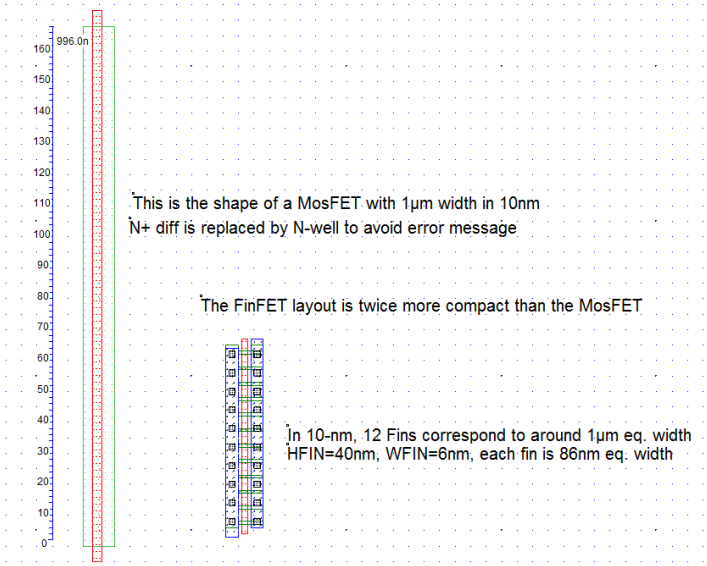


Figure 12: The 10-nm multi-fin FET with an equivalent width of 1 µm is twice more compact than the MosFET traditional design

n-FinFET characteristics

The I/V characteristics of the low-leakage and high-speed FinFET devices (Fig. 12) are obtained using the MOS model BSIM4. As shown in the figures, the low-leakage NMOS has a drive current capability of around 1.4 mA with 12 fins (equivalent to W=1.0 µm) at a voltage supply of 0.7 V. For the high speed NMOS, the drive current rises to 1.6 mA/µm. It is expected that 10+nm and 10++nm technology improvements will increase the Ion current by 10% at each iteration.

The drawback associated with this high current drive is the leakage current which rises from 4 nA/µm (low leakage NMOS) to 30 nA/µm (high speed NMOS), as seen in the Id/Vg curve at the X axis location corresponding to Vg= 0 V. From a design view-point, the “option” menu in the MOS generator enables to switch from low leakage to high-speed. In terms of layout, the only difference is the option layer that contains the MOS option information which can be Low leakage (Regular Vt), High Speed (Low VT), or High Voltage.

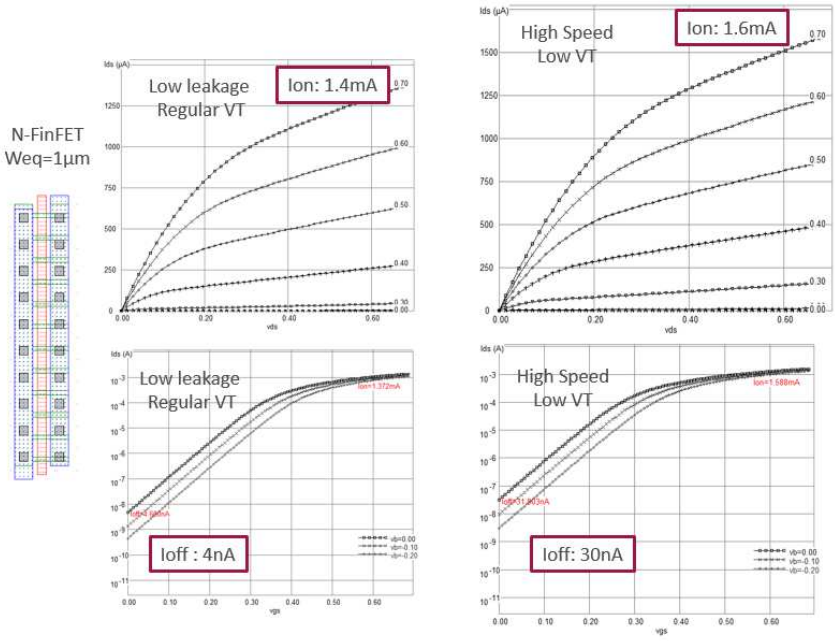


Figure 13: Id/Vd characteristics of the low leakage and high speed n-channel FinFET devices.

P-channel MOS device characteristics

The p-FinFET drive current in 10-nm technology is quite similar to the n-FinFET thanks to the strain engineering for p-channel that nearly compensates the intrinsic mobility degradation of holes (P-channel) vs. electrons (N-channel). The leakage current is around 2 nA/µm for the low-leakage device and nearly 12 nA/µm for the high-speed device (Fig. 15).

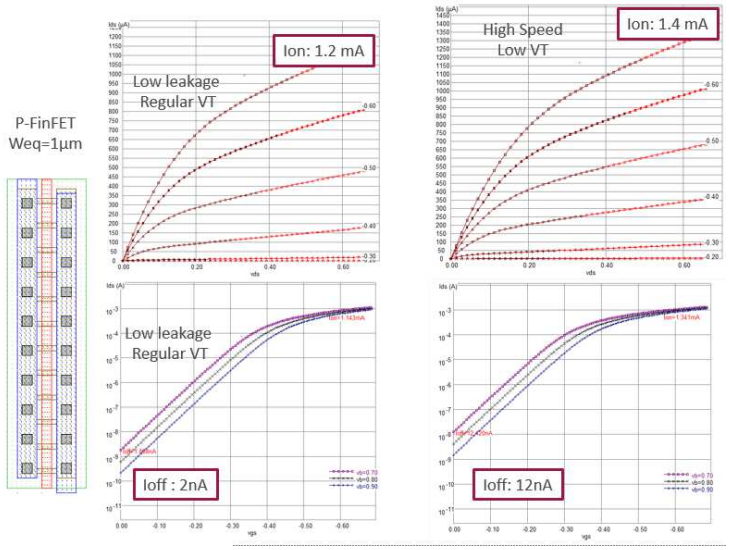


Figure 15: Id/Vg characteristics of the low leakage and high-speed p-FinFET devices

4. MOS Design for Manufacturing

Process Variability

One important challenge in nano-CMOS technology is process variability. The fabrication of millions of MOS devices at nano-scale induces a spreading in switching performances in the same IC.

The effect of process variability on the MOS Ioff/Ion characteristics is plotted using the menu "Ioff vs. Ion" under the "MOS I/V curve" menu (Fig. 16). It can be seen that the MOS devices have a wide variability in performances. The 3 MOS types (low leakage, high speed, high voltage) are situated in well-defined space in the Ioff/Ion domain. The low leakage is in the middle (medium Ion, low Ioff), the high speed on the upper right corner (high Ion, high Ioff), and the high voltage is at the lower left side of the graphics (low *Ion*, very low *Ioff*). Note that the exact locations of the dots will change for each MOS characteristics plotted because it is a random process.

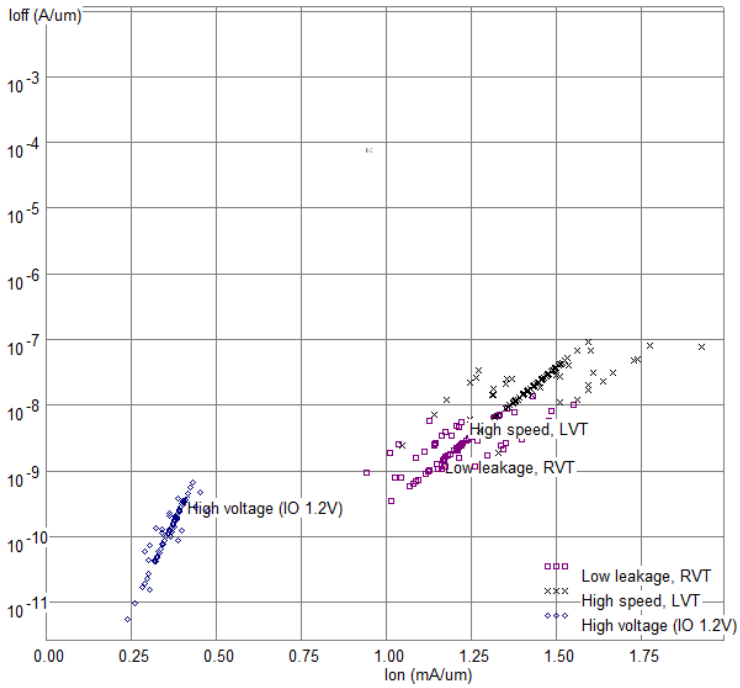


Figure 16: Ioff/Ion calculated on 100 samples of n-FinFET with random distribution of VT and U0, with a Gaussian distribution around the nominal value

5. Interconnects

Metal Layers

The number of metal layers in nano-CMOS technology usually ranges from 8 to 15, with a trade-off between integration and cost. In Microwind, only 8 metal layers are considered, according to table 6:

- M1 & M2 are at 6 λ pitch for local routing
- M3 & M4 are at 8 λ pitch for medium routing
- M5 & M6 are at 32 λ pitch for long routing and local supply
- M7 & M8 are dedicated to power supply and coil inductance

Parameter	Pitch (nm)	Pitch (λ)	Rules	Thickness (nm)	Thickness parameter	Purpose
M1	36	6	R501, R502	35	Thme	Short routing
M2	36	6	R701, R702	35	Thm2	Short routing
M3	48	8	R901, R902	70	Thm3	Medium routing
M4	48	8	RB01, RB02	70	Thm4	Medium routing
M5	96	16	RD01, RD02	120	Thm5	Long routing
M6	96	16	RF01, RF02	120	Thm6	Long routing
M7	276	46	RH01, RH02	400	Thm7	Supply, very long routing
M8	450	75	RJ01, RJ02	640	Thm8	Supply, Coil inductance

Table 6: Key features of interconnects in the 10-nm technology implemented in Microwind

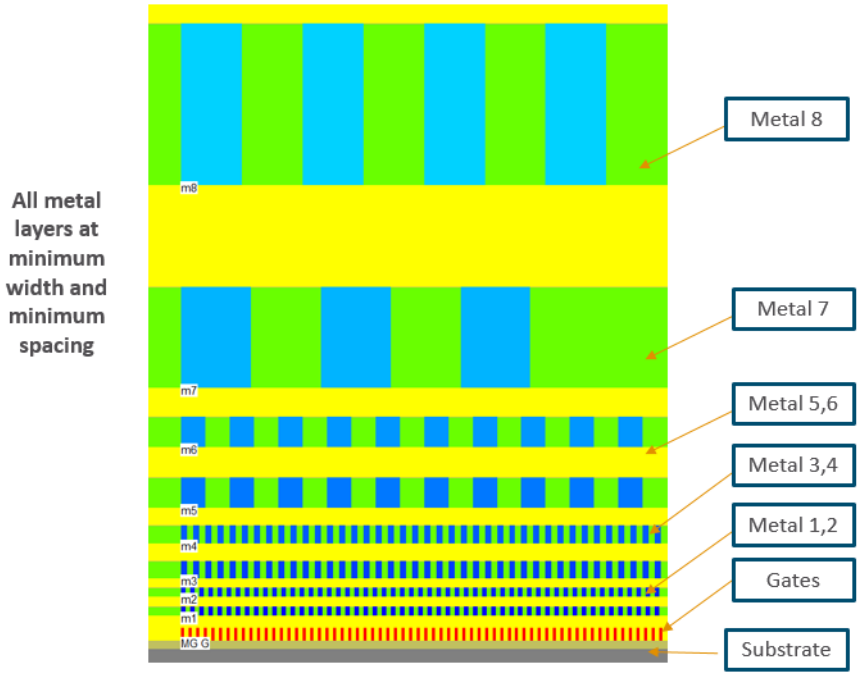


Figure 17: The 8 metal layers proposed in Microwind's implementation of the 10-nm technology

Layers *metal5* and *metal6* are a little thicker and wider, while layers *metal7* and *metal8* are significantly thicker and wider, to drive high currents for power supplies (Fig. 17).

Interconnect Resistance

The resistance and capacitance of interconnects are an important metric for evaluating the RC delay and consequently the switching speed of the signals. The order of magnitude is 50 ohm/µm and 0.35 fF/µm.

Double Patterning for M1-M2 Interconnects

The double patterning is required for metal layers as the pitch between tracks is smaller than 80nm. Half the patterns go on the first patterning and half go on the second patterning, as illustrated in Fig. 18. In order to ensure an easy selection of metal tracks for the first and second patterning, regular structures with straightforward orientation such as M1 east-west, and M2 south-north are requested. The other solution is to relax the pitch constraints for an improved manufacturability, at the cost of an extended silicon area. M3-M8 with pitch of 80-nm and higher are still fabricated using simple patterning.

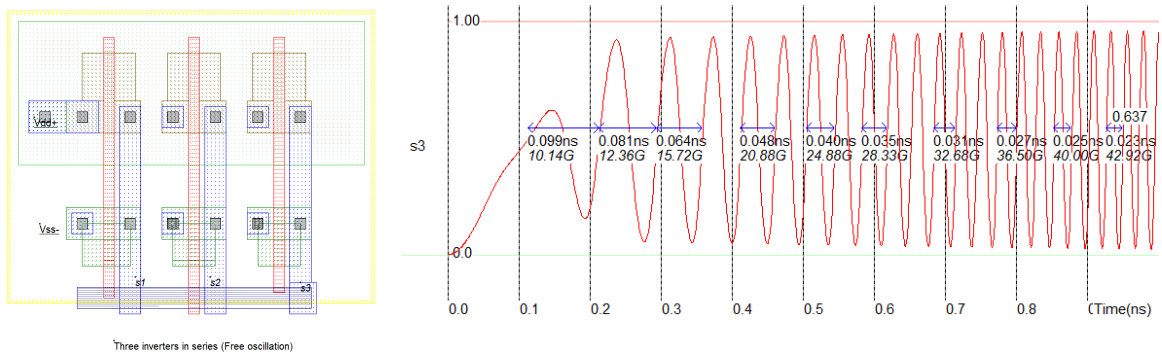
Pitch (nm)	λ	>120	110	100	90	80	70	60	50	40	30	20
Patterning		Single	Single	Single	Single							
						Double	Double	Double	Double			
										Quad	Quad	Quad
45-nm	20	All	SINGLE				DOUBLE			QUADRUPLE		
32-nm	18	M3-M8	M1-M2	Gate								
20-nm	12	M7-8		M5-M6	M3-M4	M1-M2	Gate					
14-nm	8	M7-8				M5-M6	M3-M4	M1-M2	Gate			
10-nm	6	M7-8					M5-M6	M3-M4	M1-M2	Gate		
7-nm	4	M7-8						M5-M6	M3-M4	M1-M2	Gate	

Figure 18: Single, double and quadruple patterning as a function of interconnect pitch [Brain2017]

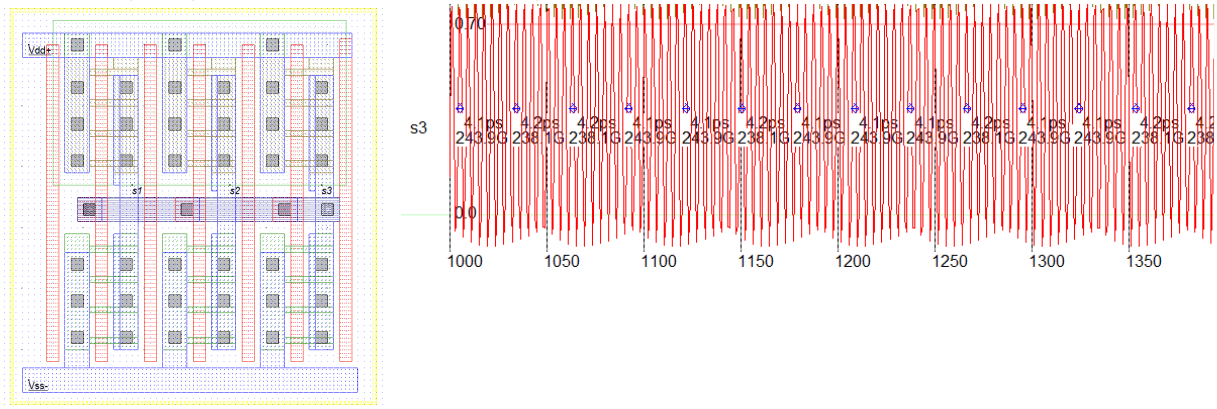
6. Ring Inverter Simulation

Performances

An improvement of switching performances as high as x 5 is obtained between 45nm and 14nm designs, although VDD is reduced from 1.1V to 0.7V. Microwind operates with lambda-based designs which are independent of the technology, but MosFET and FinFET designs are not compatible. However, comparison remains possible at similar drive currents, circuits and design styles. As seen in Fig. 19, a 3-inverter ring oscillator (RO) features a natural 43 GHz oscillation in 45-nm, which rises to nearly 250 GHz with 10-nm technology.



45nm RO3, FO1, MosFET VDD = 1.0V, Oscillation around 45 GHz



10-nm RO3, FO1, FinFET VDD = 0.7V, Oscillation around 240 GHz

Figure 19: Considerable speed improvement is observed between 45-nm 3-stage ring oscillator based on MosFET and 10-nm 3-stage ring oscillator based on FinFET

Minimum VDD

As illustrated in Fig. 20, the voltage scaling depends on the operating scenario, and may range from very low supply voltage to nominal voltage supply or even boost voltage supply (+10% of nominal supply).

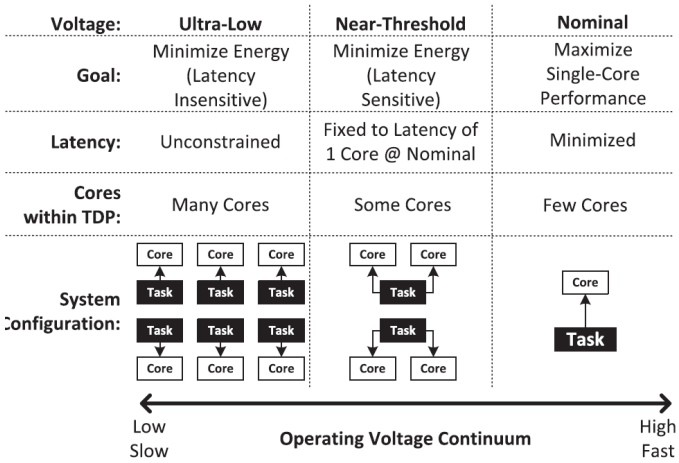


Figure 20: the voltage scaling depends on the operating scenario [Pinckney2017]

We extract the minimum VDD value for which the ring oscillator is still operating. The VDD value can be changed through the command **Simulate → Simulation Parameters.** We can also use the command Analysis → **Parametric Analysis,** click on the S3 node, select VDD voltage from 0.4 to 0.8, and monitor the frequency. It can be seen that the ring oscillator do not operate below 0.45V (Fig. 21).

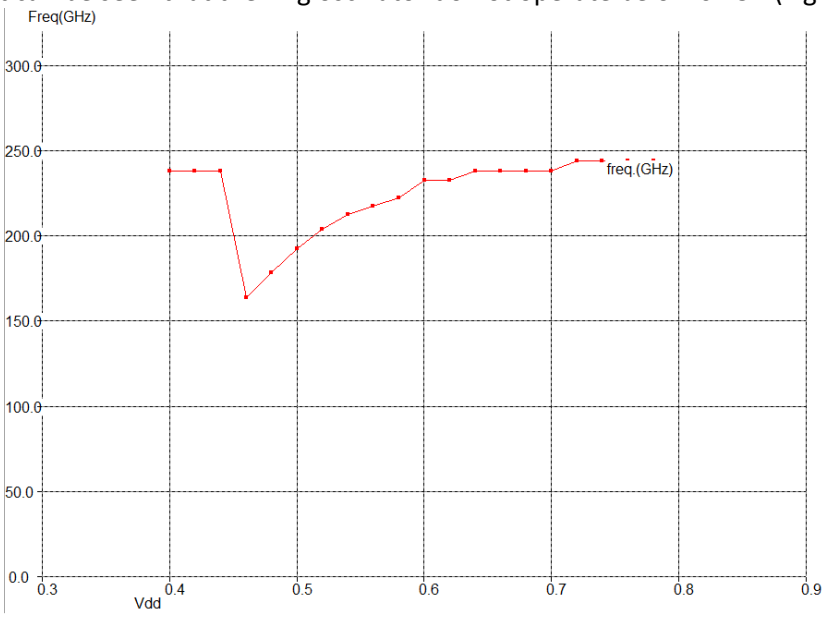


Figure 21: Modify VDD to extract the minimum operating voltage of the ring oscillator.

Simulation of Process Variations (PVT)

Considerable differences may be observed in terms of performances, depending on the process, voltage and temperature conditions. The usual temperature range is [-50°C..+125°C], the voltage variation VDD+/- 10%, and the process may also vary +/-15% for some key parameters such as the threshold voltage and mobility. Microwind gives access to "Process-Voltage-Temperature" (PVT) simulation through the command **Simulate → Simulation Parameters → Process Variations**. Direct access from the simulation waveform window is also possible using the button **"Process Variations".** The most usual simulation consists of simulating extreme situations (Min and Max), as compared to typical conditions (Table 7).

- In *Min* situation, VT is high and the mobility U0 is low. The supply is minimum and the temperature is maximum. The ring oscillating is around 100 GHz.
- In *Max* situation, VT is low, mobility U0 is high and the channel is short (LINT<0). The supply is maximum and the temperature is minimum. The ring oscillation is around 250 GHz.

Parameter class	Parameter	Symbol (BSIM4)	Unit	Min (10-nm)	Typ (10-nm)	Max (10-nm)
Process	Threshold Voltage	VT	V	0.33	0.28	0.24
	Mobility	U0	m2/V.s	0.030	0.035	0.040
Voltage	Supply	VDD	V	0.60	0.70	0.81
Temperature	Temperature	TEMP	°C	125	25	-50

Oscillating frequency	150	240	290

Table 7: Variation of process parameters and effects on the oscillating frequency

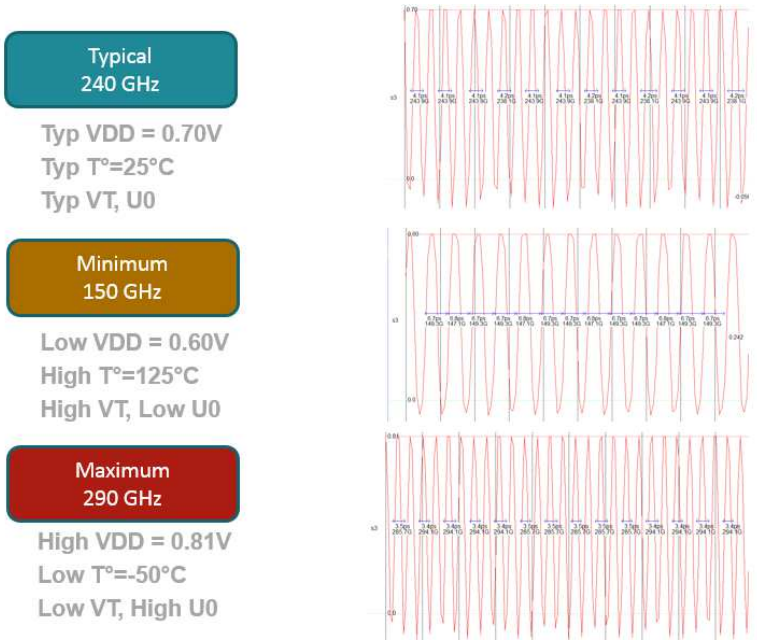


Figure 22: Typ/Min/Max simulation using PVT analysis

7. 6-transistor static RAM

One of the most representative designs for comparing technology nodes is the static RAM cell designed using 6 transistors (6T-SRAM). The size reduction from 45 to 10-nm process is illustrated in Fig. 23 with Intel's implementation of the 6T-SRAM, with a surface divided nearly by 10 (0.3 µm2 down to 0.03 µm2). High performance SRAM use 2 fins for internal inverters while high density SRAM use 1 fin. Pass transistors use more fins than inverters.

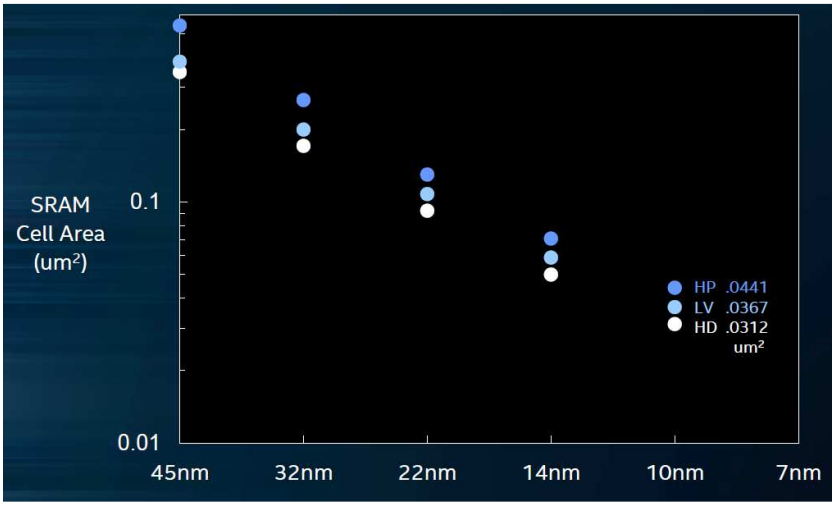


Figure 23: Reduction of the 6T-SRAM memory from 45-nm to 10-nm process of Intel, reaching 0.03µm2 for the most compact design [Miustry2017]

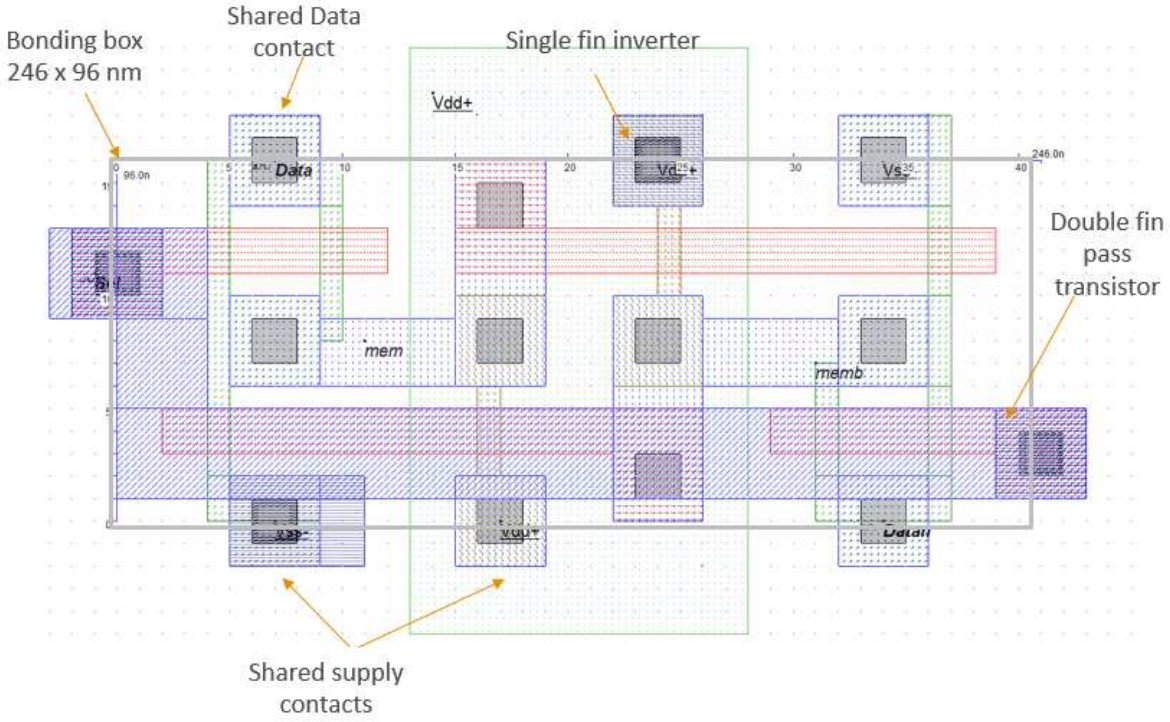


Figure 24: 6T-SRAM implementation in FinFET (SRAM-6T-10nm.MSK)

In our implementation in Microwind (see Fig. 30), the layout size is 246 x 96 nm, with a surface area of 0.024 µm^2. The layout obeys the basic design rules. Most contacts are shared with neighboring cells: the VSS, VDD contacts, the Select and Data lines. It is usual to find more aggressive layout design rules in RAM cell designs, in order to further decrease the cell area.

Compare technologies

A quick access to technology is proposed in Simulation Parameters. MosFET technologies range from 0.18µm to 20nm, FinFET technologies (red) start from 14nm. MosFET and FinFET designs are not compatible.

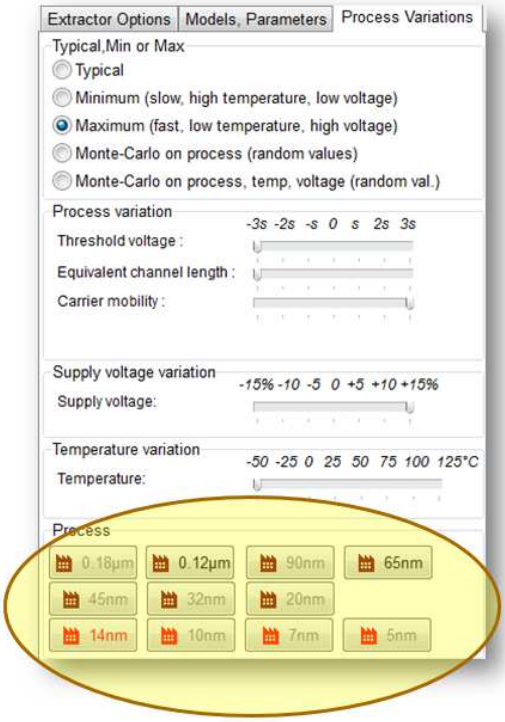


Figure 25: Quick access to MosFET and FinFET technologies

Convert MosFET design to FinFET design

In Microwind 3.8, the command Edit > Convert into FinFET creates fins from N-diffusion. Only works for vertical gates. The command generates fins according to the fin pitch as described in the design rule file (r308). An example of fin generation from a MosFET layout is reported in Fig. 26.

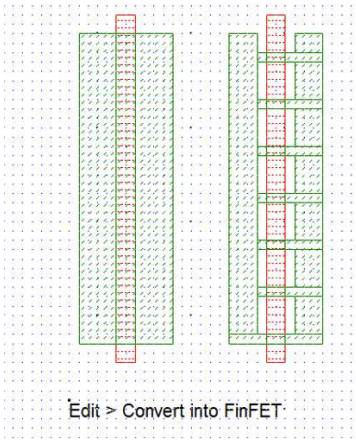


Figure 26: Convert MosFET design into FinFET. Only vertical gates are considered.

8. Conclusions

This application note has illustrated the trends in CMOS technology and introduced the 10-nm technology generation, based on technology information available from manufacturers. The key features of the 10-nm CMOS technology have been illustrated, including the FinFET, design for

manufacturing and double patterning. A 3-stage ring, FinFETs wih 1-µm equivalent width as well as interconnects with 1-µm length have been used for comparison purpose.

Acknowledgements

The adaptation of Microwind to 10-nm FinFET technology and the development of an e-learning course on nano-CMOS cell design have been made possible thanks to the financial support of the ERASMUS+ program Knowledge Alliance "Micro-Electronics Cloud Alliance" 562206-EPP-1-2015-1-BG-EPPKA2-KA.

References

Brain R. (2017). 14 nm technology leadership. Technology and Manufacturing Day, Intel. 2017.

Mistry, K. (2017). 10 nm technology leadership, Technology and Manufacturing Day, Intel. 2017.

Pinckney, N., (2017). Impact of FinFET on Near-Threshold Voltage Scalability. IEEE Design & Test, 34(2), 31-38.

Sicard, E. (2017). Introducing 14-nm FinFET technology in Microwind. Application note on-line. www.microwind.org

Xie, Q. (2015). Performance Comparisons between 7-nm FinFET and Conventional Bulk CMOS Standard Cell Libraries. IEEE Transactions on Circuits and Systems II: Express Briefs, 62(8), 761-765.