Hardware Architectures for HECC

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Summary	Context & Motivations	HECC Operations	Efficient Multiplier 00000	Architectures and Tools	Conclusion 000
Sumn	nary				

- Context & Motivations
- 2 HECC Operations
- 3 Efficient Multiplier
- Architectures and Tools for HECC
- 5 Conclusion

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Public-Key Cryptography (PKC)

- Provides cryptographic primitives such as digital signature, key exchange and specific encryption schemes
- First PKC standard: RSA
 - \geq 2000-bit keys recommended today
 - Too costly for embedded applications
- Elliptic Curve Cryptography (ECC):
 - Better performances and lower cost than RSA
 - Allows more advanced schemes
- Hyper-Elliptic Curve Cryptography (HECC):
 - Evolution of ECC focusing on larger sets of curves
 - Supposed to have a smaller cost than ECC

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Operations Hierarchy in (H)ECC



Main metric: numbers of M and S in $\mathbb{F}_\mathcal{P}$

- $\bullet\,$ ADD and DBL built using $\mathbb{F}_{\mathcal{P}}$ operations
- Modular arithmetic in $\mathbb{F}_{\mathcal{P}}$:
 - $100\cdots 200$ bits elements for HECC
 - Operations involve modular reduction
 - Choice for \mathcal{P} :
 - Generic \mathcal{P} : more flexible but slower
 - Specific *P* (*e.g.* pseudo-Mersenne): faster but more specific
- $\bullet\,$ Modular multiplication (M) and square (S):
 - Most common and costly operations
 - Efficient dedicated units

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ECC, HECC, Kummer-HECC

	$\mathbb{F}_{\mathcal{P}}$ elements size	ADD	DBL	source
ECC	$\ell_{\rm ECC}$	12M + 2S	7M + 3S	[Bernstein and Lange]
HECC	$\ell_{\rm HECC}\approx \frac{1}{2}\ell_{\rm ECC}$	40M + 4S	38M + 6S	[Lange, 2005]
Kummer	$\ell_{ m HECC}$	19M -	+ 12S	[Renes et al., 2016]

• ECC:

- Size of $\mathbb{F}_{\mathcal{P}}$ elements $2\times$ larger
- Simpler ADD and DBL operations
- HECC:
 - Smaller $\mathbb{F}_{\mathcal{P}}$
 - More operations in $\mathbb{F}_\mathcal{P}$ for ADD / DBL
- Kummer-HECC is more efficient than ECC [Renes et al., 2016]:
 - ARM Cortex M0: up to 75% clock cycles reduction for signatures
 - AVR AT-mega: up to 32% cycles reduction for Diffie-Hellman

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Curve-Level Operations in Kummer

- No ADD operation but still DBL
- Differential addition: $xADD(\pm P, \pm Q, \pm (P Q)) \rightarrow \pm (P + Q)$
- xADD and DBL can be combined: xDBLADD($\pm P, \pm Q, \pm (P - Q)$) $\rightarrow (\pm [2]P, \pm (P + Q))$

For details see [Renes et al., 2016], [Gaudry, 2007] and [Bos et al., 2016]

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xDBLADD $\mathbb{F}_{\mathcal{P}}$ Operations



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Scalar Multiplication

Montgomery ladder based crypto_scalarmult [Renes et al., 2016]:

Require: *m*-bit scalar $k = \sum_{i=0}^{m-1} 2^i k_i$, point P_b , $cst \in \mathbb{F}_{\mathcal{D}}^4$ **Ensure:** $V_1 = [k]P_b, V_2 = [k+1]P_b$ $V_1 \leftarrow cst$ $V_2 \leftarrow P_h$ for i = m - 1 downto 0 do $(V_1, V_2) \leftarrow \text{CSWAP}(k_i, (V_1, V_2))$ $(V_1, V_2) \leftarrow \text{xDBLADD}(V_1, V_2, P_b)$ $(V_1, V_2) \leftarrow \text{CSWAP}(k_i, (V_1, V_2))$ end for return (V_1, V_2) CSWAP $(k_i, (X, Y))$ returns (X, Y) if $k_i = 0$, else (Y, X)

- Constant time, uniform operations (independent from key bits)
- \bullet Some parallelism between xDBLADD internal $\mathbb{F}_{\mathcal{P}}$ operations
- CSWAP: very simple but involves secret bits (to be protected)

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Montgomery Modular Multiplication (MMM)

$$egin{aligned} R &= A imes B \ q &= (R imes (-\mathcal{P}^{-1})) \mod (2^n) \ q \mathcal{P} &= q imes \mathcal{P} \end{aligned}$$

 $n \times n \rightarrow 2n$ bits $n \times n \rightarrow n$ bits $n \times n \rightarrow 2n$ bits

Architectures and Tools



Context & Motivations

• Objective: $A \times B \mod \mathcal{P}$

Efficient Multiplier

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- Proposed in [Montgomery, 1985]
- Variants are actual state-of-the-art for $\mathbb{F}_{\mathcal{P}}$ multiplication (with generic \mathcal{P})
- Final reduction step discards *n* LSBs



Modular Multiplication: Dependencies Problem

- In practice, MMM is interleaved
 - Operands are split into s words of w bits such that $n = s \times w$
 - Iterations over partial products and reductions on words
 - Coarsely Integrated Operand Scanning (CIOS) from [Koç et al., 1996]
- Impact on hardware implementation
 - Dependencies \rightarrow latencies between internal iterations
 - Hardware pipeline in DSP slices cannot be filled efficiently
- Proposed solution: Hyper-Threaded Modular Multiplier (HTMM)
 - Based on simple CIOS algorithm
 - Use idle stages to compute other independent MMMs in parallel



HTMM Internal Architecture

- HTMM architecture: 3 hardware stages
 - Stages are fully pipelined (several clock cycles per stage)
 - 3 to 4 DSP slices in each stage





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HTMM Implementations

- Xilinx FPGAs
 - Virtex 4 XC4VLX100 (V4)
 - Virtex 5 XC5VLX110T (V5)
 - Spartan 6 XC6SLX75 (S6)
- Comparison with fastest MMM implementation in literature
 - Design presented in [Ma et al., 2013]
 - Implemented on the same FPGAs for fair comparison
- 2 versions of HTMM:
 - HTMM_DRAM : operands stored in FPGA slices (LUTs)
 - HTMM_BRAM : operands stored in FPGA BRAMs
- Parameters for HTMM:
 - $\mathcal{P}
 ightarrow$ 128 bits
 - w = 34 bits, s = 4
 - Operands size $n = s \times w = 134$ bits

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Architectures and Tools

HTMM Implementations Results

Results for 3 independent multiplications:

Version	FPGA	DSP	BRAM	FF	LUT	Slices	Freq.	Nb.	Time
			18K/9K				(MHz)	cycles	(ns)
	V4	21	6/0	1311	1201	879	252		258
[Ma et al., 2013]	V5	21	6/0	1310	1027	406	296	65	220
	S6	21	0/6	1280	1600	540	210		309
	V4	11	0/0	1638	1128	1346	330		239
HTMM_DRAM	V5	11	0/0	1616	652	517	400	79	198
	S6	11	0/0	1631	1344	483	302		261
HTMM_BRAM	V4	11	2/0	615	364	449	328		241
	V5	11	2/0	593	371	249	357	79	221
	S6	11	0/2	587	359	180	304		260

S6: -47% DSPs, -66% BRAMs, -66% slices, -15% duration

For only 1 single M, HTMM is less efficient (69 cycles against 25)

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HECC architectures require different types of units:

- $\mathbb{F}_{\mathcal{P}}$ arithmetic units: add/sub, mul, sqr, inv, \ldots
- Memories, (secure) registers, ...
- Interconnect, global input/output, ...
- Dedicated (secure) control

Problems

- Coding a complete accelerator fully in HDL is costly
- Large design space for various architectures types and parameters (nb. units, algorithms, internal communications and control)
- Need for evaluation of various architectures and parameters
- Need for numerical validation and debug

Proposed Design Framework

- Hierarchical description and simulation for HECC architectures at CCABA level (Critical-Cycle Accurate, Bit Accurate)
 - Units inputs/outputs are bit accurate
 - Units inputs/outputs and external control are critical cycle accurate
- Description of various architectures at high-level
 - Composition of units for differents parameters and optimizations
 - Scheduling tool for control and communications (work in progress)
- Units described, optimized and validated in HDL
 - Perfectly known behavior \rightarrow no need for cycle accurate simulation
 - Area, latency, ... come from actual FPGA implementation

• Dedicated simulator in Python

- Fast development and numerical validation
- Sage (http://www.sagemath.org/) interface for HECC support

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Typical Architecture Model



Parameters specified at design time:

- Width w and nb. words s for internal communications $(s \times w = n)$
- Types and number of units



Configuration for Implementations

- 128 bits HECC solutions
- $\mathbb{F}_{\mathcal{P}}$ adder-subtractor (AddSub):
 - 4 cycles latency pipeline
 - $8 \cdots 11$ cycles delay depending on w
- $\mathbb{F}_{\mathcal{P}}$ multiplier (HTMM):
 - Hyper-threaded multiplier for 3 sets of operands computed in parallel
 - 5 cycles latency for loading and reading
 - $68 \cdots 71$ cycles delay depending on w
- CSWAP unit:
 - Secure management of key bits
 - $2 \cdots 4$ cycles delay depending on w

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Results for Basic Architecture (1 Add/Sub, 1 HTMM)

Version $s \times w$	Clock cycles	Units	DSP	BRAM	FF	LUT	Slices	RAM #lines
		НТММ	11	2	587	359	180	12
		AddSub	0	0	366	226	80	-
4×34	207,383	DATA_MEM	0	1	0	0	0	112
		PRGM_MEM	0	1	0	0	0	208
		CSWAP	0	0	536	290	103	-
	185,615	НТММ	11	2	970	633	315	12
		AddSub	0	0	713	382	148	-
2×68		DATA_MEM	0	2	0	0	0	56
		PRGM_MEM	0	1	0	0	0	234
		CSWAP	0	0	553	297	122	-
		HTMM	11	2	1066	623	309	12
1×136		AddSub	0	0	784	464	212	-
	183,051	DATA_MEM	0	4	0	0	0	26
		PRGM_MEM	0	1	0	0	0	250
		CSWAP	0	0	685	431	155	-

s: number of words, w: size of words

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Increasing the Number of Arithmetic Units

Version $s \times w$	Clock cycles	Units	DSP	BRAM	FF	LUT	Slices	RAM #lines
		HTMM x 2	22	4	1174	718	360	12
		ADDSUB x 2	0	0	732	452	160	-
4x34	203,543	DATA_MEM	0	1	0	0	0	108
		PRGM_MEM	0	1	0	0	0	213
		CSWAP	0	0	536	290	103	-
	125,455	HTMM x 2	22	4	1940	1266	630	12
		ADDSUB x 2	0	0	1426	764	296	-
2×68		DATA_MEM	0	4	0	0	0	50
		PRGM_MEM	0	1	0	0	0	211
		CSWAP	0	0	553	297	122	-
	115,211	HTMM x 2	22	4	2132	1246	618	12
1×136		ADDSUB x 2	0	0	1568	928	424	-
		DATA_MEM	0	4	0	0	0	25
		PRGM_MEM	0	1	0	0	0	235
		CSWAP	0	0	685	431	155	-

s: number of words, w: size of words

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256b ECC vs 128b HECC (similar theoretical security)

FPGA	Version	DSP	BRAM	Slices	Freq.	Nb.	Time
			18K		(MHz)	cycles	(ms)
	ECC	37	11	4655	250	109,297	0.44
V4	HECC_1u	11	7	1413	330	183,051	0.55
	HECC_2u	22	9	2356	330	115,211	0.35
	ECC	37	10	1725	291	109,297	0.38
V5	HECC_1u	11	7	873	360	183,051	0.51
	HECC_2u	22	9	1542	360	115,211	0.32

Gain 1u on V5: -70% DSPs, -30% BRAMs, -49% slices, +30% duration Gain 2u on V5: -40% DSPs, -10% BRAMs, -10% slices, -15% duration

ECC results from [Ma et al., 2013]

Conclusions and Perspectives

- Kummer based HECC is an efficient alternative to ECC
 - More complex formulas but larger internal parallelism
 - Large exploration space for architectures and arithmetic
- We designed a CCABA modeling and simulator
 - High-level hierarchical description of architectures
 - Units described in HDL, only critical cycles are used
 - Fast validation/debug and evaluation of solutions in exploration space
- Future works
 - Study advanced scheduling algorithms
 - Automating generation of HDL code from high-level description
 - Explore new architectural solutions

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Thank you for your attention



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Elliptic and Hyper-Elliptic Curves for Crypto

Elliptic Curves

- Equation (Weierstrass) $E/\mathbb{K}: y^2 + a_1xy + a_3y = x^3 + a_2x^2 + a_4x + a_6$
- Defined over finite fields \mathbb{K} : \mathbb{F}_{2^m} , prime finite field $\mathbb{F}_{\mathcal{P}}$ or GF(p)
- $\mathbb{F}_{\mathcal{P}}$ elements for coefficients and coordinates: 200 \cdots 400 bits





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Hyper-Elliptic Curves

- More complex!
- Equation $H/\mathbb{K}: y^2 + h(x)y = f(x)$, deg(h) < g and deg(f) = 2g + 1
- g: genus of the curve, $g \leq 2$ in practice for reliable HECC
- $\mathbb{F}_{\mathcal{P}}$ elements for coefficients and coordinates: $100\cdots 200$ bits



Elliptic and Hyper-Elliptic Curves for Crypto

• Elliptic Curves

- Equation (Weierstrass) $E/\mathbb{K}: y^2 + a_1xy + a_3y = x^3 + a_2x^2 + a_4x + a_6$
- Defined over finite fields \mathbb{K} : \mathbb{F}_{2^m} , prime finite field $\mathbb{F}_{\mathcal{P}}$ or GF(p)
- $\mathbb{F}_{\mathcal{P}}$ elements for coefficients and coordinates: $200\cdots 400$ bits

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- More complex!
- Equation $H/\mathbb{K}: y^2 + h(x)y = f(x)$, deg(h) < g and deg(f) = 2g + 1
- g: genus of the curve, $g \leq 2$ in practice for reliable HECC
- $\mathbb{F}_{\mathcal{P}}$ elements for coefficients and coordinates: $100\cdots 200$ bits
- Kummer surface
 - Not an additive group: no addition law
 - Can be used in HECC using some (magic) trick
 - Reduced complexity for curve operations

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HTMM Detailed Architecture

