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Introducing 14-nm FinFET technology in Microwind

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This paper describes the implementation of a high performance FinFET-based 14-nm CMOS Technology in Microwind. New concepts related to the design of FinFET and design for manufacturing are also described. The performances of a ring oscillator layout and a 6-transistor RAM memory layout are also analyzed.

1. Technology Roadmap

Several companies and research centers have released details on the 14-nm CMOS technology, as a major step for improved integration and performances, with the target of 7-nm process by 2020. We recall in table 1 the main innovations over the past recent years.

Technology node	Year of introduction	Key Innovations	Application note
180nm	2000	Cu interconnect, MOS options, 6 metal layers	
130nm	2002	Low-k dielectric, 8 metal layers	
90nm	2003	SOI substrate	[Sicard2005]
65nm	2004	Strain silicon	[Sicard2006]
45nm	2008	2nd generation strain, 10 metal layers	[Sicard2008]
32/28nm	2010	High-K metal gate	[Sicard2010]
20nm	2013	Replacement metal gate, Double patterning, 12 metal layers	[Sicard2014]
14nm	2015	FinFET	This application note

Table 1: Most significant technology nodes over the past 15 years

Improved performances

The power, performance and area gains are an important metric for justifying a shift from older technology nodes to new ones. As compared to 20-nm technology node [Sicard2014], the 14-nm technology offers:

- 30 % less power consumption. This is a key feature for mobile industry for which the battery life is the top one problem.
- 30 % increase in switching performance. This is equally important in server applications and smartphones, which use faster processors and higher resolution screens.

- 2 times higher density. This is a key advantage to produce the lightest and thinnest possible smartphones.

A comparison between 45nm, 32, 22, 14 and 10nm technologies in terms of density is proposed by [Brain2017] are reported in Fig.1. The IC surface is shrunk by a factor of 5 between 45-nm and 14-nm nodes.

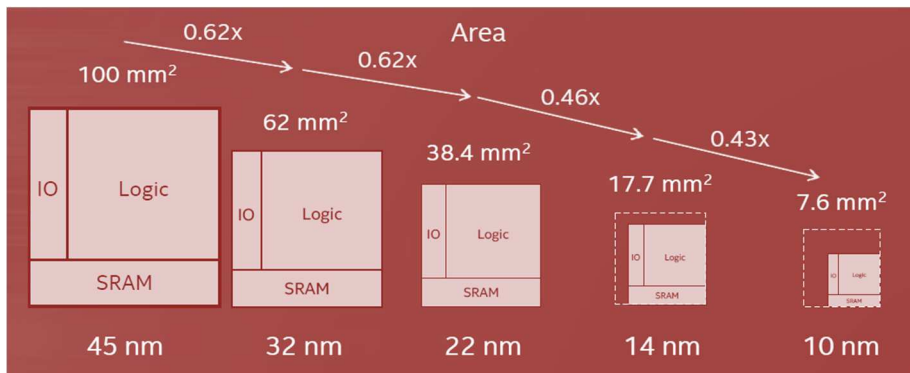


Figure 1: The evolution of silicon area with the technology nodes as presented by Intel [Brain2017]

The giant cost of fab and IC design in 14-nm

The consequences of the fab and chip design cost explosion is the drastic decrease of foundries. While more than 20 foundries existed for 130nm technology, only four major companies are providing the 14-nm process (Table 2).

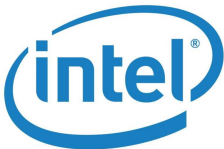



Company	Logo	Technology name
Intel		14nm, 14nm+, 14nm++
Samsung/GlobalFoundries		14LPE (Early edition) 14LPP (Performance boosted edition)
TSMC		16nm FinFET Plus (16FF+) process
UMC		14FF+, 144FFC

Table 2: 4 major players in the 14-nm chip manufacturing

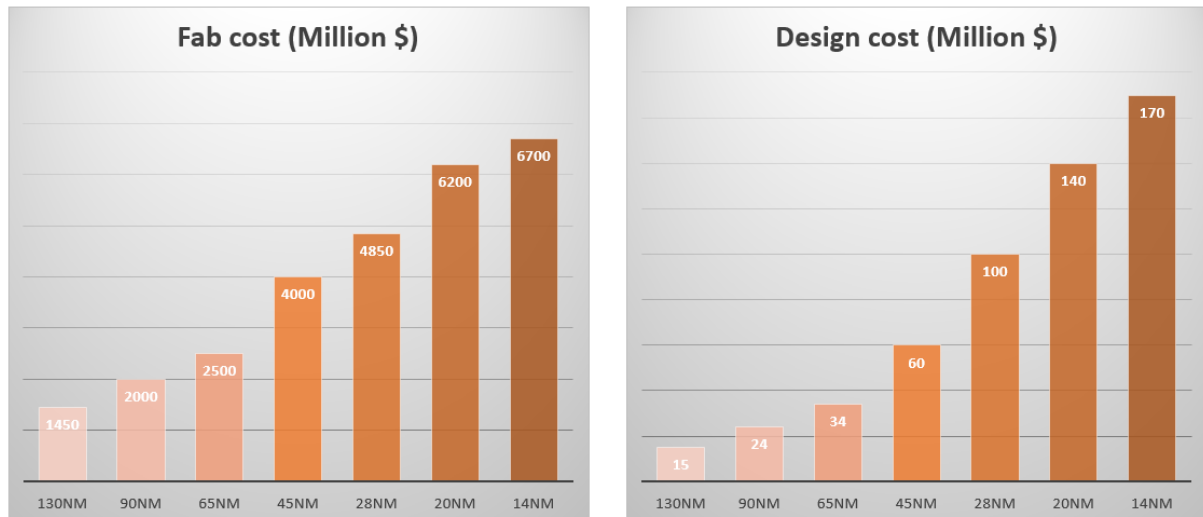


Figure 2: The extraordinary increase of the fab cost: more than 6 billion \$ for a 14-nm process, and associated chip design cost: 176 M\$, more than 10 times the cost of a 130nm IC design.



14-nm Exynos by Samsung™



14-nm Xeon by Intel™



14-nm Snapdragon by Qualcomm™



14-nm Zen Processor by AMD™

Figure 3: Examples of multi-giga-transistor processors used in mobiles, laptops and servers from various companies.

Within a same technology node, improvements are made over the years, such as Intel who improved on their original process "14nm" with the "14nm+" offering 12% higher drive current, followed 1 year later by "14nm++" process which allows for +25% higher drive current [Brain2017].

Some examples of processors used in mobile phones, laptops and servers are reported in Fig. 3, with complexity approaching 10 Billion devices. A continuous increase in switching performance has been made possible thanks to several innovations, as shown in Figure 4. Starting 14-nm, the MosFET is replaced by the FinFET, for improved current capabilities.

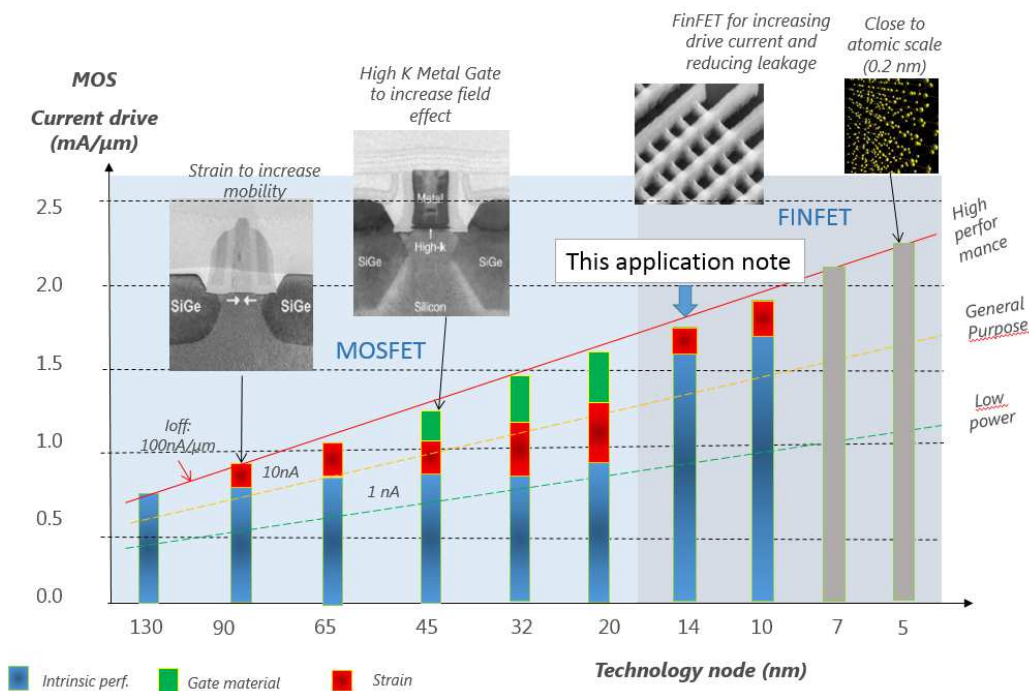


Figure 4: most significant technology improvements over the past 15 years

14-nm Process variants

Within the same “14-nm” label, we may observe a wide variety of performances, depending whether the IC fabrication process is targeted to “high performance” (HP) devices (speed whatever the power consumption), “general purpose” (GP) or “Low Power” (LP) (lower speed but power-efficient), as summarized in Table 3. Significant differences may be observed in terms of I_{on} and I_{off} currents, as illustrated in Figure 4. We implement in Microwind the general purpose 14-nm process.

14-nm Technology variant	Pros	Cons	Target application	Typical I_{on}/I_{off}
General purpose	Medium speed	Medium consumption	Laptops	1.3 mA/μm 10 nA/μm
High performance	Fast speed	High consumption	Servers	1.7 mA/μm 100nA/μm
Low power	Low speed	Low consumption	Smartphones	1.0 mA/μm 1 nA/μm

Table 3: technology variants within the same node

Power supply operation

The supply voltage, both internal to the cores and the external I/O supply have been continuously decreased due to the thinning of the gate oxide and faster switching rates thanks to reduced voltage swings. The 14-nm technology operates around 0.8V, while I/Os are supplied at 1.2, 1.5 or 1.8 V (Fig. 5).

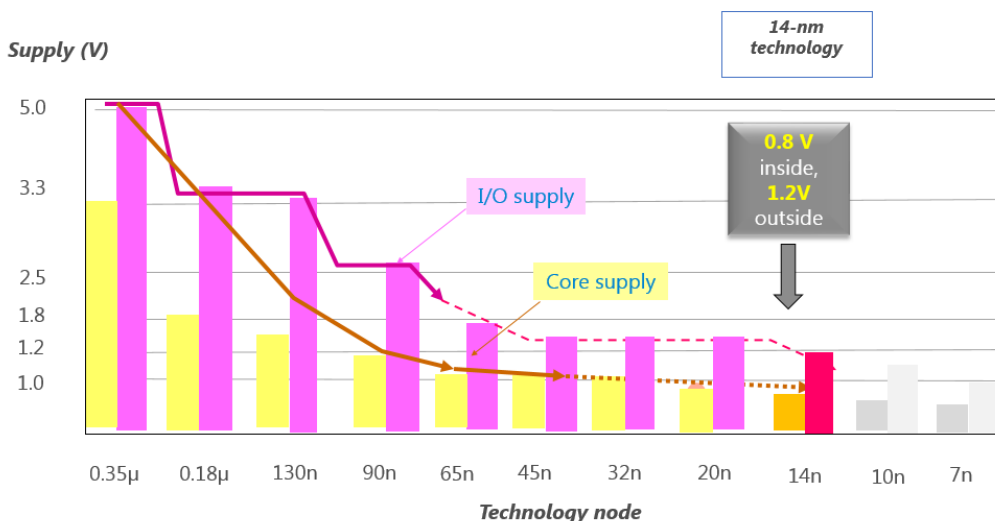


Figure 5: The core supply voltage in 14-nm technology is 0.8 V, with typical IO voltage of 1.2 V

2. Key features of the 14-nm technology

Introducing the FinFET

The FinFET device has a different layout style than the MOS device. Instead of a continuous channel, the FinFET uses fins (Figure 6), which provide the same current at a smaller size. FinFET also provides a lower leakage current (I_{off}) at the same (I_{on}) [Fischer2017].

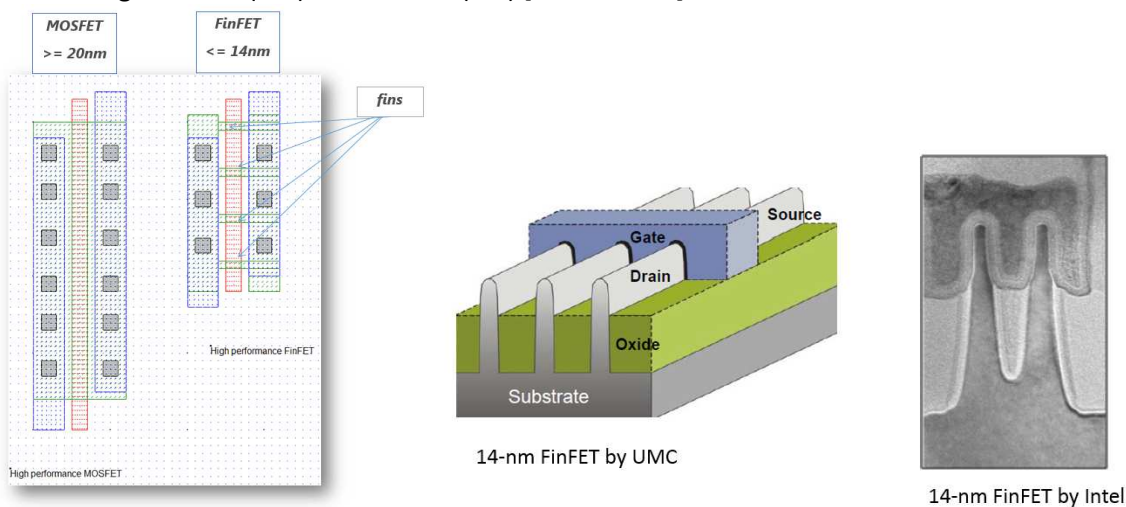


Figure 6: Introducing the FinFET in 14-nm technology: the same current switching capabilities in a smaller area. Fins cross the gate.

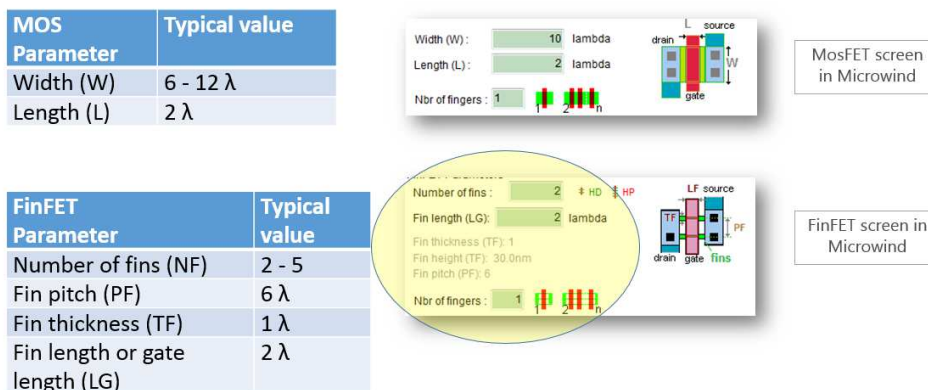


Figure 7: The introduction of the FinFET in Microwind, and comparison with traditional MosFET

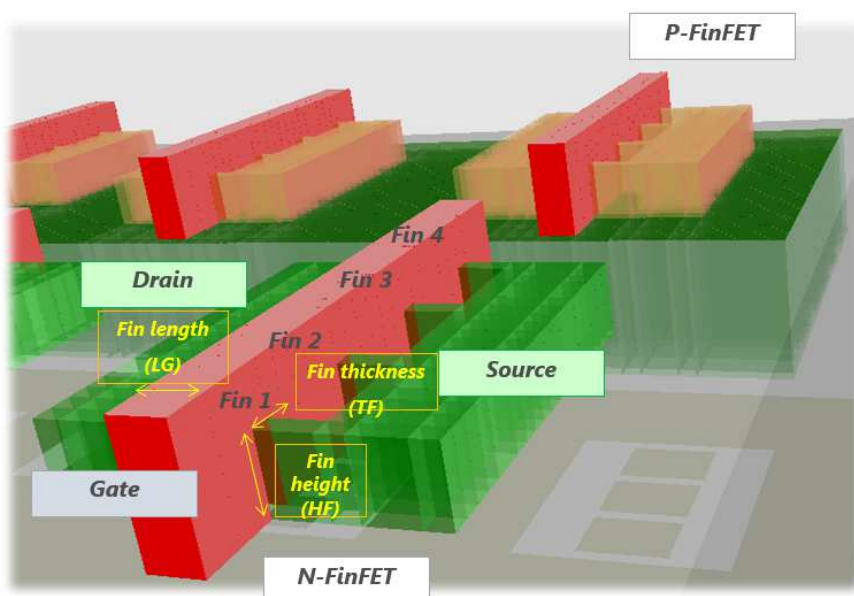


Figure 8: 3D view of the FinFET and illustrations of the Fin height (HF), Fin Thickness (TF) and Fin Length (LG).

Built on more than 15 years of FinFET research & development and solid foundation of high-K metal gate production experience, the 14-nm FinFET device reuses an important part of process elements from the previous 28-nm and 20-nm nodes, so that planar designs may be partially reused in 14-nm FinFET technology. However, the Fin design is a totally new feature which contrasts with the traditional MOS design. This leads to new screens and new acronyms such as “Fin Pitch”, “Fin thickness”, etc, as shown in Figures 7 and 8.

Lambda

In Microwind, we use an integer unit for drawing, which is fixed to 8 nm for 14-nm CMOS process (Table 4).

- The drawn gate length is 2 λ that is 16 nm.
- The fin width is 1 λ that is 8 nm.
- The lower metal pitch is 48-nm.

Microwind parameter	Unit	Code	Name in rule file	14-nm process
Lambda	nm	λ	lambda	8
Core supply	V	VDD	Vdd	0.8
Fin Width	λ	WF	R301	1
Fin pitch	λ	FP	R308	6
Fin Height	nm	HF	thdn	40
Gate height	nm	GH	thpoly	60
Gate length	λ	GL	R302	2
Gate pitch	λ	GP		6
Spacer width	nm	SW		10
Contact size	λ	CS	R401	2
EOT	Nm	EOT	b4toxe	0.9
M1 pitch	λ		R501+R502	6

Table 4: key parameters of the 14-nm processes used to configure Microwind rule file Cmos14n.RUL

Core MOS devices

Table 4 gives an overview of the key parameters for the 14-nm technological node concerning the internal MOS devices and layers. High performance NMOS/PMOS drive currents of 1.3/1.2 mA/ μm , respectively, have been achieved at 0.7 V and 100 nA/ μm off-state leakage in early versions of the Intel’s 14-nm technology [Liu2015]. Drive currents near 2 mA/ μm have been announced by [Fischer2017] for the 2nd iteration of process improvement called 14++nm (Figure 9). Such performances are in phase advance with the roadmap of Figure 3.

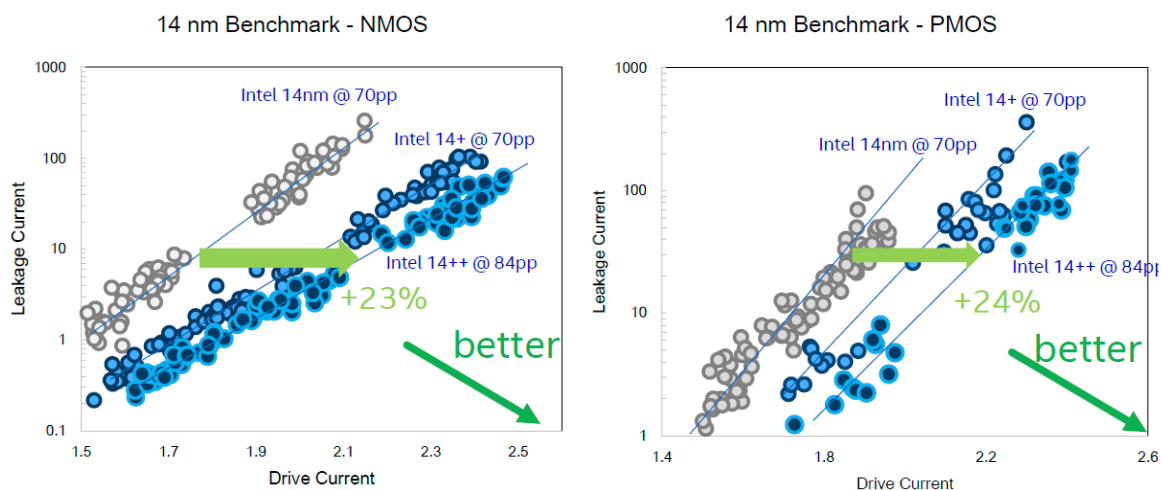


Figure 9: 3 versions of 14-nm technology by Intel, showing increased current drive with lower leakage current [Fischer2017].

Commercial 14-nm processes propose up to 3 threshold options, namely high-Vt (HVT), regular Vt (RVT), and low Vt (LVT).

- HVT – High Threshold Voltage causes less power consumption, but switching is slow. HVT are used in power critical functions.
- LVT – Low Threshold Voltage causes more power consumption and switching timing is optimized. LVT are used in time critical functions.
- RVT – Regular Threshold Voltage (sometimes called Standard VT or SVT) offers trade-off between HVT and LVT i.e., moderate delay and moderate power consumption.

In Microwind, we only use 2 types of MOS devices for the core and reuse the same name as for previous nano-CMOS technologies:

- Low leakage MOS (LL), close to RVT
- High Speed MOS (HS), close to LVT

Parameter	In Microwind
$V_{DD\ core}$ (V)	0.8
Effective gate length (nm)	16
MOS variants	2
Ion N (mA/ μ m) at 0.8V	1.3 (LL) 1.7 (HS)
Ion P (mA/ μ m) at 0.8V	1.1 (LL) 1.4 (HS)
Ioff N (nA/ μ m)	1 (LL) 10 (HS)
Ioff P (nA/ μ m)	1 (LL) 10 (HS)
Gate dielectric	HfO ₂
Gate stack	Al/TiN
Equivalent oxide thickness (nm)	0.9

Table 4: Key features of the core devices proposed in the 14-nm technology

IO MOS devices

Table 5 gives an overview of the key parameters for the 14-nm technological concerning the Input/output MOS devices and associated supply voltage. In Microwind, we only consider 1.2V I/O supply and tune the “High-Voltage” (HV) MOS device on the median performances. Other standards usually supported in commercial 14-nm process include 1.2, 1.5 and 1.8V I/O supply.

Parameter	High Voltage (HV) MOS in Microwind
$V_{DD\ IOs}$ (V)	1.2
Effective gate length (nm)	100
Ion N (mA/ μ m)	0.3
IonP (mA/ μ m)	0.22
Ioff N (nA/ μ m)	0.1
Ioff P (nA/μm)	0.1

Table 5: Key features of the I/O devices proposed in the 14- nm technology and corresponding values in Microwind

3. Transistor performances in 14-nm technology

Designing a 1µm-width FinFET

The evaluation of the equivalent FinFET channel width corresponds to the following formulation (Eq. 1). The evaluation of the current is usually expressed in mA/µm, meaning that a 1-µm equivalent width FinFET design is needed to evaluate the current. In the proposed 14-nm technology, H_{FIN} is 40nm, W_{FIN} 8nm, so one fin has an equivalent width of 88 nm (Figure 10).

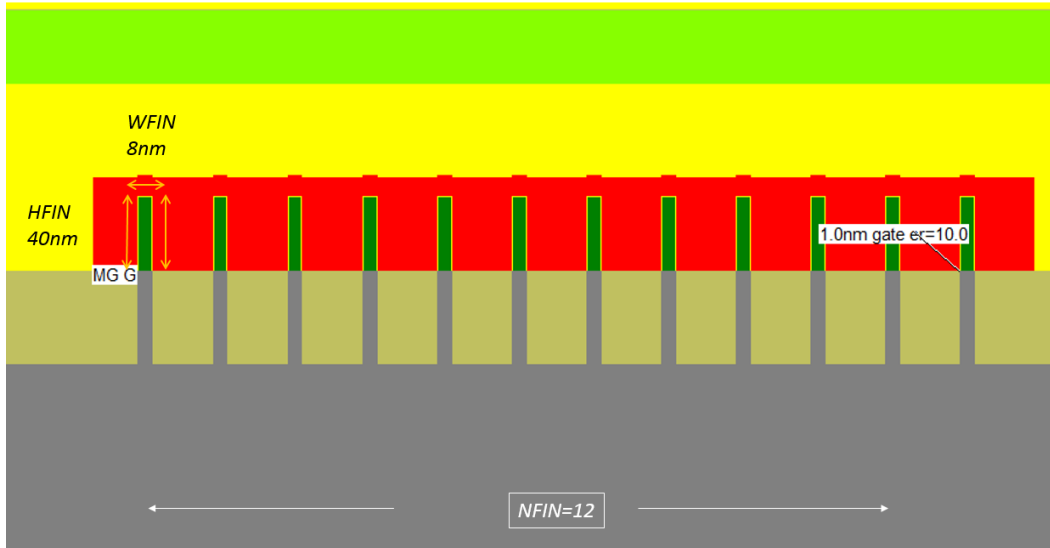


Figure 10: The equivalent width of a multi-fin FET

$$W_{eq} = (2 \times H_{FIN} + W_{FIN}) \times N_{FIN} \quad \text{Eq. 1}$$

$$W_{eq} = (2 \times 40 + 8) \times 12 = 1056 \text{ nm} \approx 1 \mu\text{m} \quad \text{Eq. 2}$$

An equivalent width of 1µm, as it would be designed using MosFET’s, corresponds to around 12 fins in 14-nm technology. As seen in Fig. 11, the FinFET with a 1-µm width is smaller than a MosFET with the same width. We get the following I/V characteristics (Fig. 11) for n-channel FinFET and p-channel FinFET.

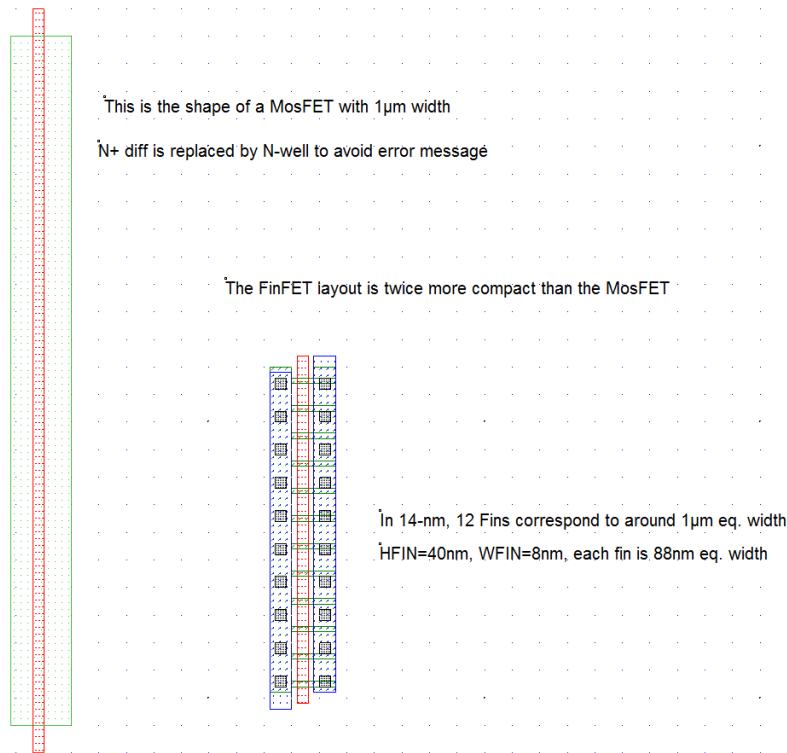
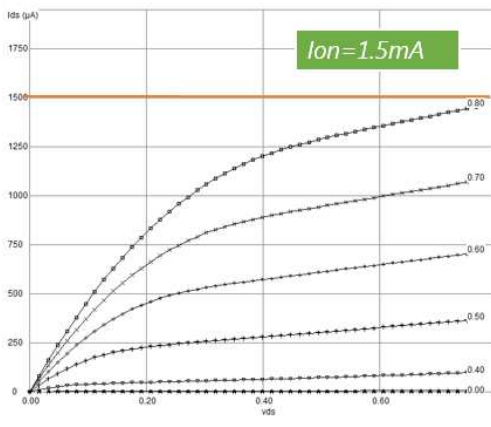
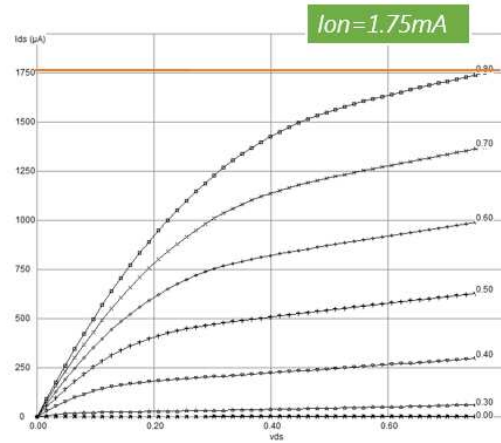


Figure 11: The multi-fin FET with an equivalent width of 1 μ m is almost twice more compact than the MosFET traditional design



Microwind's Low Leakage n-FinFET (Regular VT)
 12 fins, Weq=1 μ m,
 L=16 nm



Microwind's High speed n-FinFET (Low VT)
 12 fins, Weq=1 μ m,
 L=16 nm

Figure 12: Id/Vd characteristics of the low leakage and high speed nMOS devices.

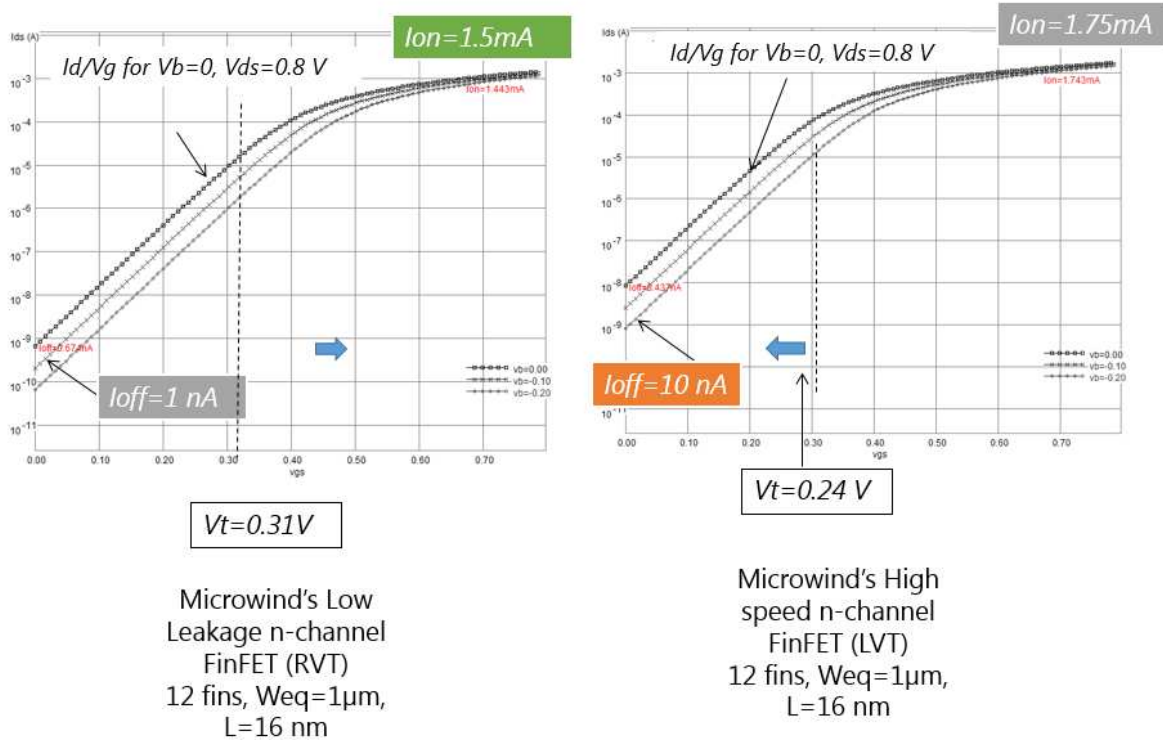


Figure 13: I_d/V_g characteristics (log scale) of the low leakage and high-speed nMOS devices

The I/V characteristics of the low-leakage and high-speed MOS devices (Figs. 12 and 13) are obtained using the MOS model BSIM4. As shown in the figures, the low-leakage NMOS has a drive current capability of around 1.5 mA with 12 fins (equivalent to $W=1.0\mu\text{m}$) at a voltage supply of 0.8 V. For the high speed NMOS, the drive current rises to 1.75 mA/ μm .

The drawback associated with this high current drive is the leakage current which rises from 1 nA/ μm (low leakage NMOS) to 10 nA/ μm (high speed NMOS), as seen in the I_d/V_g curve at the X axis location corresponding to $V_g=0\text{ V}$ (Fig. 13). From a design view-point, the “option” menu in the MOS generator enables to switch from low leakage to high-speed. In terms of layout, the only difference is the option layer that contains the MOS option information (Fig. 14), which can be Low leakage (Regular V_t), High Speed (Low V_t), or High Voltage.

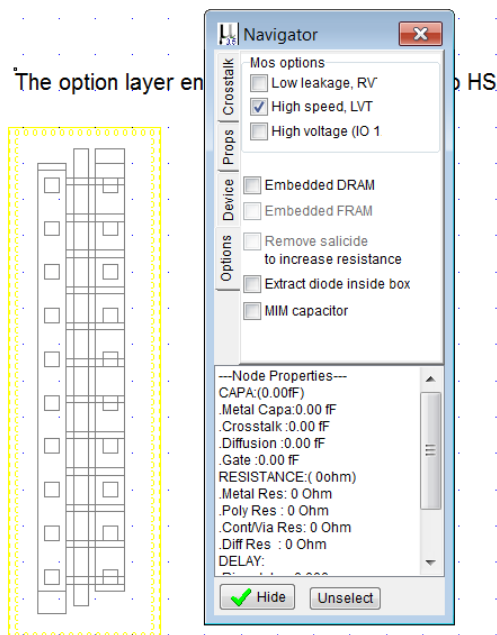


Figure 14: Changing the option of the device from low-leakage to high-speed using the option layer. Double-click in one corner of the option layer to change its properties

P-channel MOS device characteristics

The p-FinFET drive current in 14-nm technology is quite similar to the n-FinFET thanks to the strain engineering for PMOS that nearly compensates the intrinsic mobility degradation of holes (P-channel) vs. electrons (N-channel). The leakage current is around 1 nA/μm for the low-leakage device and nearly 10 nA/μm for the high-speed device (Fig. 15).

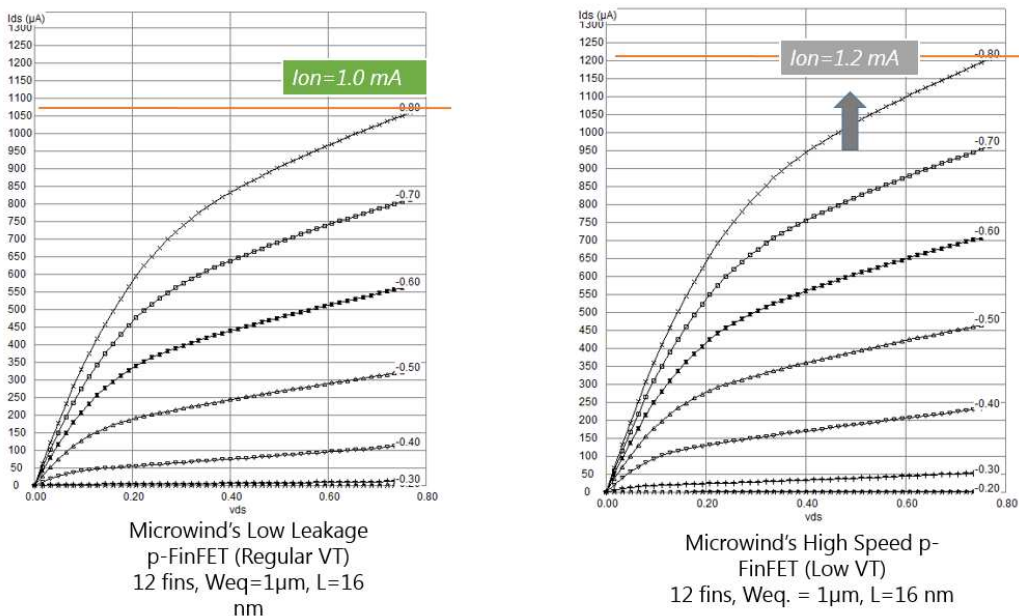


Figure 15: Id/Vg characteristics of the low leakage and high-speed p-FinFET devices

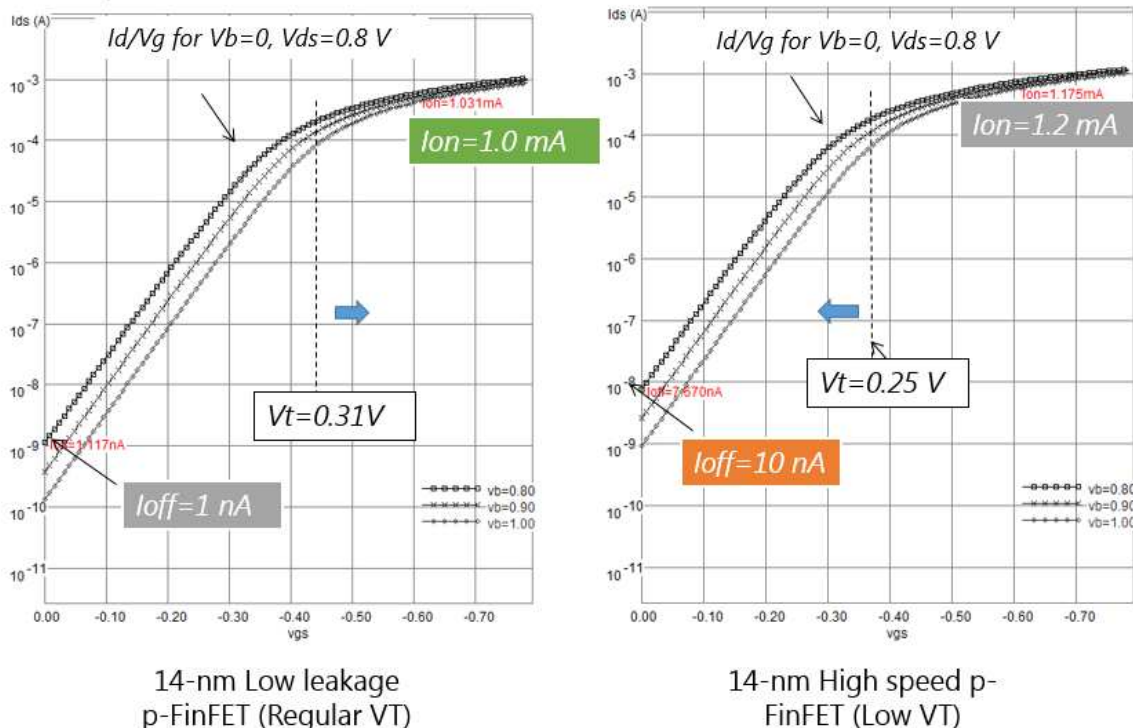


Figure 16: I_d/V_g characteristics (log scale) of the low leakage and high-speed p-FinFET devices

4. MOS Design for Manufacturing

Process Variability

One important challenge in nano-CMOS technology is process variability. The fabrication of millions of MOS devices at nano-scale induces a spreading in switching performances in the same IC.

The effect of process variability on the MOS I_{off}/I_{on} characteristics is plotted using the menu “ I_{off} vs. I_{on} ” under the “MOS I/V curve” menu (Fig. 17). It can be seen that the MOS devices have a wide variability in performances. The 3 MOS types (low leakage, high speed, high voltage) are situated in well-defined space in the I_{off}/I_{on} domain. The low leakage is in the middle (medium I_{on} , low I_{off}), the high speed on the upper right corner (high I_{on} , high I_{off}), and the high voltage is at the lower left side of the graphics (low I_{on} , very low I_{off}). Note that the exact locations of the dots will change for each MOS characteristics plotted because it is a random process.

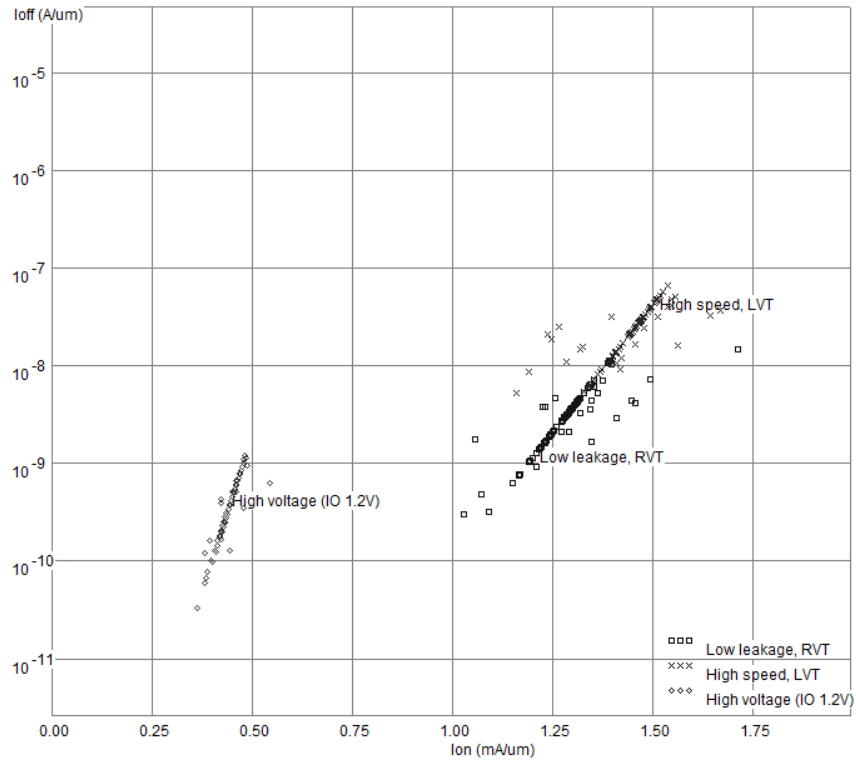
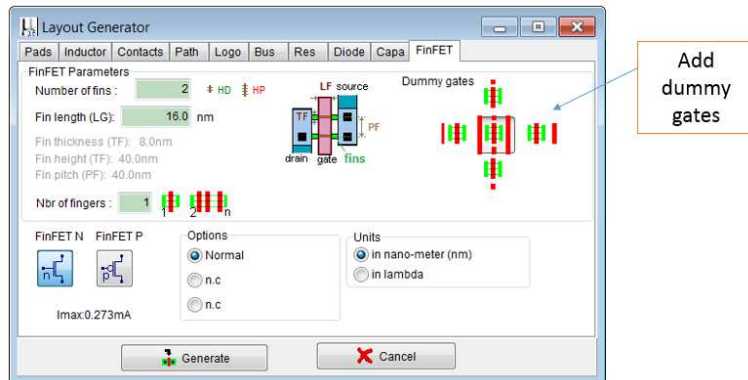


Figure 17: I_{off}/I_{on} calculated on 100 samples of n-FinFET with random distribution of V_T , U_0 , and $LINT$ with a Gaussian distribution around the nominal value

Dummy gates

One solution to reduce MOS performance variability is to design in a regular way the MOS gates. An option exists in the device generator to add “dummy” gates around the active device (Fig. 18). The variability of lithography depending on the environment will significantly affect the dummy gate, but only little the central active gate.



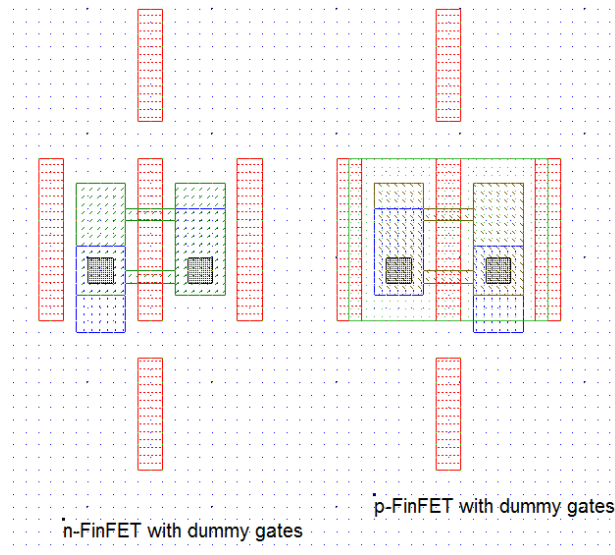


Figure 18: The layout generation includes the dummy gate option at any side (or all sides) of the active device to reduce variability and increase manufacturability

5. Interconnects

Metal Layers

As seen in figure 19, the original 14-nm technology from Intel [Brain2017, Natharajan2014, Fischer2015] comprises 10 to 12 layers depending on the option (here “High Performance” and “High Density”), the lower ones for short routing, the medium ones for long routing, and the upper ones for various purpose including supply network, Metal-Insulator-Metal (MIM) capacitance, and high quality embedded coil inductors thanks to a very thick upper layer ($1\mu\text{m}$). One innovation described by [Fischer2015] is the airgap in metal layers M4 & M6, which lowers the equivalent dielectric permittivity. As a consequence, the interconnect capacitance is reduced by around 15%, leading to an equivalent RC delay reduction.

In Microwind, only 8 metal layers are considered, according to table 6:

- M1 & M2 are at 6λ pitch for local routing
- M3 & M4 are at 8λ pitch for medium routing
- M5 & M6 are at 32λ pitch for long routing and local supply
- M7 & M8 are dedicated to power supply and coil inductance

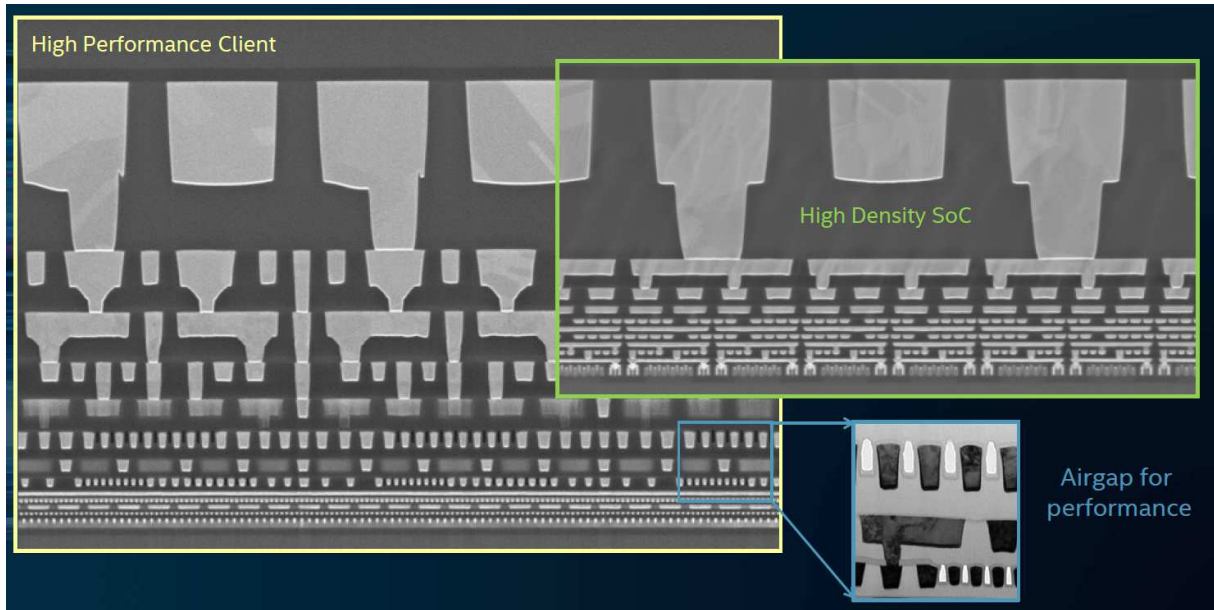


Figure 19: Intel’s 14-nm technology with 10 to 12 metal layer options [Brain2017]

Parameter	Pitch (nm)	Pitch (λ)	Rules	Thickness (nm)	Thickness parameter	Purpose
M1	48	6	R501, R502	68	Thme	Short routing
M2	48	6	R701, R702	68	Thm2	Short routing
M3	64	8	R901, R902	80	Thm3	Medium routing
M4	64	8	RB01, RB02	80	Thm4	Medium routing
M5	128	16	RD01, RD02	80	Thm5	Long routing
M6	128	16	RF01, RF02	80	Thm6	Long routing
M7	368	46	RH01, RH02	150	Thm7	Supply, very long routing
M8	600	75	RJ01, RJ02	600	Thm8	Supply, Coil inductance

Table 6: Key features of interconnects in the 14-nm technology implemented in Microwind

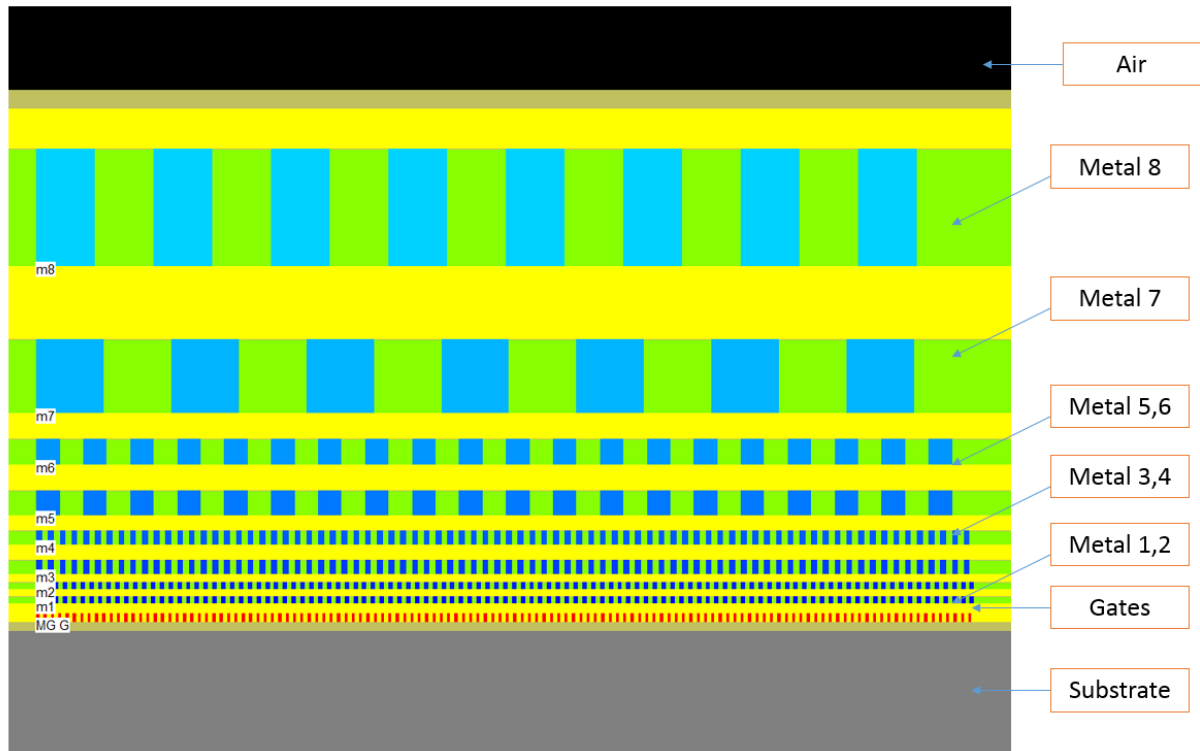


Figure 20: The 8 metal layers proposed in 14-nm technology

Layers *metal5* and *metal6* are a little thicker and wider, while layers *metal7* and *metal8* are significantly thicker and wider, to drive high currents for power supplies (Fig. 20).

Interconnect Resistance

The resistance and capacitance of interconnects are an important metric for evaluating the RC delay and consequently the switching speed of the signals. In figure 21, the spread of capacitance and resistance of Intel’s 14-nm metal2 using a 52-nm pitch is reported [Fischer2015]. The order of magnitude is 43 ohm/μm and 0.3 fF/μm.

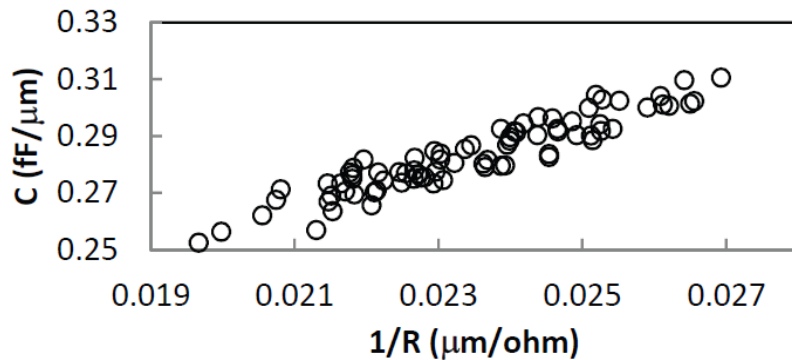


Figure 21: C and R per μm for metal 2 with 52-nm pitch, (Intel’s 14-nm technology [Fischer2015])

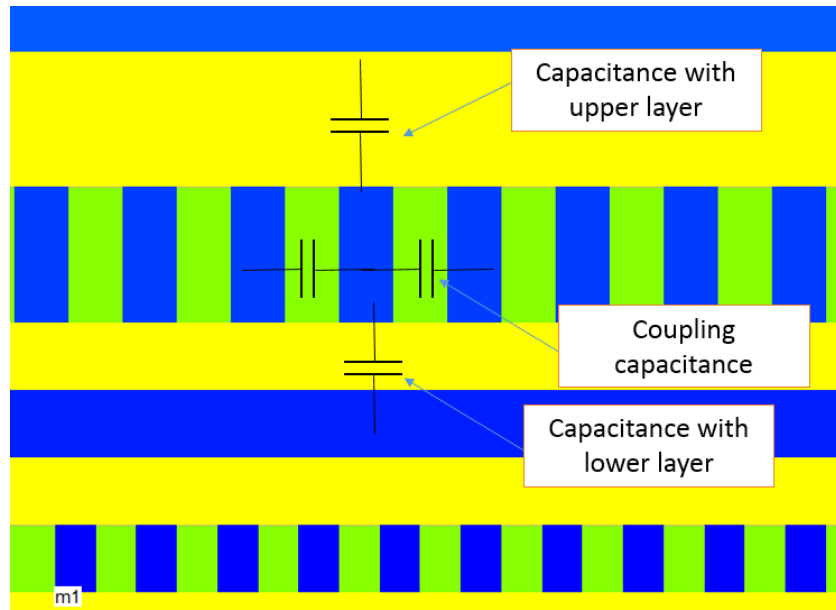


Figure 22: The interconnect capacitance is the sum of upper, lower and sidewall capacitance

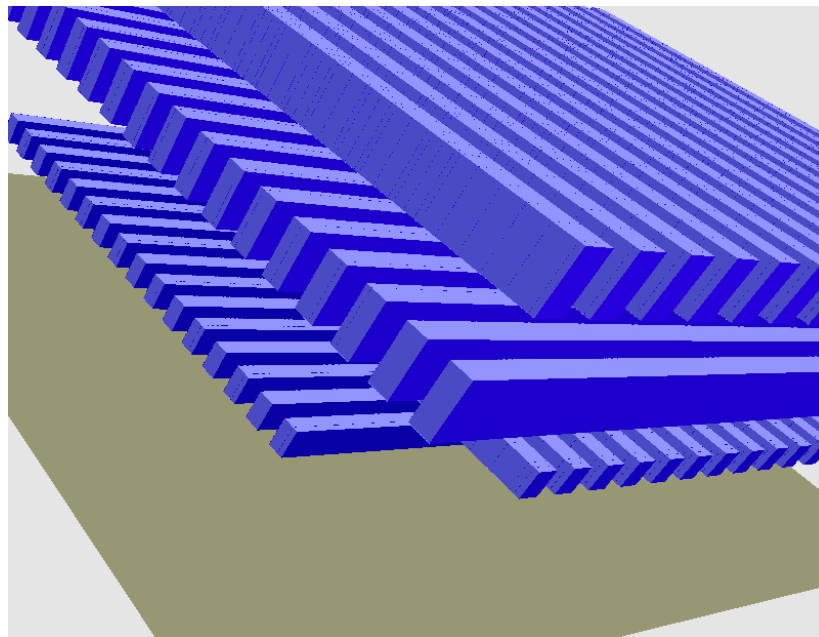
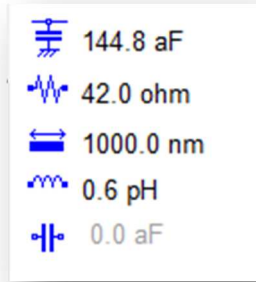
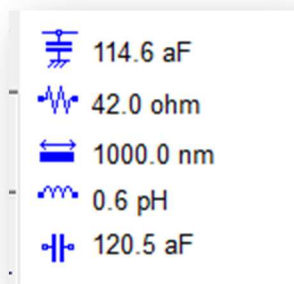
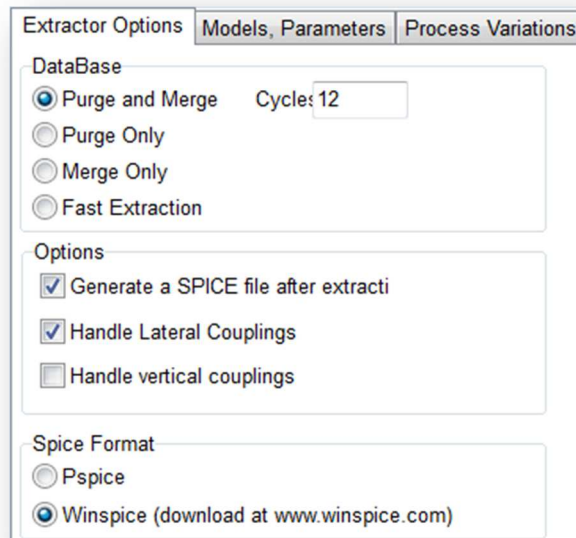


Figure 23: 3D view of interconnects in M1-M4, with a 1µm length (metals-m1-4-1mm-14nm.MSK)

We may draw a set of interconnects with 1µm length in metal1, 2, 3 and 4 (Figs. 22 and 23) with standard width and spacing. The estimation of R,LC of a metal2 interconnect lead to the following results.



We can see that the resistance is close to Intel’s values at comparable pitch and length (Around 40 $\Omega/\mu\text{m}$). However, the capacitance is underestimated: 0.15 fF instead of 0.3 fF. The main reason is the crosstalk capacitance that may be evaluated using the simulation parameter “Handle Lateral Couplings”, or “Simulate with Crosstalk”. Consequently, the total node capacitance is close to 0.25fF/mm, a value close to [Fischer2015].



Double Patterning for M1-M2 Interconnects

The double patterning is required for metal layers as the pitch between tracks is smaller than 80nm. Half the patterns go on the first patterning and half go on the second patterning, as illustrated in Fig. 24. In order to ensure an easy selection of metal tracks for the first and second patterning, regular structures with straightforward orientation such as M1 east-west, and M2 south-north are requested. The other solution is to relax the pitch constraints for an improved manufacturability, at the cost of an extended silicon area. M3-M8 with pitch of 80-nm and higher are still fabricated using simple patterning.

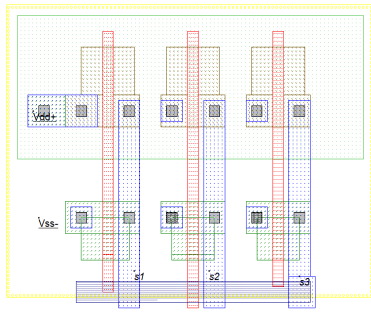


Figure 24: Single, double and quadruple patterning as a function of interconnect pitch [Brain2017]

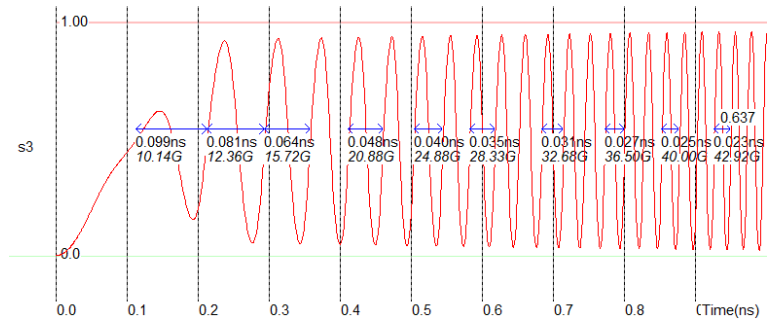
6. Ring Inverter Simulation

Performances

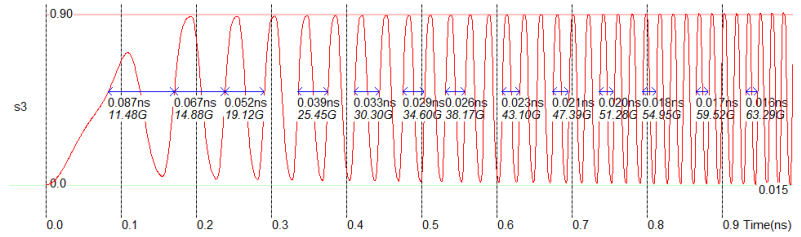
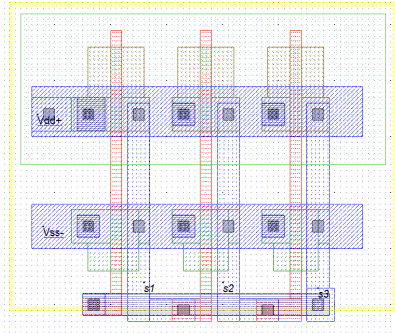
An improvement of switching performances as high as x 4 is obtained between 45nm and 14nm designs, a result close to [Xie2015, Steegen2015], although VDD is reduced from 1.1V to 0.8V. Microwind operates with lambda-based designs which are independent of the technology, but MosFET and FinFET designs are not compatible. However, comparison remains possible at similar drive currents, circuits and design styles. As seen in Fig. 25, a 3-inverter ring oscillator (RO) features a natural 43 GHz oscillation in 45-nm, which rises to nearly 200 GHz with 14-nm technology. Using High Speed option instead of Low Leakage improves 10-20% more the frequency, with increased power consumption.



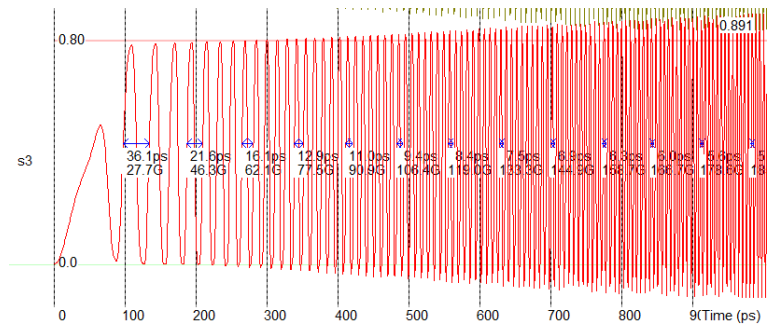
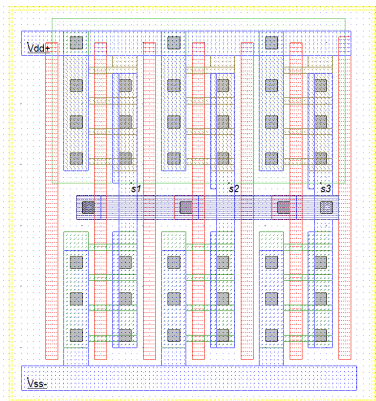
Three inverters in series (Free oscillation)



45nm RO3, FO1, MosFET



20nm RO3, FO1, MosFET



14-nm RO3, FO1, FinFET

Figure 25: Considerable speed improvement is observed between 45-nm 3-stage ring oscillator based on MosFET and 14-nm 3-stage ring oscillator based on FinFET

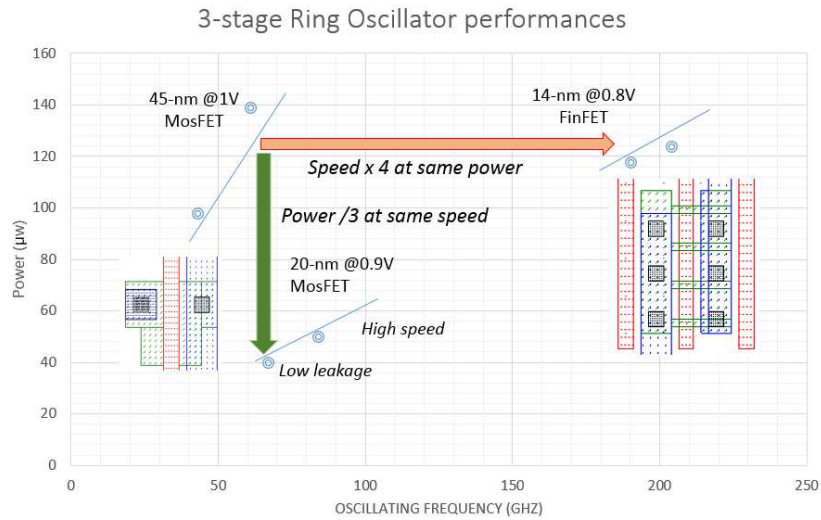


Figure 26: Plot of RO3 oscillating frequency as a function of power dissipation, for three technologies and device options.

The trends towards increases switching speeds is illustrated in Fig. 26. At similar power dissipation (around 100µW), the speed improvements is as high as a factor of 4. Similar trends may be found in [Stegen2015].

Minimum VDD

We extract the minimum VDD value for which the ring oscillator is still operating. The VDD value can be changed through the command **Simulate** → **Simulation Parameters**. We can also use the command **Analysis** → **Parametric Analysis**, click on the S3 node, select VDD voltage from 0.5 to 0.95, and monitor the frequency. It can be seen that the ring oscillator do not operate below 0.6V (Fig. 27).

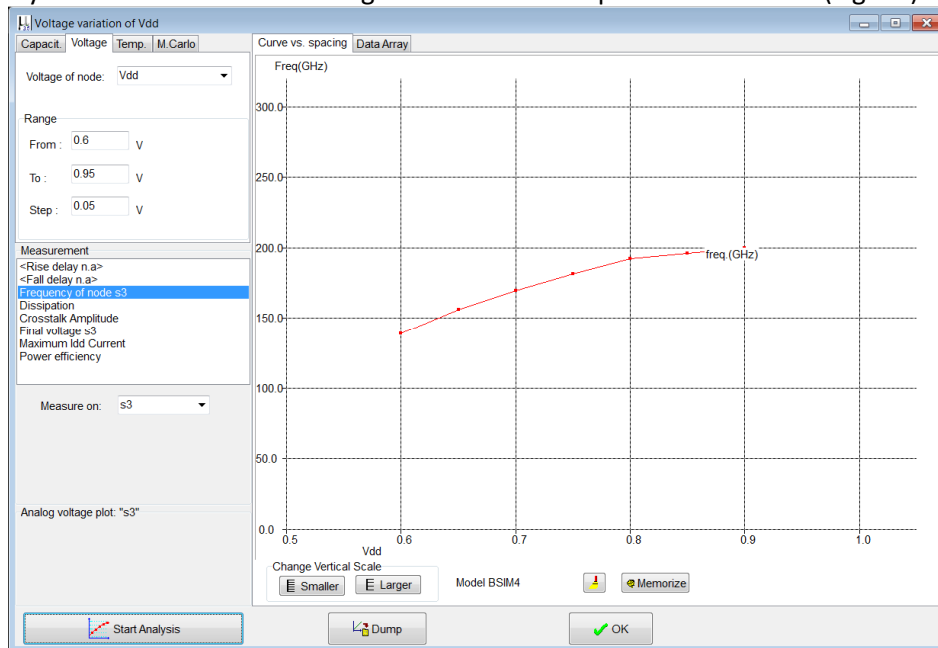


Figure 27: Modify VDD to extract the minimum operating voltage of the ring oscillator.

Simulation of Process Variations (PVT)

Considerable differences may be observed in terms of performances, depending on the process, voltage and temperature conditions. The usual temperature range is [-50°C..+125°C], the voltage variation VDD+/- 10%, and the process may also vary +/-15% for some key parameters such as the threshold voltage and mobility. Microwind gives access to “Process-Voltage-Temperature” (PVT) simulation through the command **Simulate** → **Simulation Parameters** → **Process Variations**. Direct access from the simulation waveform window is also possible using the button “**Process Variations**”. The most usual simulation consists of simulating extreme situations (Min and Max), as compared to typical conditions (Table 7).

- In *Min* situation, VT is high and the mobility U0 is low. The supply is minimum and the temperature is maximum. The ring oscillating is around 100 GHz.
- In *Max* situation, VT is low, mobility U0 is high and the channel is short (LINT<0). The supply is maximum and the temperature is minimum. The ring oscillation is around 250 GHz.

Parameter class	Parameter	Symbol (BSIM4)	Unit	Min (14-nm)	Typ (14-nm)	Max (14-nm)
Process	Threshold Voltage	VT	V	0.36	0.31	0.27
	Mobility	U0	m2/V.s	0.030	0.035	0.040
Voltage	Supply	VDD	V	0.68	0.8	0.92
Temperature	Temperature	TEMP	°C	125	25	-50
Oscillating frequency				100	196	250

Table 7: Variation of process parameters: the oscillating frequency ranges from 100 to 250 GHz

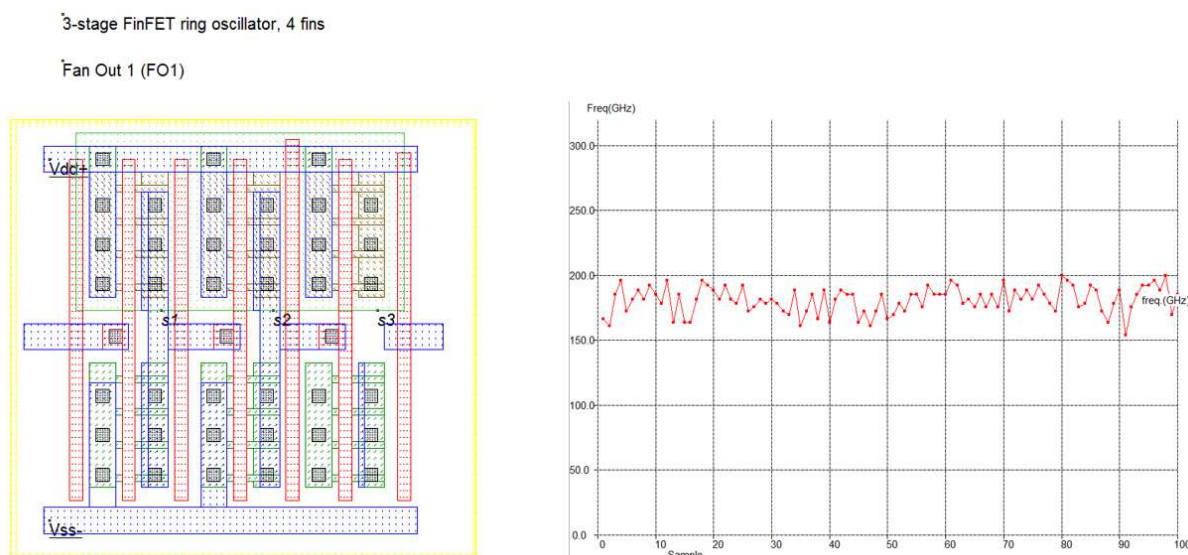


Figure 28: Monte-carlo simulation with 100 random sets of technology parameters

Another type of simulation consists in choosing a set of random variables and produce several iterations. Figure 28 shows the oscillation frequency variation with 100 random samples. The variation is much less as the random variation is of normal distribution around the typical values.

7. 6-transistor static RAM

One of the most representative designs for comparing technology nodes is the static RAM cell designed using 6 transistors (6T-SRAM). The size reduction from 22 to 14-nm process is illustrated in Fig. 29 with Intel’s implementation of the 6T-SRAM, with a surface divided nearly by 2. In our implementation in Microwind (see Fig. 30), the layout size is 328 x 129 nm, with a surface area of 0.043 μm^2 , close to [Song2015]. The layout obeys the basic design rules. Most contacts are shared with neighboring cells: the VSS, VDD contacts, the Select and Data lines. It is usual to find more aggressive layout design rules in RAM cell designs, in order to further decrease the cell area.

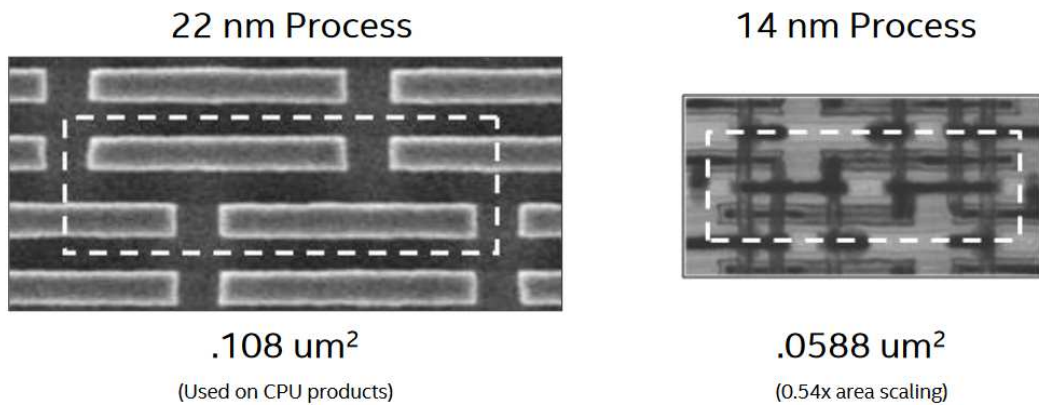


Figure 29: Reduction of the 6T-SRAM memory from 22-nm to 14-nm process of Intel [Natharajan2014, Fischer2015]

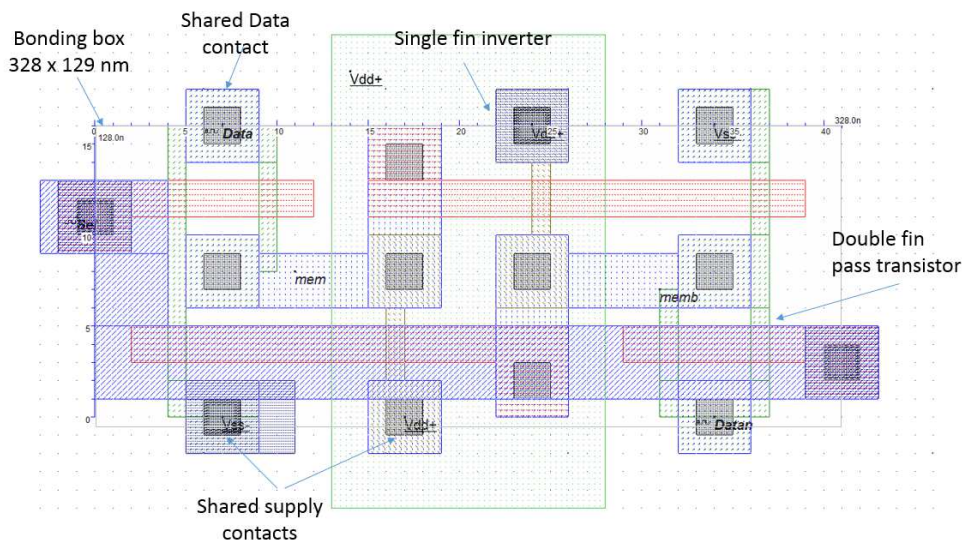


Figure 30: 6T-SRAM implementation in FinFET (SRAM-6T-14nm.MSK)

8. Conclusions

This application note has illustrated the trends in CMOS technology and introduced the 14-nm technology generation, based on technology information available from manufacturers. The key features of the 14-nm CMOS technology have been illustrated, including the FinFET, design for manufacturing and double patterning. A 3-stage ring, FinFETs with 1- μm equivalent width as well as interconnects with 1- μm length have been used for comparison purpose.

Acknowledgements

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