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A Comprehensive Compact Model for the Design of All-Spin-Logic Circuits

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By relying on pure spin transmission and low-frequency charge-spin conversions, All Spin Logic (ASL) has the potential to replace CMOS technology, which relies only on pure charge currents. As ASL technology is gaining in maturity, compact models are needed to fill the gap between application requirements and circuit fabrication. However, defining such a model is a tedious task due to the numerous physical parameters to consider and the need for flexibility to explore design tradeoffs. In this paper, we propose an accurate, generic, scalable, and easy-to-use compact model for ASL devices. The model has been validated by comparing with experimental results, which allows investigating the impact of device characteristics such as channel length and channel width on the propagation delay. The model has been implemented in Cadence using in Verilog-A, which allows running transient simulations and comparing the implementations of 4-bit adder and multiplier circuits regarding the area, energy and delay metrics.

Index Terms—Spintronic, All Spin Logic, circuit design, compact model.

I. INTRODUCTION

SPINTRONIC devices have the potential to lower the power consumption of computing systems and to reach nanometer scales. Indeed, All Spin Logic (ASL) devices [1], [2] allow pure spin transmission and low-frequency charge-spin conversions, while CMOS technology relies on pure charge currents only. The design of ASL device-based circuits leads to numerous challenges related to the heterogeneity they introduce and the large design space to explore. As the technology is gaining in maturity, compact models are needed to fill the gap between application requirements at the system level and circuit fabrication at the device level. In particular, accurate simulations of spin injection/detection effects are needed to estimate the magnetic tunnel junction (MTJ) [3] switching time and spin diffusion delay according to materials properties. Furthermore, the models should be generic to allow exploring fabrication-related device parameters such as channel lengths and MTJ sizes. Such exploration should allow investigating not only performances tradeoffs but should also help designers to prevent from device damages. For instance, an injection current that is not properly calibrated can damage graphene (resp. metal)-based channels due to Joule heating (resp. electromigration) effects. Finally, a scalable approach is mandatory to investigate the design of complex, hierarchical circuits. It is worth noticing that, to be adopted by the designer community, the approach should be compliant with current standardized CMOS-based design techniques and should be implemented in an existing commercial environment.

Hence, there is a need for accurate, generic, scalable, and easy-to-use, i.e. comprehensive, compact models. However, to our knowledge, there is no such model in the literature. Indeed, models have been implemented in MatLab to execute

transformed conductance matrix [4]. These approaches are not scalable and cannot be used for complex circuits design. Verilog-A model proposed in [5] implements ASL device as a single block, which avoids exploring the design space for its optimization and the hierarchical design. A circuit simulation environment relying on basic electrical circuit elements such as resistors, capacitors and current sources has been defined in [6], and a scalable Verilog-A model is proposed in [7]. Both approaches do not integrate important characteristics such as spin diffusion delay and channel breakdown effects.

The following summarizes the contributions of the paper:

- Comprehensive ASL device compact model taking into account spin-transfer torque effect [8], spin diffusion delay [9] and channel breakdown effect [10]–[14].
- IP block-like organization of the model, which allows the independent design of injector, detector, channel and contact devices. This allows cross-layer optimization of ASL-based circuits and eases the design of hierarchical, complex circuits.

This paper is organized as follows. Section II introduces the ASL device-based circuit fundamental and related work. Section III presents the proposed compact model, which has been implemented in Cadence using Verilog-A. In Section IV, we investigate the design of hierarchical 4-bit adders and multipliers circuits. In Section V, we validate the model through comparisons with experimental results and Cadence simulations are carried to compare implementations. Section VI concludes the paper and gives perspectives to this work.

II. BACKGROUND AND RELATED WORK

A. ASL Fundamental

Fig. 1 (a) illustrates the ASL device we consider. It is mainly composed of i) two perpendicular MTJs (Fig. 1 (b)) to inject/detect spin currents and store spin information and ii) a channel for spin current transmission. The MTJ is composed

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of one oxide barrier sandwiched between two ferromagnetic layers (FMs). Depending on the relative magnetization orientations of two FM layers, the MTJ has two resistance levels (R_P and R_{AP}) that are represented by states “0” and “1”. The state of MTJs is written by applying a voltage/current source (V_{write}/I_{write}) above a critical current I_{c0} . Then, a charge current I_{inj} is injected through the MTJ free layer and polarized into the channel. With spin-flipping and diffusion through the channel, the spin current arriving at the detector will switch the MTJ state if it is larger than the critical current I_{c0} . The resulting state S_{out} depends on the injected current I_{inj} polarity and the input MTJ state S_{in} . A negative (resp. positive) value for I_{inj} — injected from MTJ free layer to the channel (channel to free layer), will lead to $S_{out} = S_{in}$ (resp. $S_{out} = not(S_{in})$).

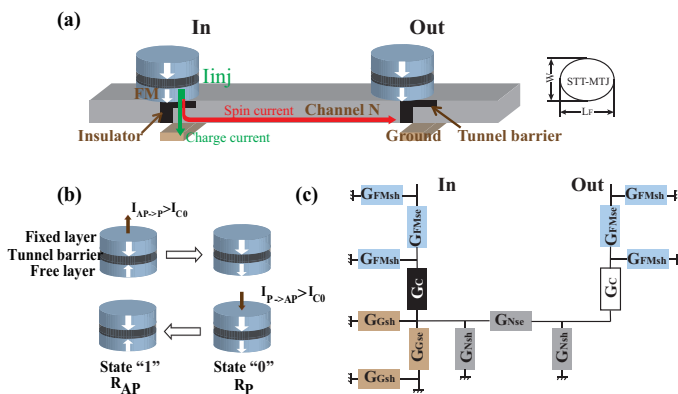


Fig. 1. (a) ASL device with an asymmetric structure. (b) MTJ parallel state (R_P , represented by “0”) and anti-parallel state (R_{AP} , represented by “1”). (c) Spin circuit model of basic ASL device. Each block is a π -network of conductance matrix, and corresponds with the component in (a).

B. Related ASL Compact Modeling

Spin-circuit-based compact modeling has been proposed in [4]. In this model, each device is represented as a π -network with the conductance matrices, which allows ASL-based circuits implementation and analysis. However, such approach is not scalable since complex circuits design leads to large-scale matrices that need to be carefully established. Furthermore, the model is implemented in MatLab, which is not a suitable platform for the designer community. In [5], the authors proposed a compact model integrating all the devices into a single block using a set of predefined equations. Such model is not suitable for hierarchical circuit design since the bloc is specific to a given cell. A circuit simulation environment relying on electrical circuit elements has been proposed [6] and an ASL model has been implemented with Verilog-A [7]. Both approaches enable the design and the simulation of spintronic devices-based circuits using a circuit solver such as HSPICE. However, they do not integrate important characteristics such as spin diffusion delay and channel breakdown effects. Different from existing models, we propose a comprehensive compact model that relies on the Maxwell’s equations adapted to the spin domain. This leads to an implicit definition of current and voltage

relations in circuits, which thus ensure generic design solution. This very flexible model has been decomposed into blocks corresponding to injector/detector, channel, ground and contact devices. Furthermore, for the first time, our model takes into account channel breakdown and channel spin diffusion delay effects. This allows preventing from destructive design options and helps the designer calibrating the devices (e.g. injection current specification). Our model is implemented with Verilog-A on Cadence platform, which allows designing hierarchical and complex circuits in an environment already used by the designer community.

III. PROPOSED ASL MODEL

This section presents the ASL compact model we propose. We first present the details of the model and we then introduce the Verilog-A implementation in Cadence.

A. Compact Model

The aim of this work is to propose a comprehensive model for ASL device which combines MTJ and spin injection/detection models. The MTJ model relies on physical equations proposed in [8], which allow taking into account i) tunneling resistance, ii) TMR effect, iii) spin transfer torque effect: switching threshold current and dynamic switching delay. Different from the related models, the spin injection/detection model we propose also takes into account the spin diffusion delay and the channel breakdown, as detailed in the following.

a) *Modified Maxwell’s equations for ASL model*: Our ASL compact model relies on current-voltage equations deduced from Maxwell’s equations in the spin domain. The set of equations defined in [15] corresponds to the generalized form of Kirchhoff’s Potential and Flow laws (KPL and KFL). They are defined by:

$$j = \sigma \nabla \mu + \sigma_s \nabla \mu_s \quad (1)$$

$$j_s = \sigma_s \nabla \mu + \sigma \nabla \mu_s \quad (2)$$

where j (resp. j_s) is the charge (resp. spin) current density, σ (resp. σ_s) is the charge (resp. spin) conductivity and μ (resp. μ_s) is the charge (resp. spin) quasi-chemical potential. From these basic current rules, we thus define a set of charge and spin currents device-specific rules. In our model, ρ (ρ_s) is the charge (spin) resistivity, L is the channel length, L_s is the spin diffusion length and t is the thickness.

We assume 4 types of devices: injector/detector, contact, channel and ground, and define their charge/spin currents as follows:

- Injector and detector:

$$I_F(0) = \frac{\pi W L_{Fi}}{4 \rho_{Fi} t_{Fi}} \Delta \mu + \frac{\pi P_{Fi} W L_{Fi}}{4 \rho_{Fi} L_{sFi}} \mu_{sFi}(0) \quad (3)$$

$$I_{sF}(0) = \frac{\pi P_{Fi} W L_{Fi}}{4 \rho_{Fi} t_{Fi}} \Delta \mu + \frac{P_{Fi}^2 \pi W L_{Fi}}{4 \rho_{Fi} L_{sFi}} \mu_{sFi}(0) \quad (4)$$

where W is the MTJ width, P_{Fi} is the ferromagnet spin conductivity polarization and t_{Fi} is the free layer thickness.

- Contacts:

$$I_{Ci} = \frac{\pi W L_{Fi}}{8 R A_{Ci}} \Delta \mu + P_{Ci} \cdot \frac{\pi W L_{Fi}}{8 R A_{Ci}} \Delta \mu_s \quad (5)$$

$$I_{sCi} = P_{Ci} \cdot \frac{\pi W L_{Fi}}{8 R A_{Ci}} \Delta \mu + \frac{\pi W L_{Fi}}{8 R A_{Ci}} \Delta \mu_s \quad (6)$$

where P_{Ci} is the spin resistance polarization of the contact and $R A_{Ci}$ is the resistance area product of the contact. We assume two types of contacts: i) a simple FM-N contact with no material between the ferromagnet and the channel and ii) a more complex contact involving a Tunnel Barrier (TB) to improve the spin injection efficiency.

- Channel:

$$I_N = \frac{W t_N}{\rho_N L_N} \Delta \mu \quad (7)$$

$$I_{sN}(0/L_N) = \frac{W t_N}{\rho_N L_{sN}} \left[\frac{\mu_{sN}(L_N) - \mu_{sN}(0)}{\sinh(L_N/L_{sN})} \mp \frac{(\cosh(L_N/L_{sN}) - 1) \mu_{sN}(L_N)}{\sinh(L_N/L_{sN})} \right] \quad (8)$$

where L_N is the channel length.

- Ground:

$$I_G = \frac{L_{Fi} t_G}{2 \rho_G L_G} \Delta \mu \quad (9)$$

$$I_{sG} = \frac{L_{Fi} t_G}{2 \rho_G L_{sG}} \mu_{sG}(0) \quad (10)$$

b) Channel breakdown and diffusion delay:

- The average transit time of carriers through the interconnect proposed in [9] is defined as:

$$t_{DIFF} = \frac{L_N^2}{2D} + \frac{L_N}{v_f} \quad (11)$$

where $L_N^2/2D$ is the diffusive time constant and L_N/v_f is the ballistic time constant. D is the electron diffusion coefficient, and v_f is the Fermi velocity of electrons.

- A channel is characterized by a breakdown current density J_{BD} . It corresponds to an upper limit a current density should not exceed to avoid channel destruction or malfunction. As detailed in [10]–[14], the physical phenomenon induced by the breakdown current depends on the channel material:

- For a metal material, a large current density leads to a high electromigration, which results in the breakdown of the channel. By considering the copper material, the Blech model [13], [14] allows defining the maximum current density $J_{BR,Cu}$ by:

$$J_{BR,Cu} \times L_N = \frac{\Omega \Delta \sigma}{Z^* e \rho_{Cu}} \quad (12)$$

where Ω , $\Delta \sigma$, Z^* are the atomic volume, normal stress difference between stripe ends and the effective valence of Cu, respectively; ρ is the resistivity and e is the electron charge.

- For semiconductor material, channel breakdown occurs when Joule heating effect leads to a temperature

larger than the fusion point. For such a material, the maximum current density is defined by [11], [12]:

$$J_{BR} = \left[\frac{g(T_{BD} - T_0)}{\rho_N t_N W} \times \frac{\cosh(\frac{L_N}{2L_H}) + g L_H R_T \sinh(\frac{L_N}{2L_H})}{\cosh(\frac{L_N}{2L_H}) + g L_H R_T \sinh(\frac{L_N}{2L_H}) - 1} \right]^{1/2} \\ g^{-1} = \left\{ \frac{\pi k_{ox}}{\ln[6(t_{subox}/W + 1)]} + \frac{k_{ox}}{t_{subox}} W \right\}^{-1} \\ + \frac{R_{Cox}}{W} + \frac{1}{2k_{Si}} \left(\frac{L_N}{W + 2t_{subox}} \right)^{1/2} \\ R_T \approx L_{Hm} / [k_m t_m (W + 2L_{Hm})] \\ L_{Hm} = [k_m / (k_{ox} t_m t_{subox})]^{1/2} \quad (13)$$

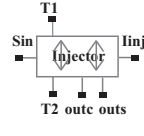
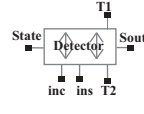
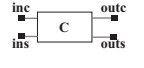
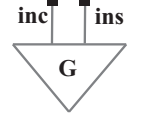
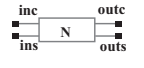
Where T_{BD} and T_0 are the breakdown and room temperatures respectively; g is the contact thermal resistance per length unit, $L_H = \sqrt{k_g W t_N / g}$ is the thermal healing length, k_g is the thermal conductivity of channel material, k_{ox} and t_{subox} are the thermal conductivity and thickness of the substrate, respectively; R_{Cox} is the contact thermal resistance between channel and substrate, K_{Si} is the thermal conductivity of the highly doped Si substrate, R_T is the contact thermal conductance, L_{Hm} is the thermal healing length of heat spreading into the contact, k_m and t_m are the thermal conductivity and thickness of the metal electrodes.

B. Verilog-A Implementation

The compact model has been implemented in Cadence using Verilog-A. Table I represents the 5 symbols corresponding to the following ASL devices and their parameters: *Injector* and *Detector*, contacts C_{TB} and C_{FM-N} (Tunnel barrier and FM-N interface), ground lead G and channel N . Each block describes the current-voltage relations of the device, based on the equations previously described. *Injector* and *Detector* also take into account the spin torque switching effect and N integrates the spin diffusion and channel breakdown effects. The following details the 5 blocks:

- “*Injector*” integrates a resistance tunneling model, a STT model and a spin injection model. The state of an MTJ depends on the voltage source V_{write} connected to terminals “ $T1$ ” and “ $T2$ ”. The MTJ state is output on terminal S_{in} , taking into account the switching delay. The output is represented as a voltage signal: “ $V=0V$ ” and “ $V=1V$ ” correspond to parallel and anti-parallel state respectively. Once the MTJ state has been configured, an injection current I_{inj} is injected into the channel from the MTJ free layer through the terminal “ I_{inj} ”. This leads to a charge current “*outc*” and a spin current “*outs*”.
- “*C*” corresponds to the contact model, which can be implemented with or without tunnel barrier (TB). The two input terminals “*inc*” and “*ins*” represent the input charge and spin currents. Terminals “*outc*” and “*outs*” represent the output charge and spin currents.
- “*G*” and “*N*” correspond to the ground and channel model respectively. Part of the charge and spin currents

TABLE I
ASL DEVICE PARAMETERS.

	Symbol	Parameter (unit)	Description	Default value	Range
Global		W (nm) T_0 (K)	Device width Temperature	40 300	[25,50] — ⁴
Injector		$TMR(0)$ ⁵ α^3 H_k^3 (A/m) M_s^3 (A/m) ρ_F ($\Omega \cdot m$) L_{sF} (nm) P_F	TMR ratio with 0 V_{bias} Ferromagnetic damping factor Ferromagnetic anisotropy field Ferromagnetic saturation magnetization Ferromagnetic resistivity Ferromagnetic spin diffusion length Ferromagnetic spin polarization	120% 0.027 270×10^3 [3] 1.1×10^6 [3] 2.6×10^{-6} 0.2 0.5	[60,600]% [0.007,0.027] X ⁵ X — — [0,0.99]
Detector		State L_F (nm) t_{ox} (nm) t_F (nm) RA_F^3 ($\Omega \mu m^2$)	MTJ state representation MTJ length MTJ Oxide barrier height MTJ free layer height MTJ resistance area product	“0” (P) “1” (AP) 40 0.85 1.3 5	— [25,50] [0.8,1.5] — [5,15]
Contact		$Type_C$ P_C RA_C ($\Omega \mu m^2$)	Contact type selection Contact spin resistance polarization Contact resistance area product	1 (with TB) 0 (without TB) 0.5 100 (with TB) 8.79×10^{-4} (without TB)	1, 0 [0,0.99] X
Ground		L_G (μm)	Ground length	1	$\geq L_{sN}$
		t_m^1 (nm)	Metal electrode thickness	5 [11]	X
		k_m^1 ($Wm^{-1}K^{-1}$)	Metal electrode thermal conductivity	22 [11]	X
		k_{Si}^1 ($Wm^{-1}K^{-1}$)	Thermal conductivity of the highly doped Si substrate	100 [11]	—
		t_{subox}^1 (nm)	Substrate thickness	90 (SiO_2) [11]	X
		k_{ox}^1 ($Wm^{-1}K^{-1}$)	Substrate thermal conductivity	1.4 (SiO_2) [11]	—
Channel		RC_{ox}^1 (m^2KW^{-1})	G/N-substrate interface thermal contact resistance	1×10^{-8} [11]	X
		T_{BD}^1 (K)	G/N material breakdown temperature	875 [11]	X
		k_g^1 ($Wm^{-1}K^{-1}$)	G/N material thermal conductivity	100 (graphene) [11]	X
		v_f^2 (m/s)	G/N material fermi velocity of electrons	0.8M (graphene)	X
		D^2 (m^2/s)	G/N material electron diffusion coefficient	0.02 (graphene)	X
		$t_{G/N}^6$ (nm)	G/N material thickness	“1” (graphene) ⁶	X
		$\rho_{G/N}$ (Ω^6)	G/N material resistivity	2.86×10^3 (graphene) ⁶	X
		$L_{sG/N}$ (μm)	G/N material spin diffusion length	1	X
		$Type_{G/N}$	G/N material selection	1 (semi), 0 (metal)	1, 0
		$\frac{\Omega \Delta \sigma}{Z^* e}$ (ΩA)	Metal G/N breakdown current density calculation factor	5.1×10^{-4} (copper) [10]	X
		L_N (nm)	Channel length	90	$< 0.8L_{sN}$

¹ Parameters used to calculate the breakdown current density for semiconductor material.

² Parameters used to calculate the spin diffusion time.

³ Parameters used to calculate MTJ spin transfer torque and TMR effects.

⁴ Parameters are fixed in this model.

⁵ Parameters depend on the material.

⁶ The unit of the graphene resistivity is [Ω] and the graphene resistance is calculated as $R = \rho_N \times \frac{L_N}{W}$ instead of $R = \rho_N \times \frac{L_N}{W \times t_N}$. We thus arbitrary set the graphene thickness to “1”. The resistivity unit of other materials is [Ωm]; the material thickness is thus set to the actual one.

outputted by the contact flows into the ground while the remaining part flows into the channel, where it will propagate until reaching a detector.

- “Detector” corresponds to block able to switch a MTJ state according to the current flowing through a contact. Above a threshold current, the “State” terminal is switched to 1V (parallel) or 0V (anti-parallel) depending on the injection current polarity and the MTJ state input. The state can be read by applying a voltage source “ V_{read} ” to terminals “T1” and “T2” and is output to “Sout” terminal.

Fig. 2 illustrates a 3-input majority gate and its implementation in Cadence. It is composed of 2 input terminals to input data ($In1$ and $In2$), 1 control terminal (F), 1 output terminal (Out) and 4 channels. We assume a same channel length $L1$ between the channel crossing and the inputs. A length $L2$

characterizes the channel linking the crossing to the output MTJs. Depending on the state of F and the injection current polarity, AND/OR/NAND/NOR2 function is configured.

Obviously, the implementation in Cadence follows the same structure: the MTJs and the channels are represented by 4 components; C_{TB} , C_{FM-N} and G correspond to the contact and the ground respectively. Each component is configured according to various parameters (e.g. channel lengths and injection currents). From such a model, one can design hierarchical circuits, run the simulation, and explore design parameters, as it will be shown in the result section.

IV. HIERARCHICAL CIRCUIT DESIGN

The aim of the proposed model is to allow designing realistic, hierarchical, ASL devices-based circuits. In this section, we investigate the design of two 4-bit adders and a 4-bit

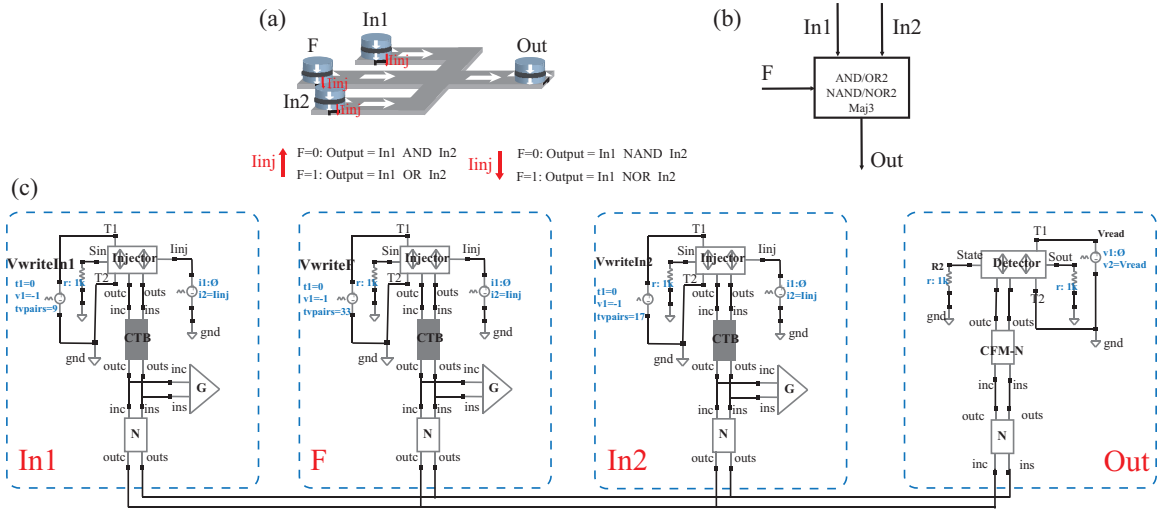


Fig. 2. (a) 3-input majority gate architecture: $In1$ and $In2$ as inputs, F as control terminal, Out as output. (b) Functional symbol of the 3-input majority gate. (c) Implementation in Cadence of ASL-based 3-input majority gate. Inj ector/ Det ector are the input/output ferromagnet/MTJ blocks; C_{TB} and C_{FM-N} are contact block with and without tunnel barrier respectively; G is ground lead block; N is channel block.

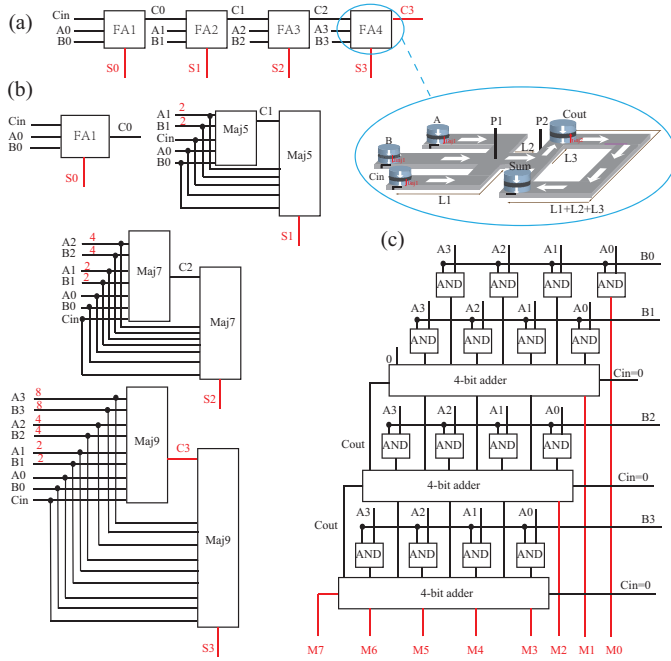


Fig. 3. (a) serial adder, (b) parallel adder and (c) multiplier. For the parallel adder, numbers on red correspond to the weights.

multiplier. Adders and multipliers play an important role in today's digital signal processing and many other applications. Since they are designed according to multiple objectives (latency, power, layout regularity and area), it is important to explore the design space by taking into account physical properties of the devices.

A. 4-bit Adder

We investigate serial and parallel implementations described in the following. For both circuits, the operands are $A = A_3A_2A_1A_0$ and $B = B_3B_2B_1B_0$.

1) Serial adder

The serial adder is implemented by cascading full-adders [16] (Fig. 3 (a)). A full adder requires to sum-up the spin current injected from three MTJs (A , B and C_{in}), which is achieved using the same channel crossing structure described for the 3-inputs majority gate (i.e. 4 channels are needed). The resulting spin current then diffuses toward C_{out} and Sum MTJs: since C_{out} result is required to compute Sum , a fifth channel connects both MTJs. The length of this channel is L_3 .

Fig. 3 (a) illustrates the serial adder. The carry-out from a stage propagates to the next stage, hence introducing a delay in the computation. The total delay of the circuit is the sum of 4 contributions: i) the MTJ state writing time ($\times 1$ since all the inputs are injected simultaneously), ii) the time needed to change the state of intermediate signals ($\times 5$ on the critical path which includes 4 carry signals and 1 sum) and iii) the MTJ state reading time ($\times 1$ since all the results are read simultaneously). The implementation of the serial adder requires 20 MTJs.

2) Parallel adder

Replacement and duplication method leads to a parallel implementation of the adder. Compared to the serial adder, the parallel adder is expected to reduce the latency at the cost of extra resources and energy. For its implementation, input carry C_{i-1} of stage i is replaced with its primary inputs $A_{0/\dots/i-1}$, $B_{0/\dots/i-1}$ and the weights of the original inputs of this stage A_i , B_i are duplicated. Eq. 14 shows an example for C_1 .

$$\begin{aligned} C_1 &= Maj(A_1, B_1, C_0) \\ &= Maj(A_1, B_1, A_1, B_1, A_0, B_0, C_{in}) \end{aligned} \quad (14)$$

The number of inputs increases with the stage as follow: both C_i and S_i require $2^i A_i/B_i$, $2^{i-1} A_{i-1}/B_{i-1}$ and so on. As illustrated in Fig. 3 (b), the parallel adder is implemented using 3/5/7/9-inputs majority gates. Compared to the serial adder, the delay of the parallel adder is expected to decrease since there is no carry propagation. Indeed, in addition to MTJ

state writing time ($\times 1$) and reading time ($\times 1$), critical path delay includes the time to change the state carry signal ($\times 1$) and sum signal ($\times 1$).

B. 4-bit Multiplier

The considered 4-bit multiplier is illustrated in Fig. 3 (c). $A = A_3A_2A_1A_0$ and $B = B_3B_2B_1B_0$ are the multiplicator and the multiplicand respectively. A classical array structure is used: the first stage is the multiplication of A_i and $B_{0/1}$; results are transmitted to the second stage, where additions occur, etc. The multiplier is implemented using 16 AND gates (each AND gate corresponds to a 3-inputs majority gate configured for AND function) and three 4-bit adders, for which serial and parallel implementations are possible. The multiplier is thus a hierarchical circuit for which multiple design options are possible. In the results section, we will investigate delay-area design tradeoffs.

V. SIMULATION RESULTS

A. Model Validation

In order to setup the simulation environment, we first tune the compact model in order to match with characterization results. For this purpose, we simulate the spin resistance ΔR_s , for which experimental data have been reported in the literature for Py/Mg (ferromagnet/channel) [17] and Py/Cu [18] materials. By adjusting the spin polarization to 0.58 (resp. 0.37) and the channel spin diffusion length to 205 nm (resp. 320 nm) for Py/Mg (Cu) material, the simulation results are well aligned with characterization results, as illustrated in Fig. 4.

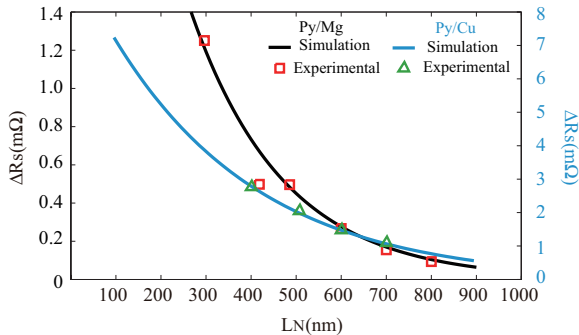


Fig. 4. Simulation and characterization results ΔR_s comparison for channels implemented with Mg and Cu materials.

B. Device Simulation

In the following, device level simulations are carried out in order to estimate the breakdown current and the delay. We assume a graphene channel, which leads to the use of the default values defined in Table I. Fig. 5 reports the estimated breakdown current according to the length and the width of the channel. The area located under a line corresponds to current density values leading to a channel working properly. The area located above a line corresponds to current density values exceeding the breakdown current, which are likely to damage the

channel due to Joule self-heating or electromigration damages effects (for semi-conductor and metal materials respectively). The larger the channel area, the smaller J_{BD} . This is due to the lateral 3D heat spreading into the substrate, the contacts and along the graphene channel. The heat transfer depends on the thermal conductance and hence on its length and width: a small channel length/width leads to high thermal conductance, which contributes to maintaining the heat spreading along the graphene and into the contacts [12].

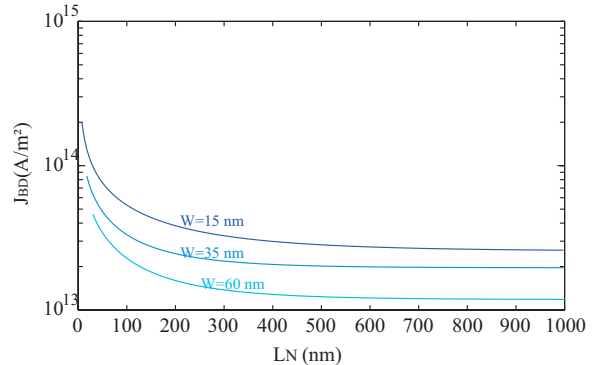


Fig. 5. Channel breakdown current density J_{BD} according to channel length L_N and channel width W .

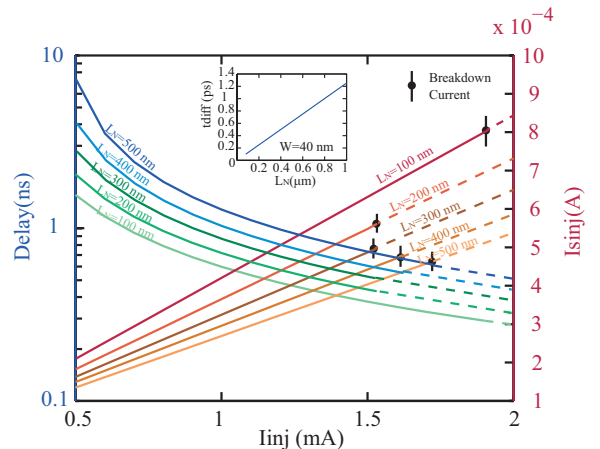


Fig. 6. Delay and channel spin current I_{sinj} according to the injection current I_{inj} and channel lengths L_N . For each channel length, the breakdown current is labeled on I_{sinj} curves. The following defines i) the maximum injection current, ii) the corresponding spin injection current and iii) the delay according to the channel length: (1.9 mA, 803 μA , 0.292 ns) for 100 nm, (1.587 mA, 581 μA , 0.4164 ns) for 200 nm, (1.565 mA, 509 μA , 0.5039 ns) for 300 nm, (1.63 mA, 478 μA , 0.5586 ns) for 400 nm, (1.72 mA, 463 μA , 0.6108 ns) for 500 nm. Inset gives the spin diffusion delay t_{diff} according to L_N .

In the following, we assume the ASL device illustrated in Fig. 1 (a) and we investigate the impact of the injection current I_{inj} and the channel length L_N on the delay. Fig. 6 gives the evolution of the delay for I_{inj} ranging from 0.5 mA to 2 mA. As an example, for a 500 nm channel length, the delay decreases from 7.3 ns for $I_{inj} = 0.5$ mA to 1.27 ns for $I_{inj} = 1$ mA. We also plot the spin current I_{sinj} injected to a channel according to I_{inj} . The plain line corresponds to injection current value respecting the breakdown current constraints while dashed line represents

cases for which channel is likely to be damaged. For instance, for $L_N = 100 \text{ nm}$, the breakdown current is estimated to be $803 \mu\text{A}$, which corresponds to a maximum value of 1.9 mA for I_{inj} . The inset represents the spin diffusion delay t_{diff} according to L_N and for $W = 40 \text{ nm}$. Results show that t_{diff} approximates 1 ps range, which can be neglected considering to the MTJ switching delay (100 ps to few ns for $W = 40 \text{ nm}$). It is worth noticing that the diffusion delay is expected to play a significant role in the total delay as MTJ fabrication technology will gain in maturity.

In the following, we investigate the impact of the channel length on the delay of the 3-input majority gate illustrated in Fig. 2 (a). We define $L1$ (resp. $L2$) as the distance between the injector and the channel crossing (resp. the distance between the channel crossing and the detector). We consider $I_{inj} = 700 \mu\text{A}$, which allows keeping the current density below the breakdown current for the total channel sizes we assume (100 nm , 200 nm and 300 nm). As illustrated in Fig. 7, the delay decreases while $L1$ increases, which is due to the fact that the backflow current (e.g. current coming from $In1$ and going to $In2$ at the crossing point) decreases as $L1$ channel resistance increases. Hence, for a 3-input majority gate, the optimal solution is obtained for $L2 = 0$. From a layout point of view, this can be easily implemented by implementing the crossing structure below the detector. However, such a layout is not possible for more complex devices such as a 5-input majority gate, which can thus be optimized using channel length exploration.

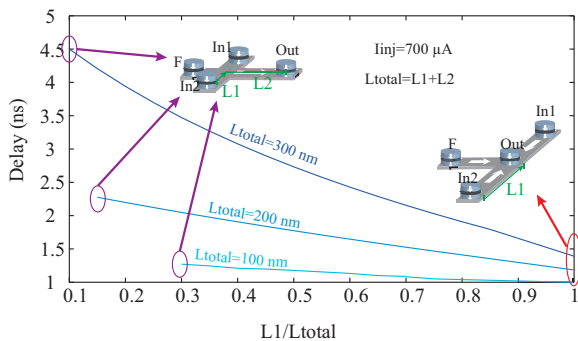


Fig. 7. Propagation delay (including switching and spin diffusion delays) for a 3-input majority gate.

C. Circuit Simulation

Based on the developed compact model, we use Cadence to run transient simulations for 4-bit adder and multiplier circuits. We consider 40 nm MTJs and $1 \mu\text{m}$ for the channel spin diffusion length. Regarding the 3-input majority gate illustrated in Fig. 2 (resp. Full-Adder illustrated in Fig. 3), we assume $L1 = 70 \text{ nm}$ and $L2 = 30 \text{ nm}$ (resp. $L1 = 50 \text{ nm}$, $L2 = L3 = 25 \text{ nm}$).

1) 3-input majority gate

Fig. 8 illustrates the simulation results of the 3-input majority gate considering $I_{inj} = 700 \mu\text{A}$. Simulation results validate the functional behaviors of the 3-input majority gates, which can implement the AND/OR/NAND/NOR functions

depending on i) the state of the control terminal F and ii) the injection current polarities. The average delay of this gate is 0.9 ns .

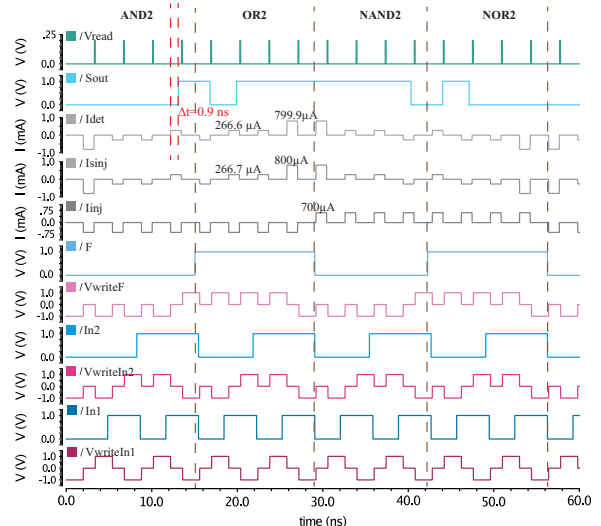


Fig. 8. Simulation results for a 3-input majority gate. V_{writei} is the MTJ write voltage source for the i terminal; $In1/In2/F$ are injector input terminals; I_{inj} is the injection current for all the input terminals; I_{sinj} is the spin current on the injector side; I_{det} is the spin current on the detector side; S_{out} is the gate output state; V_{read} is the voltage source applied to the detector to read the state of the MTJ.

2) 4-bit adders

For the serial adder, we first set the injection current I_{inj1} to 1.07 mA , which leads to the maximum spin current allowed in the channel. Then, considering the length of the channels and the weights needed to compute Sum (the weight of C_{out} is twice the weight of A , B and C_{in}), I_{inj2} is set to $973 \mu\text{A}$. We assume two values for the ferromagnetic damping factor: $\alpha = 0.027$ relies on a conservative technology while $\alpha = 0.007$ is a more aggressive technology leading to a lower MTJ threshold current. As reported in Table II, we obtain 13.1 ns (resp. 9.63 ns) for the average delay and 3.2 nJ (resp. 2.35 nJ) for the energy consumption for a conservative (resp. aggressive) technology. It is worth noticing that a design space exploration (e.g. on the channel lengths, device width) could be carried out to improve the performance of the circuit.

The same approach has been followed for the parallel adder. For $\alpha = 0.027$, the spin current received by the detector is too small to switch the MTJ state. Since a higher injection current will damage the channel, this circuit implementation is not realistic for a conservative technology. When implemented with a more aggressive ferromagnetic damping factor, the spin current can be detected, which leads to 5.8 ns delay and 3.3 nJ energy consumption (see Table II). Traditional design tradeoffs relying on area, power and delay can thus be investigated to compare serial and parallel implementations.

3) 4-bit multiplier

In order to illustrate the scalability of our model, we design and simulate 4-bit array multipliers relying on serial and parallel adders. Fig. 9 illustrates a simulation result and Table II summarizes the area, energy and delay for conservative and aggressive parameters. We conclude from this study that our

TABLE II
ADDERS AND MULTIPLIERS PERFORMANCE COMPARISON.

Circuit		Area (μm^2)	$\alpha = 0.027$		$\alpha = 0.007$	
			Energy (nJ)	Delay (ns)	Energy (nJ)	Delay (ns)
4-bit adder	Serial	0.32	3.2	13.1	2.35	9.63
	Parallel	0.84	N/A	N/A	3.3	5.8
4-bit Multiplier	Serial	1.6	11.1	39.8	8.35	29.3
	Parallel	3.16	N/A	N/A	11.2	17.8

model not only allows comparing circuits but also helps to identify, early in the design process, the limits induced by a given technology.

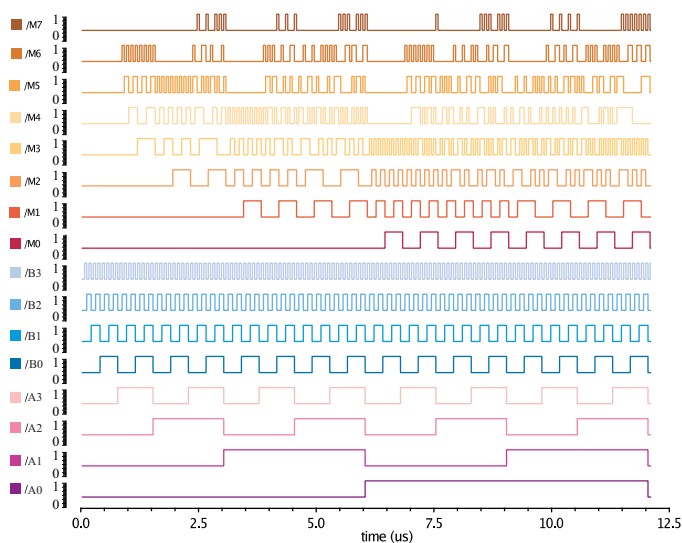


Fig. 9. Simulation results of a 4-bit array multiplier with serial adders. $A_3 \cdots A_0$ and $B_3 \cdots B_0$ are the operands; $M_7 \cdots M_0$ are the outputs.

VI. CONCLUSION

In this paper, we propose a comprehensive compact model for ASL devices. The model relies on extended Maxwell's equations in the spin domain and allows taking into account both spin diffusion delay and channel current density breakdown. After validating the model by comparing with experimental results, we have investigated the impact of device characteristics such as channel length and channel width on the propagation delay. Furthermore, the model has been implemented with Verilog-A in Cadence, which allows running transient simulations and comparing the implementations of the 4-bit adders and multipliers circuits regarding the area, energy and delay metrics. In our future work, we will investigate design space exploration to optimize the circuits performances.

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