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# Robustness of SiC MOSFET under Avalanche Conditions

Ilyas Dchar, Marion Zolkos  
SuperGrid Institute  
130 rue Léon Blum,  
F-69100, Villeurbanne, FRANCE

Cyril Buttay, Hervé Morel  
Univ Lyon, CNRS, INSA-Lyon  
Laboratoire AMPÈRE, UMR 5005  
F-69621, Villeurbanne, FRANCE

**Abstract**— In high voltage direct current (HVDC) converters, a series connection of semiconductor devices is often used to achieve the desired blocking voltage. In such configuration, an unequal voltage sharing may drive one or more devices into avalanche breakdown, eventually causing the failure of the entire group of devices. This paper presents the experimental evaluation of SiC MOSFETs from different manufacturers operated in avalanche. A setup was developed to test the devices under such condition. The reliability of SiC MOSFETs have been compared. To correlate the experimental results with the failure mechanism, the MOSFETs were decapsulated to identify the failure sites on the SiC dies. Examination results show that for some tested devices, the failure occurs at the metallization source of the die, and results in a short circuit between all three terminals of the MOSFETs. Furthermore, it has been found that the parasitic BJT latch up and the intrinsic temperature limit are the main failure mechanisms for these devices.

**Keywords**— Reliability, SiC MOSFET, Avalanche breakdown, Failure mechanism, Critical energy, Parasitic BJT.

## I. INTRODUCTION

After years of research and studies, silicon-carbide (SiC) semiconductor devices have become commercially available for high-power applications. The interest of SiC as a material for high voltage is mainly due to its superior properties, which exceed those of silicon, especially: a larger bandgap and a higher critical field [1]. However, SiC devices have a lower maturity level than their silicon counterparts, which may cause some reliability issues. For gated structures (such as MOSFETs), two phenomena may result in degrading their robustness. First, the electric field through the gate oxide is ten times stronger than that of silicon-based devices [2]. The higher electric field and the thin layer of the gate oxide may reduce the reliability of the gate. Furthermore, the carrier injection into the gate oxide is much higher in SiC devices than that of Si.

Many papers have been published on the topic of the behavior of SiC MOSFETs under short-circuit operation [2]-[3]-[4]. However, the reliability of SiC MOSFETs has not been verified fully under single avalanche conditions. Ji Hu *et al.* presented a failure mechanism analysis for SiC MOSFET under avalanche mode conduction [5]. It was reported that avalanche failure of SiC MOSFET results from two mechanisms: First, there is BJT latch-up caused by high avalanche energy dissipated over short avalanche durations. This mechanism is exacerbated by variations in the electrical parameters between

different cells in the MOSFET which cause current focusing and temperature surges (hot spots) [6]. The second mechanism concerns the intrinsic temperature limit of the device which may happen at low energy over long duration [7].

In this paper, tests are carried out to understand ruggedness of commercial SiC MOSFETs regarding single pulse avalanche conditions, but also to analyze their failures mechanisms. Tests are performed on two types of 1200 V and 1700 V SiC MOSFETs manufactured by Wolfspeed (C2M0045170D and C2M0080120D) and a third type of MOSFETs from ROHM (SCH2080KE). The characteristics of these devices are summarized in Table I.

TABLE I. RATED CHARACTERISTICS OF SiC MOSFETs

	V <sub>BR</sub> (V)	I <sub>D</sub> (A)	R <sub>on</sub> (mΩ)	Die size (mm <sup>2</sup> )
<b>DUT 1</b> (C2M0080120D)	1200	36	80	10.41
<b>DUT 2</b> (C2M0045170D)	1700	72	45	29.98
<b>DUT 3</b> (SCH2080KE)	1200	40	80	12 (MOSFET die) 9.1 (SBD die)

This investigation is organized as follows. In section II the experimental setup is described and test protocol is presented. Section III shows the measurement results. Section IV discusses the failure mechanisms. Finally conclusions are given in Section V.

## II. EXPERIMENTAL SETUP

### A. Description of the bench

Figure 1 shows the structure of the avalanche test circuit used for the experiment. This circuit is described with more details in [8]. It consists in a high voltage source  $V_E$ , a pulse voltage generator, a current limiting resistor  $R$  (50 Ω), a capacitor bank (1250 μF, 3000 V) and the DUT. An auxiliary high voltage IGBT (3 kV/500 A) is connected in series with the MOSFET to control the avalanche duration of the DUT. The IGBT is driven with an isolated gate signal. Figure 2 shows the picture of the test bench based on the circuit schematic in Fig. 1. For safety reasons, the circuit is placed in a metal enclosure which includes the high voltage power supply, the capacitors, the test zone, and a control panel. An interlocking mechanism, connected to a high voltage contactor, prevents any accidental contact with high voltage. The implementation of these safety systems required a

fairly long cabling between the capacitors and the test zone, resulting in a relatively large total stray inductance (10  $\mu\text{H}$ ).

The test circuit in Fig.1 was chosen instead of a more common UIS (Unclamped Inductive Switching) set up [9] because it is more versatile (short-circuit tests, not presented here, can be performed too). With the circuit in Fig. 1, the avalanche energy can be varied without using different inductors: here, the voltage across the capacitor bank and the duration of the pulse are the only parameters to set.

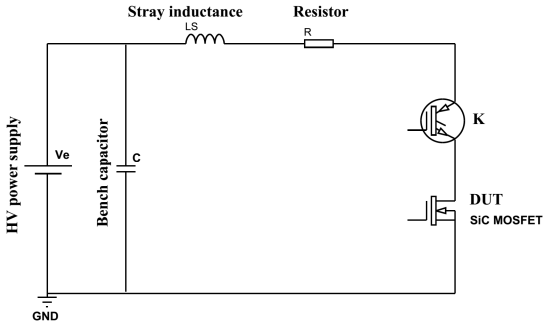


Fig. 1. Schematic of the avalanche test circuit.

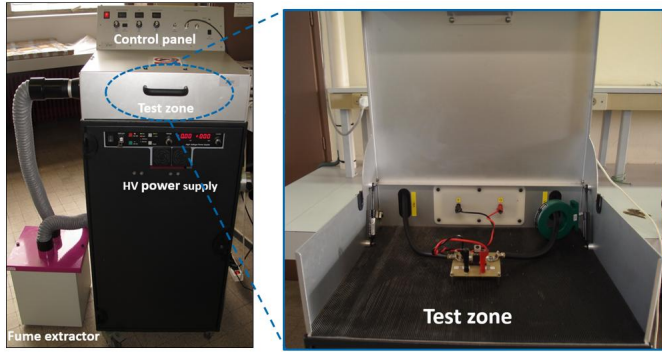


Fig. 2. Experimental setup.

### B. Test Protocol

Avalanche tests are carried out by applying a single pulse to the auxiliary IGBT “K”. In order to estimate the avalanche energy leading to device’s failure, the DC voltage is gradually increased from a low value where the device is able to sustain the avalanche conditions, up to the value producing the failure. Before failure, the device can sustain many voltage pulses. Once failed, the device is no longer able to block the full DC voltage. The avalanche energy leading to the device failure can be evaluate by calculating the time integral of the product of the drain-source voltage  $V_{DS}$  and the drain current  $I_{DS}$ , as shown in equation (1):

$$E_c = \int_{t_1}^{t_2} V_{DS}(t) \cdot I_{DS}(t) dt \quad (1)$$

In order to compare the results of robustness of the SiC MOSFETs, the critical energy density is calculated according to the following equation:

$$E_c^* = \left(\frac{1}{S_d}\right) \cdot E_c \quad (2)$$

Where  $S_d$  is the surface of the SiC die.

Fig. 3 presents the typical set of waveforms for a destructive single-pulse avalanche test:  $V_K$  is the gate signal applied to the IGBT (red);  $I_{DS}$  is the current in the SiC MOSFET (green) and  $V_{DS}$  is the voltage across the DUT (blue) and  $E$  refers to the amount of energy dissipated by the device during the avalanche time  $t_{av}$  (gold). As can be seen,  $V_{DS}$  is initially equal to ( $V_i \approx 0$ ) when the IGBT is off. Once the pulse is applied through the auxiliary IGBT “K” ( $t_1 \leq t \leq t_3$ ) and the DC voltage exceeds the breakdown voltage ( $V_{BR} < V_E$ ) of the MOSFET, an avalanche current flows. At this stage, the avalanche current is limited by the resistor ( $I = (V_E - V_{BR})/R$ ) to a few amperes. After failure of the device ( $t_2$  in Fig. 3), the voltage across the DUT collapses to almost zero, and the current increases dramatically to  $I = V_E/R$ . Briefly after the failure, the IGBT is turned-off, interrupting the current. During the entire sequence, the DUT is driven with a negative voltage (-8 V) to force it in the off-state.

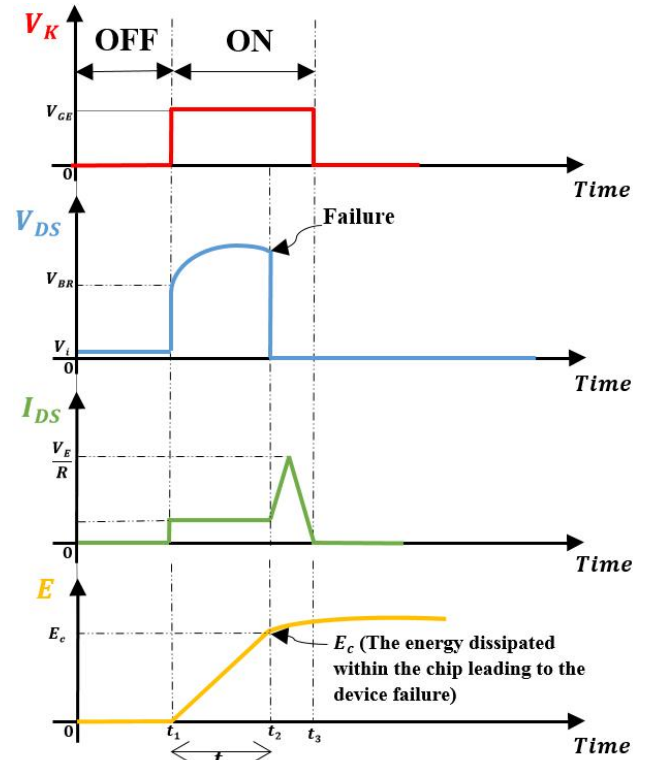


Fig. 3. Typical avalanche test waveforms.

### C. Failure analysis

To correlate the experimental results with the failure mechanism, SiC MOSFETs were decapsulated to examine the failure sites on the SiC dies. For that, we have used concentrated sulfuric and nitric acids. Using both acids simultaneously is a more efficient way to dissolve plastic molded components than using concentrated acids alone [8, 10]. The devices to be opened are placed in a beaker, on a hotplate at 200 °C, and a pipette is used to slowly drip the acids. After decapsulation, the samples were rinsed in acetone, and observed using an optical microscope (Zeiss Axio-Scope 1) and a scanning electron microscope (Tescan Mira 3).

### III. EXPERIMENTAL RESULTS

Avalanche experiments were conducted on several samples of each SiC Power MOSFETs listed in table I, at 25 °C. The results are shown in Fig.4, where the energy density threshold to failure (called critical energy density) is plotted as a function of the avalanche duration before failure ( $t_{av}$ ). In this figure, each point is the result of a destructive avalanche test on a given device. In order to compare the robustness of SiC MOSFETs, the critical power density (critical energy divided by the time before failure  $t_{av}$ ) is also given in Fig.5.

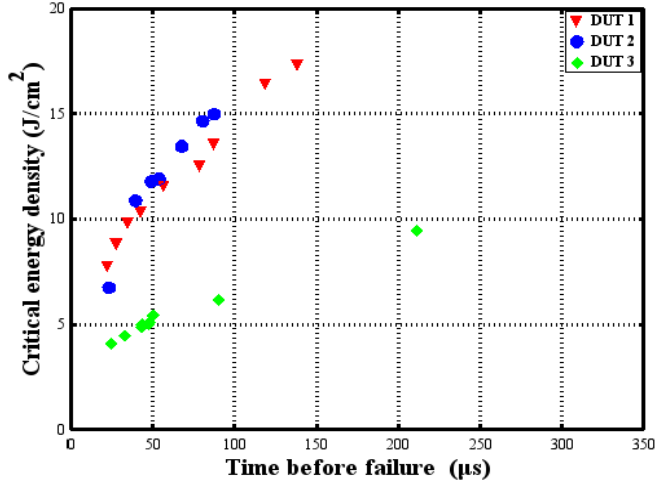


Fig. 4. Critical energy density as a function of the avalanche duration. Note that for DUT3, the energy density was calculated using the surface area of the MOSFET die only (for consistency with the other devices). The external diode is not considered in the calculation.

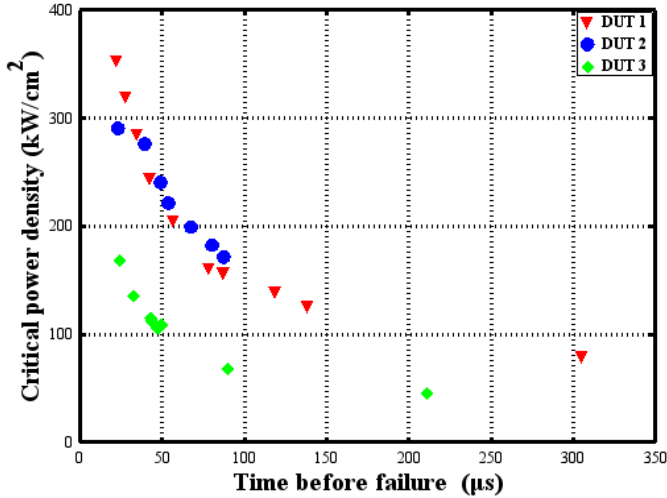


Fig. 5. Critical power density as a function of the avalanche duration.

Using the same dataset as in Fig.4, we analyzed the breakdown voltage of the SiC MOSFETs. Fig. 6 presents the distribution of breakdown voltages for DUT 1, 2 and 3 (the breakdown voltage is measured at the beginning of the avalanche pulse). For all tested devices, it appears that the actual breakdown is much higher than the rated voltage of the devices. Moreover, there is a relatively small scattering of the  $V_{BR}$  values between DUT 1 and 3. There is no significant relationship between  $V_{BR}$  and  $E_c$  for a given DUT.

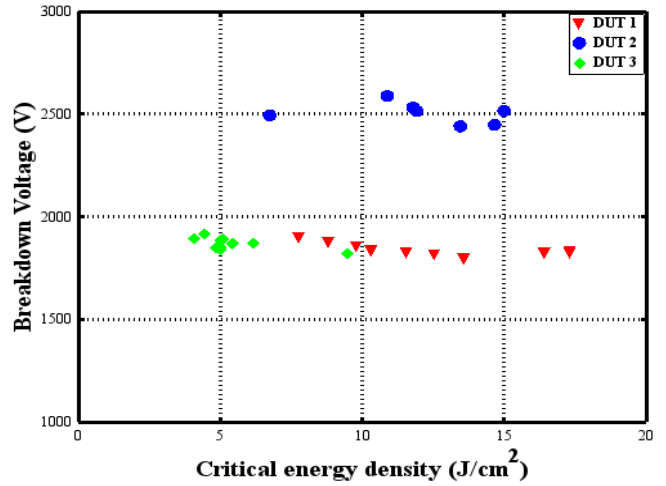


Fig. 6. Breakdown voltage as a function of the avalanche duration.

Fig. 7 and 8 show an example of waveforms measured on DUT 1 under destructive avalanche stress for  $T_{CASE} = 25$  °C. The dissipated energy leading to failure is about 1.01 J ( $E_c^* = 9.77$  J/cm<sup>2</sup>). From these figures, failure occurs on both gate and source pads, resulting in a short circuit between all three terminals of the device (Gate-Drain-Source). As shown in Fig.7, a sudden collapse in the voltage across the MOSFET is recorded at 34.4  $\mu$ s. The current increases dramatically to about 35 A after device failure. Fig. 8 shows that the gate oxide fails with a short circuit between gate and source (after avalanche,  $V_{GS}$  reaches 0 V).

The decapsulation of the device shows that high temperature was reached by the device during avalanche operation, as the source and gate metallization have melted, and the SiC underneath shows a clear change in structure. An example image is shown in Fig. 9. The decapsulated device shows a localized black spot where failure occurred. Other inspected dies for DUT 1 looked similar to that imaged in Fig. 9 (all the failures have led to current crowding in localized area resulting to molten SiC and metallization). The exact location, however, changed from die to die, indicating that there is no clear weak area.

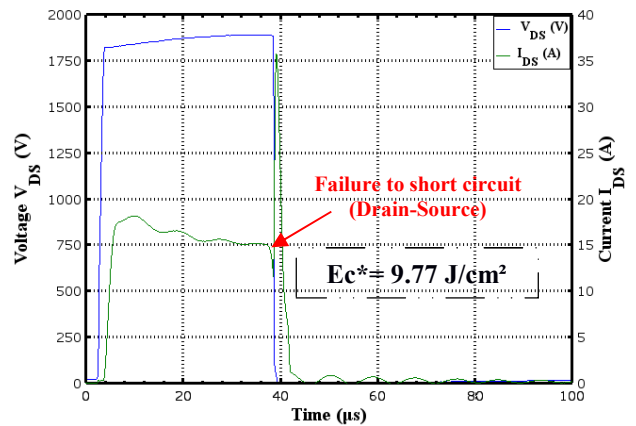


Fig. 7. Measured drain-source voltage and current across the DUT 1 under avalanche conditions.  $t_{av} = 34.4$   $\mu$ s;  $E_c = 1.01$  J;  $V_{BR} = 1854$  V.

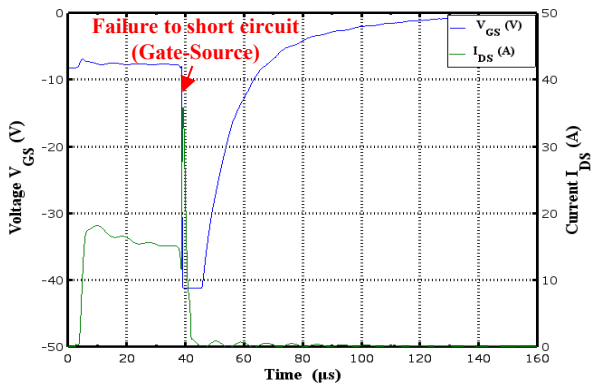


Fig. 8. Measured gate voltage and drain current across the DUT 1 under avalanche conditions.  $t_{av}=34.4 \mu s$ ;  $E_c=1.01 J$ ;  $V_{BR}=1854 V$ .

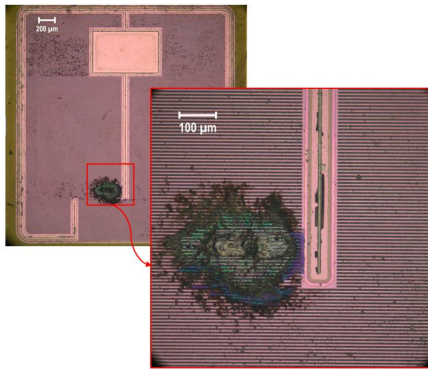


Fig. 9. Damaged SiC die for DUT 1 @  $t_{av}=34.4 \mu s$ ;  $E_c=1.01 J$ ;  $V_{BR}=1854 V$ .

Figure 10 shows the surface analysis of the damaged zone for DUT 1. A surface inspection allows us to see clearly the damage zone at the source metallization. The SEM observation proves that the avalanche is always localized in a small area of the die, resulting in very high temperature sufficient to create a crater in the SiC die. These crater seems to be the origin of the physical short circuit between the drain-source observed during the device failure.

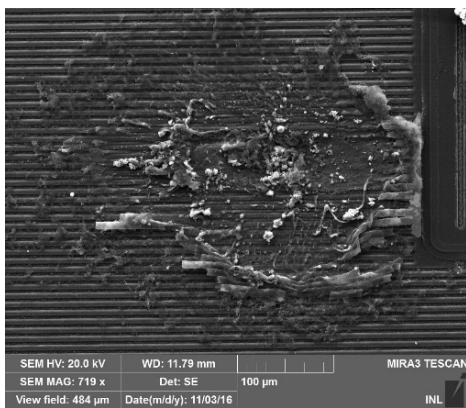


Fig. 10. SEM image of the damaged zone for DUT 1.

Further avalanche experiments have been conducted on the DUT 2. The first results on DUT 2 are plotted in Fig.11, where drain-source voltage and current are presented. For avalanche duration 23.4  $\mu s$ , failure appears with a short circuit between all three terminals of the device, similarly to failure of DUT 1. Figure 12 shows the microscopic picture of a decapsulated

device after avalanche failure at 2.17 J (6.73 J/cm<sup>2</sup>). It can be seen that the damage is located at the left edge of the source metallization.

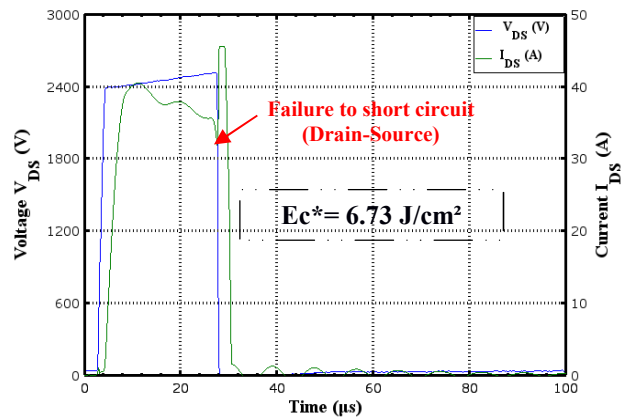


Fig. 11. Measured reverse voltage and current across the DUT 2 under avalanche conditions.  $t_{av}=23.4 \mu s$ ;  $E_c=2.17 J$ ;  $V_{BR}=2495 V$ .

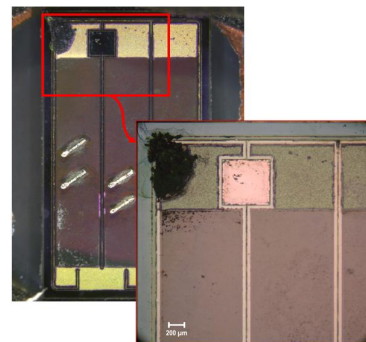


Fig. 12. Damaged of SiC die for DUT 2 @  $t_{av}=23.4 \mu s$ ;  $E_c=2.17 J$ ;  $V_{BR}=2495 V$ .

Fig. 13 shows similar results for another sample of DUT 2, measured for a longer avalanche pulse. It can be seen that for higher energy test, the outcome is quite the same: after the voltage collapses across the MOSFET, the current increases dramatically, resulting in a short circuit between all three terminals of the device. Figure 14 shows the location of the damage. Both cases shown in Fig.12 and 14 indicate the same failure mode for DUT 2. The failure sites occur at the source metallization and result in the collapse of the voltage across the DUT 2 (short-circuit failure mode).

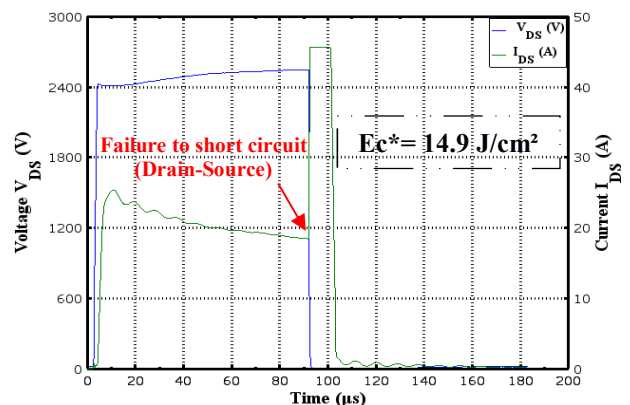


Fig. 13. Measured reverse voltage and current across the DUT 2 under avalanche conditions.  $t_{av}=87.4 \mu s$ ;  $E_c=4.492 J$ ;  $V_{BR}=2517 V$ .

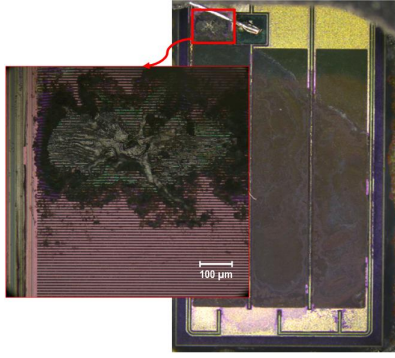


Fig. 14. Damaged SiC die for DUT 2 @  $t_{av}=87.4 \mu s$ ;  $E_c=4.492 J$ ;  $V_{BR}=2517 V$ .

Similar tests have been extended to DUT 3 (For these devices, the manufacturer packaged both a MOSFET and a diode in the same TO-247 case). Figure 15 reports waveforms of DUT 3 measured at ambient temperature (25 °C). The obtained results show that failure appears as a short circuit between the Drain-Source of the DUT 3. Examinations of device that have undergone catastrophic failure during avalanche tests show that failures occur on the edge of the external schottky diode. The failure results in the collapse of the voltage across the diode (short-circuit). Then, to a short circuit between the drain and source terminals of the case. Figure 16 shows such an example of damaged die for DUT 3. As it can be seen, a clear defect is located in the diode's periphery, near the edge of the device. The energy was concentrated in a single spot rather than distributed evenly over the surface of the die. In the other hand, no indication of damage has been observed in the SiC MOSFET die. This means that the failure of MOSFET was caused by the breakdown of the external diode's periphery during avalanche.

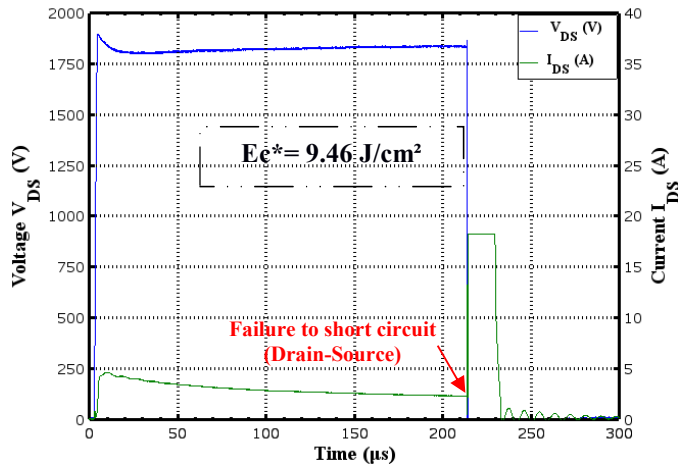


Fig. 15. Measured reverse voltage and current across the DUT 3 under avalanche conditions.  $t_{av}=211 \mu s$ ;  $E_c=1.13 J$ ;  $V_{BR}=1821 V$ .

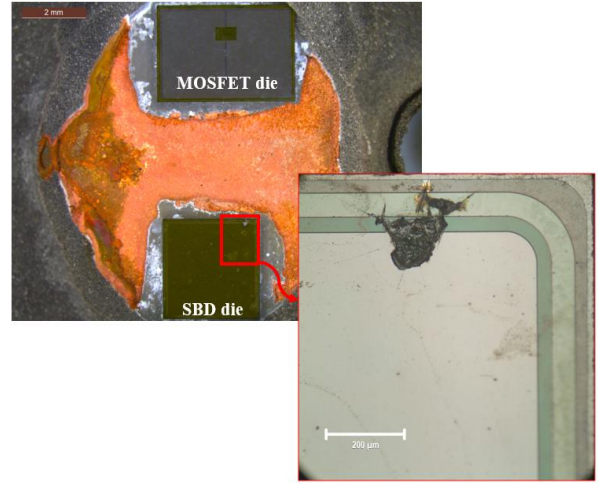


Fig. 16. Damaged SiC die for DUT 3 @  $t_{av}=211 \mu s$ ;  $E_c=1.13 J$ ;  $V_{BR}=1821 V$ .

#### IV. DISCUSSION

Single pulse avalanche ruggedness was evaluated for commercial SiC MOSFETs from two manufacturers (wolfspeed and RHOM). Each device was tested with increasing magnitude of avalanche energy up to the device's failure point. The results shown in Fig. 4-5 indicate that SiC MOSFETs from Cree (DUT 1 and 2) are relatively more robust to single pulse avalanche compared to MOSFETs from RHOM (DUT 3). The results in Fig. 4 show that the critical energy is not constant for a given device, but increases with the avalanche pulse duration. This seems to indicate that during avalanche, only a small area of the die is involved in the power dissipation. Decapsulation of failed devices are shown in Fig. (9-10-12-14-16) and confirm that the damage is indeed localized in a relatively small area. For Wolfspeed devices, the failures are localized at the source terminal of the SiC die (Fig 9-10-12-14). For RHOM device, shown in Fig. 16, the failure occurs at the edge of an external schottky diode.

Several internal device failure mechanisms may cause the collapse of the device voltage during avalanche, and eventually the catastrophic failure of these devices. According to the test results, the failures can be classified by failure location on power MOSFETs into two categories. First, for DUT 1 and 2, it has been found that two failure mechanisms may happen. One of the failure mechanisms is the activation of a parasitic BJT which is found in the MOSFET structure. As shown in Fig.17, a NPN parasitic bipolar transistor is formed among the N+ source ("emitter"), the P-body ("base"), and the N-type drain ("collector") [11]. In fact, when the P-N junction is in avalanche mode, a large avalanche current will flow and hole current will turn on the parasitic BJT [12]. Since the BJT will demonstrate a snapback negative resistance characteristic, this will lead to current crowding in localized areas and create a molten spot which lead to a short circuit between the Drain-Source of the MOSFET (short circuit failure mode). This failure mechanism is influenced by the parametric variability between the cells in the power MOSFET which cause non uniform current distribution and temperature surges in the device [13]. A second

failure mechanism is the intrinsic temperature limitation of the device. In fact, the device simply loses its voltage blocking capability if the intrinsic carrier concentrations approach those of the background doping concentration. The thermally generated carriers will generate an extremely high leakage current and lead to a sudden collapse in the voltage, current focusing then to device failure, similar to the case of parasitic BJT activation. However, the device failure may occur before exceeding the intrinsic temperature limit due to the lower melting point of the metallization [14]. In fact, during avalanche, high power dissipation in the DUT may lead to extremely elevated junction temperature which causes the metallization to melt (The melting temperature for aluminum is around 660°C).

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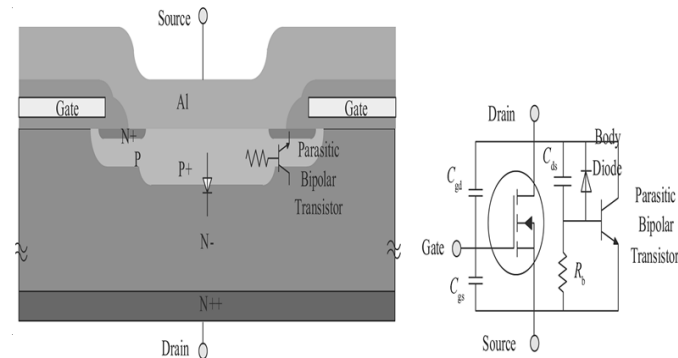


Fig. 17. Equivalent circuit of power MOSFET [13].

For DUT 3, it has been noticed that failures appear at lower energy. Examination of failed devices show that all failures occur on the edge of the external schottky diode where the electrical field intensity is greatest. The avalanche is localized at the corner of the external diode resulting to a short circuit between the drain and source terminals of the case. The avalanche test highlighted a weakness in the external diode, not in the MOSFET die itself. This means that for DUT3, our tests are inconclusive regarding the actual robustness of the MOSFET die in avalanche.

## V. CONCLUSION

This paper investigates the robustness of different commercial SiC MOSFETs in avalanche operation. The single pulse robustness test shows that the critical energy is relatively different from one device reference to another. The critical energy also depends strongly on the duration of the avalanche pulse. The experimental results have shown that DUT 1 and 2 are more robust than DUT 3. An analysis of various devices tested to destruction indicates that failure spots occur at the metallization sources for DUT 1 and 2. In the other hand, the breakdown of DUT 3 was to be found caused by the failure of an external SBD diode. The two common failure mechanisms for DUT 1 and 2, BJT latch-up and intrinsic temperature limit, were discussed. At this stage of our investigations, it is not clear yet which of these mechanisms is directly responsible for the device failures.

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