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Geoffroy Houin, Frederic Duez, Luc Garcia, Eugenio Cantatore, Fabrizio Torricelli, et al.. High performance low voltage organic field effect transistors on plastic substrate for amplifier circuits. Organic Field-Effect Transistors XV , Aug 2016, San Diego, CA, United States. pp.99430H, 10.1117/12.2238792 . hal-01534922

HAL Id: hal-01534922

<https://hal.science/hal-01534922>

Submitted on 8 Jun 2017

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High performance low voltage organic field effect transistors on plastic substrate for amplifier circuits

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ABSTRACT

The high performance air stable organic semiconductor small molecule dinaphtho[2,3-b:2',3'-f]thieno[3,2-b]thiophene (DNNT) was chosen as active layer for field effect transistors built to realize flexible amplifier circuits. Initial device on rigid Si/SiO₂ substrate showed appreciable performance with hysteresis-free characteristics. A number of approaches were applied to simplify the process, improve device performance and decrease the operating voltage: they include an oxide interfacial layer to decrease contact resistance; a polymer passivation layer to optimize semiconductor/dielectric interface and an anodized high-k oxide as dielectric layer for low voltage operation. The devices fabricated on plastic substrate yielded excellent electrical characteristics, showing mobility of 1.6 cm²/Vs, lack of hysteresis, operation below 5 V and on/off current ratio above 10⁵. An OFET model based on variable ranging hopping theory was used to extract the relevant parameters from the transfer and output characteristics, which enabled us to simulate our devices achieving reasonable agreement with the measurements

Keywords: organic field effect transistors, plastic substrate, parameter extraction, flexible amplifier

1. INTRODUCTION

Enormous research efforts over the last decade on organic semiconductors have led to impressive achievements in various devices which apply them as active materials. This has mainly been driven by coordinated developments in chemical and device engineering. Organic light emitting diodes (OLED) are already in the market. Organic photovoltaics (OPV) and organic field effect transistors (OFET) are starting to emerge as commercial products. It can be envisaged that low cost, flexible and large area devices made with these materials^[1-3] will soon enable new electronic applications.

Enabling the switching function, the field effect transistor (FET) is the single most important component in electronic circuits. OFETs have already shown better performances than that of the amorphous silicon, with the prospective to replace thin film transistors in active matrix displays. Several different types of circuits using OFETs have been proposed; among them were high gain inverters and MHz operation ring oscillators^[4]. One of the major issues in the application of organic semiconductors is their operational stability, limiting their performance under ambient condition. A major breakthrough was achieved with the invention of dinaphtho[2,3-b:2',3'-f]thieno[3,2-b]thiophene (DNNT)^[5,6] (chemical structure is shown in Figure 1), which showed not only high performance, but also excellent air stability. Another issue is the operational voltage of OFETs. Oxygen plasma of Al gate together with self-assembled monolayer (SAM)^[7] treatment of the surface yielded dielectric with very high capacitance, which allowed DNNT based OFETs operate at low voltage. However, simplification of the fabrication processes is necessary for large scale production of these devices.

In this paper, we report our approach to realize high performance, low voltage DNNT-based OFETs with special focus on process simplification. In this regard, we replaced oxygen plasma for the growth of Al₂O₃ with anodization, and SAM treatment with a polymer layer. We also applied oxide interfacial layer to reduce the contact resistance between the active layer and the electrode. These processes were carried out on plastic substrate, resulting in flexible OFETs operating below 5 V, current on/off ratio above 10⁵ and mobility of 1.6 cm²/Vs. The hysteresis-free characteristics of these devices allowed us to further exploit their applicability in amplifier circuits. We present device modeling for the

extraction of relevant parameters. Simulated transfer and output characteristics obtained in the commercial CAD environment Virtuoso[®] were compared to experimental data obtaining good modeling accuracy. This allowed us to design an amplifier circuit using our OFET devices and passive components such as resistors and capacitors, a work which is still in progress.

2. OFET DEVICE ENGINEERING

2.1 Silicon gate-based OFETs

Our initial OFET, which served as the reference device, was fabricated on a Si substrate. Here below we describe the details of the fabrication process and the measured device performance.

2.1.1 Fabrication process

Highly n-doped silicon substrate with thermally grown SiO₂ (200 nm) was used as gate and dielectric in a bottom gate, top contact structure, as is shown in Figure 1. Surface treatment of the SiO₂ was carried out using poly(1-vinyl-1,2,4-triazole (PVT) (see Figure 1 for chemical structure) from a solution in water (3mg/mL)^[8]. PVT was deposited by spin-coating and then dried in vacuum at 80°C for two hours forming about 15 nm of passivation layer. 30 nm of DNNT p-type semiconducting layer was evaporated thermally at slow rate 0.1 Å/s under vacuum. We used gold as source/drain contact material. Gold was evaporated thermally through shadow mask to create a device with a channel length (L) of 100 μm and a channel width (W) of 1mm.

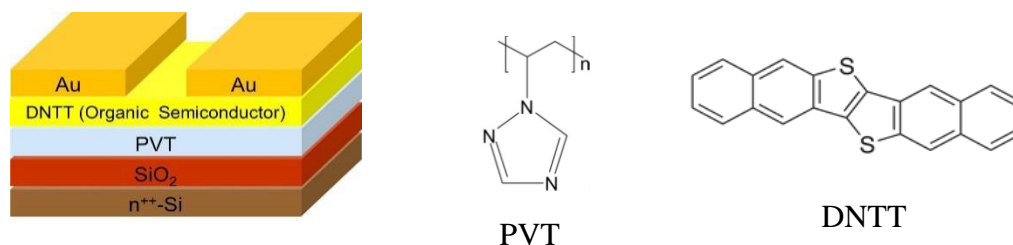


Figure 1. OFET architecture on Silicon substrate and molecular structure of PVT and DNNT.

2.1.2 Results and discussions

The electrical characteristics of a typical device are presented in Figure 2 a) and b). The transfer curve in saturation regime ($V_{DS} = -30$ V) showed no hysteresis, thanks to the effective passivation of the oxide surface by PVT, which minimized interfacial trap densities. The steep subthreshold slope of around 0.2 V/decade, even with low total gate capacitance (14.7 nF/cm²), was also demonstrating the excellent dielectric/active layer interface. The on/off current ratio is higher than 10⁶ and a low threshold voltage of around -3 V was obtained. The maximum saturation mobility μ_{sat} derived from gate voltage dependant mobility measurements is around 0.4 cm²/Vs. Well defined linear and saturation behaviours are evident from the output curves. Despite of these excellent device performances, further improvements can be envisaged. The mobility of the device can be improved enhancing the charge injection from the source contact to the semiconductor layer, as well as by better charge transport at the interface between the dielectric and active layer. Operating voltages can be significantly decreased by applying high k dielectrics. With these strategies in mind, we developed low voltage, high performance OFET devices on plastic substrate, which will be described in the next section.

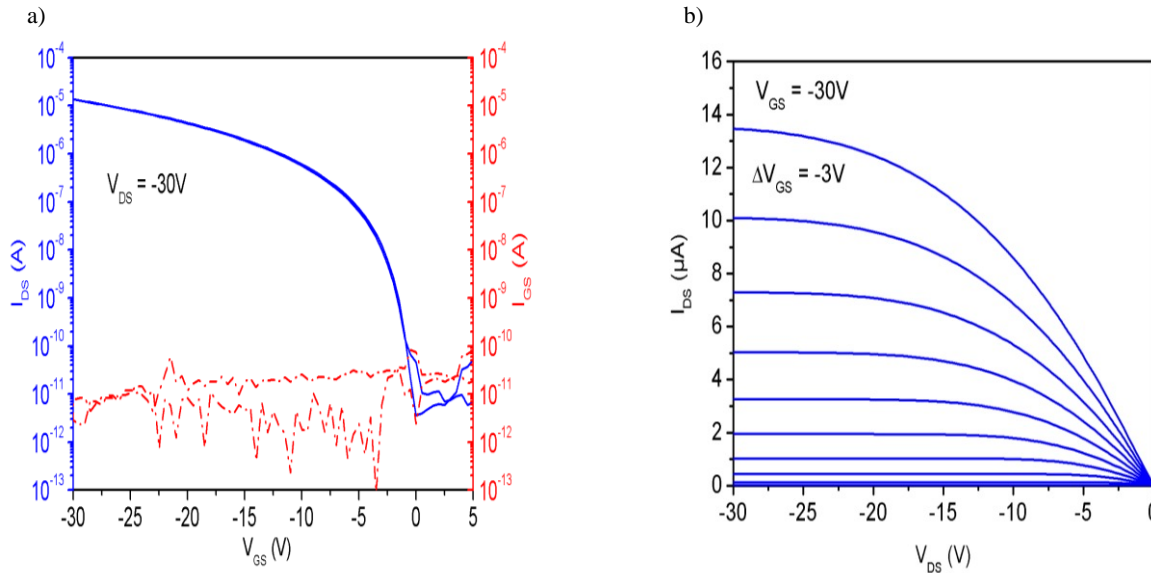


Figure 2. a) Transfer characteristics of reference OFET in saturation regime; b) corresponding output characteristics.

2.2 OFETs on plastic substrates

In each optimization step, the device on Si substrate served as reference. Firstly, an oxide interfacial layer was included in order to decrease the contact resistance between the charge injecting/extracting electrodes and the active semiconductor layer. Secondly, Polystyrene replaced PVT as the passivation layer on the gate insulator, due to its lower dielectric constant and the consequent reduction of interfacial dipoles which is detrimental to charge transport. Anodization of Al was chosen as simple step to grow high-k dielectric and obtain an high gate capacitance, which leads to low operating voltages. All processing was carried out on a plastic substrate, as will be described in detail below.

2.2.1 Fabrication process

Standard PEN foil (thickness of $50\mu m$) was selected as substrate. Polydimethylsiloxane (PDMS) thick films were used to facilitate the process (as support for evaporation and spin-coating). We applied surface annealing of PEN to smoothen its surface. 100 nm thick aluminum gate was evaporated under vacuum with an e-Beam evaporator. Aluminum oxide was formed by anodization using electrochemistry. A constant current was applied between the Al gate and platinum counter electrode in citric acid solution. Oxide thickness was controlled by increasing the voltage. The oxide layer thickness was estimated to be 30 nm. Polystyrene in a solution of chlorobenzene (3mg/mL) was chosen as surface treatment polymer to replace PVT, spin coated on the Al_2O_3 surface and dried in oven at $80^\circ C$ for two hours. 30 nm of DNTT was evaporated thermally at a slow rate under vacuum. A WO_3 (10nm) /Au combination for the contact material was thermally evaporated through a specifically designed shadow mask with $L = 50 \mu m$ and $W = 500 \mu m$. The final device structure is presented in Figure 3.

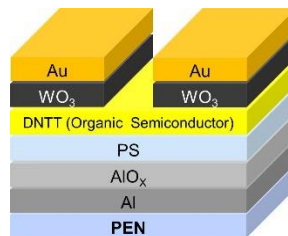


Figure 3. Optimized OFETs architecture on PEN substrate

2.2.2 Results and discussions

The transfer and output characteristics of a typical device on plastic foil operating below 5 V are shown in Figure 4 a) and b). The maximum value of the gate voltage dependent mobility reached 1.6 cm²/Vs. The on/off current ratio is higher than 10⁵. The devices did not show any hysteresis, which is a basic requirement for circuit design.

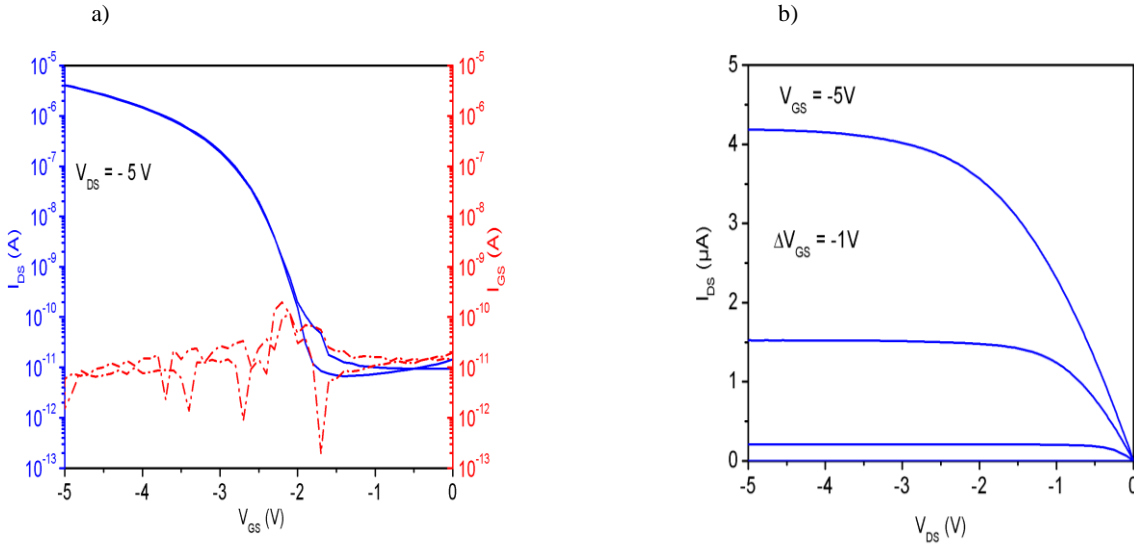


Figure 4. a) Transfer characteristics of optimized OFET in saturation regime on plastic substrate; b) corresponding output characteristics

The enhancement of device mobility from 0.4 cm²/Vs on Si substrate to 1.6 cm²/Vs on plastic substrates can be attributed mainly to two factors. One is the role of WO₃ as the interfacial layer for efficient charge injection from the electrode to the active layer, which effectively reduces the contact resistance. Detailed discussions on the different oxide and metal combinations, energy level alignment and quantitative contact resistance analysis are going to be described in a separate publication. Another factor is the application of polystyrene (PS) as a passivation layer. Here the low dielectric constant of PS ($\epsilon \sim 2-3$) has weaker dipole at the interface comparing to PVT ($\epsilon \sim 5-6$), which is beneficial for charge transport^[9]. Such an excellent performance allowed us to take next step towards amplifier circuit design.

3. MODELING

3.1 Transistor model

Several models were developed for a p-channel OFET^[10,11]. We based all our simulations on the model developed by D. Raiteri et al.^[12]. It applies Variable Range Hopping^[13] theory for organic semiconductors. Note that this model is using a bottom and a top gate. It has been demonstrated that the drain-source current (I_{DS}) in an organic semiconductor can be expressed as follows:

$$I_{DS} = \frac{W}{L} \beta [V_{OD,S}^{\gamma} - V_{OD,D}^{\gamma}] \left(1 + \frac{V_{DS}}{E_p L}\right) + \frac{W}{L} \frac{V_{DS}}{R'_{sub}} \quad (1)$$

$$V_{OD,X} = V_{SS} \ln \left[1 + \exp \left(\frac{V_G - V_X - V_{FB} + \eta(V_G - V_S)}{V_{SS}} \right) \right] \quad (2)$$

Where W is the channel width, L is the channel length, β is the current prefactor depending on all the electrical parameters characterizing the transport, including the insulator capacitance per unit area between the semiconductor and

the gate, and γ is the traps coefficient depending on the working temperature of the transistor and the characteristic temperature related to the disorder of the system. $V_{OD,X}$ is the overdrive voltage for the drain or the source, E_p is the pinch-off field depending on the early voltage V_p . R'_{sub} is the bulk resistance directly linked to the off current, V_{SS} is the sub-threshold slope, V_{FB} is the flat-band voltage that accounts for the charge neutrality in the metal-insulator organic-semiconductor structure. Finally η is the top-gate coupling to which we will give a value of 0, because our TFTs do not have a top-gate.

3.2 Parameter extraction

Simulation of OFET is necessary to predict the behavior of the final circuit structure^[14]. To achieve this, an extraction of the parameters corresponding to our OFET device is needed.

Equations (1) and (2) give us 7 parameters, collected in Table 1, to be extract from transfer and output characteristics of the OFET.

The easiest parameter to obtain is the early voltage V_p that can be extrapolated from the output curve, taking the slope for a low bias of V_{GS} around the highest V_{DS} . Then we normalized this value to the channel length and we obtained the equivalent pinch-off electric field E_p .

Two functions can be used to determine the other coefficients from the transfer curves:

$$w = \frac{\int I_{DS} dV_{GS}}{I_{DS}} \quad (3)$$

$$z = \frac{\int I_{DS}^2 dV_{GS}}{I_{DS}} \quad (4)$$

In saturation regime, we can write that:

$$w_{sat} = \frac{V_{GS}}{\gamma + 1} + \frac{V_T}{\gamma + 1} \quad (5)$$

$$z_{sat} = \frac{W}{L} \frac{\beta}{\gamma + 1} (V_{GS} - V_T)^{\gamma + 1} \quad (6)$$

Approximating equation (5) with a straight line $\gamma = mV_{GS} + q$, we can immediately derive:

$$\gamma = \frac{1}{m} - 1 \quad (7)$$

$$V_T = -\frac{q}{m} \quad (8)$$

In a similar way, we can derive β from equation (6). The subthreshold voltage V_{SS} can be extracted from the transfer curve in saturation regime evaluating the slope m' in the subthreshold region as indicated in equation (9):

$$V_{SS} = \frac{\gamma \text{Log}(e)}{m'} \quad (9)$$

Finally, equation (10) and (11) allow us to extract V_{FB} and R'_{sub} .

$$V_{FB} = V_T + \eta(V_{TG} - V_S) \quad (10)$$

$$R'_{sub} = \frac{L V_{DS}}{W I_{off}} \quad (11)$$

Equation (10) in our case can be rewritten as $V_{FB} = V_T$, because we don't have top gate. All seven extracted parameters are compiled in Table 1, which will be used for simulation in the following section.

Table 1. Model parameters extracted from our device characteristics

	Symbol	Extracted Value	Tuned Value	Unit
Current prefactor	β	3×10^{-6}	1.1×10^{-7}	[A/V ^γ]
Traps coefficient	γ	2	2.2	[K/K]
Sub-threshold slope	V_{SS}	0.03	0.18	[V]
Flat-band voltage	V_{FB}	- 2.3	-2.3	[V]
Bulk resistance	R'_{sub}	6×10^{10}	6×10^{11}	[Ω]
Pinch-off field	E_p	1×10^5	1×10^5	[V/cm]
Top-gate coupling	η	/	/	[μm/μm]

4. SIMULATION

We use CADENCE Virtuoso[®] to run a simulation of our OFET characteristics. Then we compared them to our devices measurements.

Using a classical scheme to test our device in simulation (I_{DS} as function of V_{GS} , Figure 5 a) and I_{DS} as function of V_{DS} figure 6 a)), we observed that the model fitted well with the parameters that we extracted. However, the fitting could be further improved. We studied the influence of each parameter on transfer and output curves to find the optimal values for all seven parameters.

Figure 7 shows the way to proceed to tune the parameters to fit the best model with the experimental data.

Table 1 gathered all the new optimized values for the model parameters.

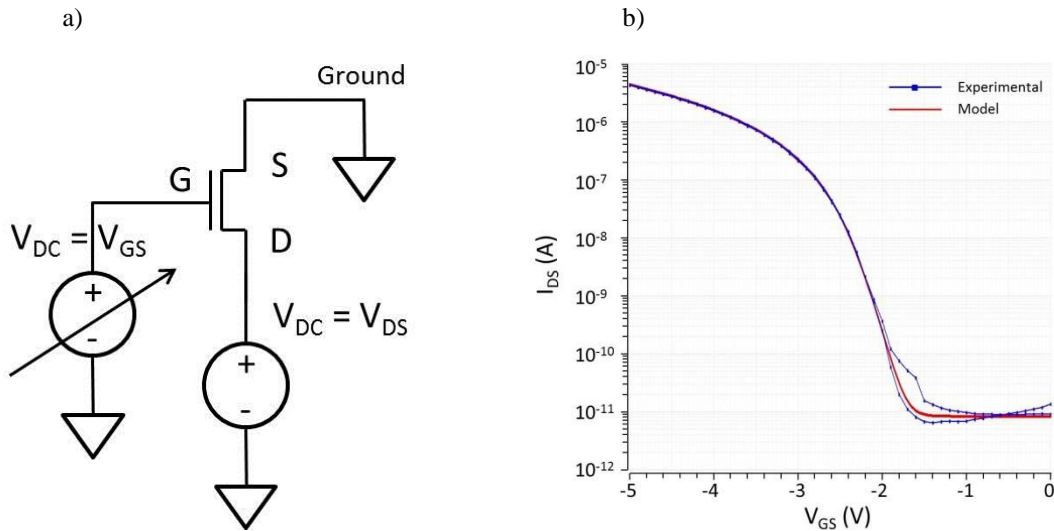


Figure 5. a) device operation scheme; b) Fitting of the model to the experimental transfer curve using optimally tuned values

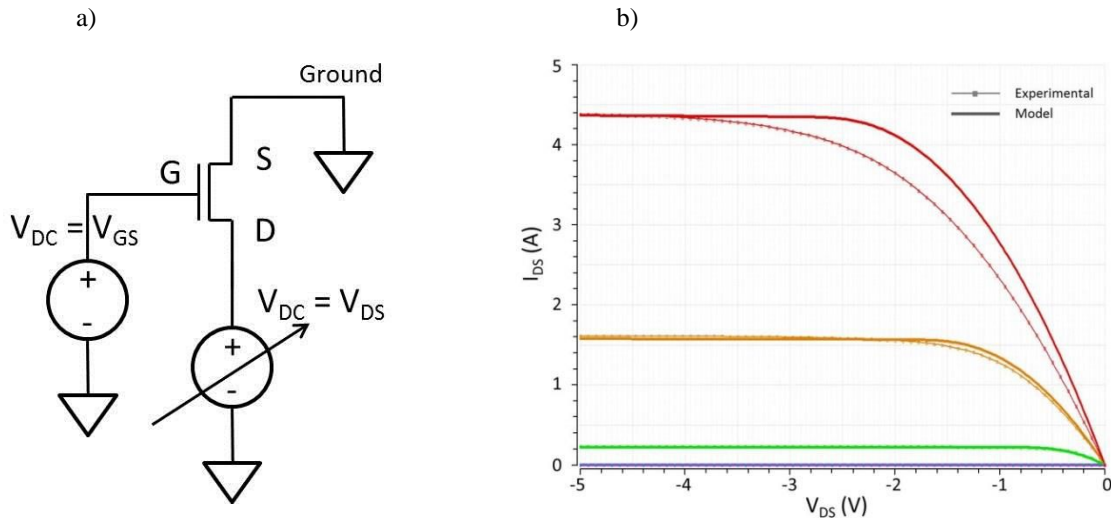


Figure 6. a) device operation scheme; b) Fitting of the model to the experiment output curves using optimally tuned values

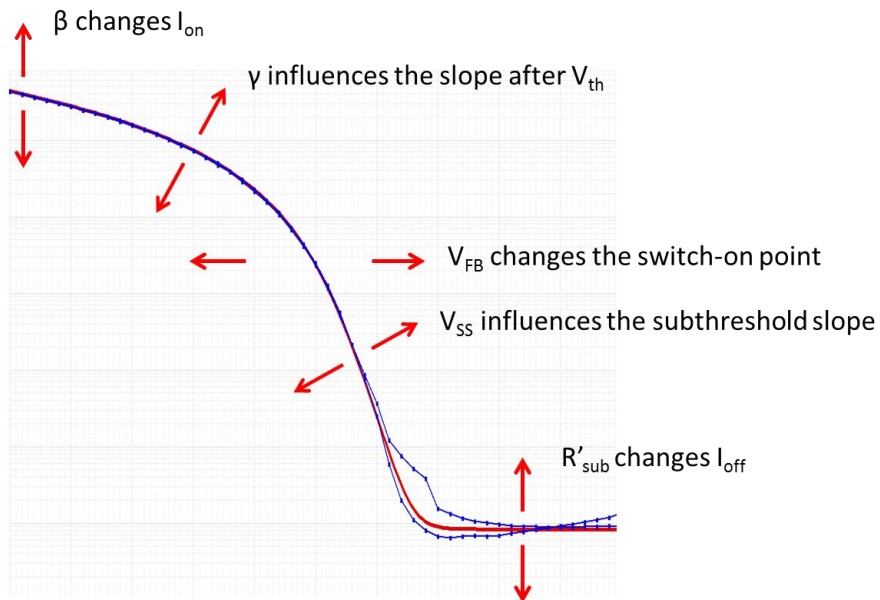


Figure 7. Optimization possibilities to get the best fitting between experimental and simulations

We focus on the transfer curve to tune the parameter values, but we also observed some influences on the output curves: E_p has a mild influence on the slope in saturation (remind that our OFETs are long); β changes the separation of the curves for different gate voltages, γ increases or decreases the maximum drain current; V_{SS} helps to increase the maximum current; R'_{sub} has no relevant influence. At last, when V_{FB} decreases, I_{DS} also decreases.

This allowed us to design an amplifier circuit composed of our OFETs and passive components such as resistor and capacitor. Work is in progress towards manufacturing such an amplifier on plastic substrate.

5. CONCLUSION AND PERSPECTIVES

In this work, we presented our approach to fabricate high performance OFET devices on plastic substrate, which are used to realize a flexible amplifier. Air-stable organic semiconductor small molecule DNNT acted as active layer. We first fabricated our device on rigid Si/SiO₂ substrate as control device, then used a number of approaches to improve device performance on a plastic substrate. Our focus has been on simplifying fabrication process. Solution processing anodization was used to grow high k dielectric Al₂O₃ with controllable thickness. Simple spin coating of a polymer was applied to passivate the oxide surface. With low dielectric constant, polystyrene proved to yield the best performance. We also observed that application of an oxide interfacial layer (WO₃) decrease the contact resistance between the electrode and the semiconductor layer. All these attempts resulted in a device fabricated on plastic substrate with excellent electrical characteristics showing mobility of 1.6 cm²/Vs, lack of hysteresis, and current on/off ratio above 10⁵, while operating below 5V. An OFET model was used to extract the relevant parameters from transfer and output characteristics of our device, which enabled us to simulate the OFET and compare the results with experimental measurements, achieving good agreement. Based on these parameters, an amplifier circuit was designed consisting of our p-type OFET and passive components such as resistances and capacitors. Work is in progress to optimize these passive components and include them in the amplifier together with our newly developed OFET.

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