Present and future of I/O-buffer behavioral macromodels

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Abstract. Modern Signal and Power Integrity (SI/PI) verification flows rely on accurate models for complex I/O-buffers that drive and receive electrical signals on high-speed channels. The sheer density of modern integrated circuits makes detailed transistor-level descriptions computationally cumbersome to the point where they become unusable for system-level simulations. Fortunately, transistor-level descriptions may be replaced with more compact representations that approximate the input/output buffers behavior with considerable accuracy while providing a simulation speedup of several orders of magnitude. Known as behavioral models, surrogate models or macromodels, these computationally efficient equivalents have become a de-facto industry standard in SI/PI simulations. This paper presents an overview of the state-of-the-art in I/O-buffer behavioral modeling, introducing the main features of both standard and emerging solutions. Open issues and future research directions are also discussed.

I. Introduction

Data throughputs at all levels across computational platforms have been continuously and rapidly increasing over the last years. Wired communication interfaces have considerably improved: boundaries of transmission data-rates have been pushed forth, pin-count has been minimized and systems, as a whole, has become less power-hungry. This is particularly true in mobile devices such as cell-phones, smart-phones, tablets, wearables, Internet of Things (IoT) and many other consumer products that benefit from recent, highly specialized protocols designed for high power efficiency and reduced Electromagnetic interference (EMI). Mobile terminals are complex environments, confined to miniaturized volumes and subject to extreme versatility: bit-rates and voltage levels adapt according to target applications, sending large amount of data across intricate and dense interconnects that link key parts of a mobile device (e.g., memory, display, battery, RF-transceivers and several other specialized chips). Whereas system users obviously benefit from such a broad offer of features, system designers are challenged to face and solve complex signal and power integrity problems [1, 2].

Indeed designing state-of-the-art, highly integrated systems such as multi-layer printed circuit boards (PCB), systems-in-package (SiP) or systems-on-chip (SoC) requires in-depth analysis of system reliability. This is only possible thanks to accurate and sophisticated software simulation tools, able to account for signal distortion in non-ideal interconnects, crosstalk, power-supply fluctuations and other similar phenomena. However, the feasibility of these simulations heavily depends on a new type of expertise: macro-modeling [3]. The sheer complexity of the systems makes transistor-level netlists cumbersome. The alternative consists in using compact and accurate surrogate models, built for computational speed and that mathematically mimic devices input-output responses. With simulation becoming less time consuming, the design flow is streamlined and system-level verification coverage can be extended to more complex analysis. However, as designers strive to meet the ever higher market expectations, the task of creating behavioral models has become a real great challenge; models need to be outstandingly accurate to account for multi-Gbps data-rates, continuous reduction of signal amplitudes, impact of supply-voltage variations and bouncing, dynamic supply-current, and many other aspects that the simulations necessarily need to study and verify.
This overview article focuses on an unambiguous discussion on the state-of-the-art modeling solutions for integrated circuit (IC) I/O-buffers, providing a summary of the inherent features and possible limitations of the various modeling approaches. An example test-case involving the signal integrity/power integrity (SI/PI) co-simulation of a memory interface for mobile applications is presented to highlight the benefits of I/O-buffer macromodeling in real design scenarios. Final remarks and additional thoughts on the evolution of behavioral modeling in the near future conclude this paper.

II. I/O-Buffer macromodeling concept

The top panel of Fig. 1 shows the typical structure of a single-ended output buffer that interfaces the internal IC core with the external interconnects. A macromodel of this device is defined as *any* set of nonlinear dynamic relations that reproduce the behavior of output- and supply-port currents as a function of the port voltages. Similar relations maybe established for input drivers or differential devices.

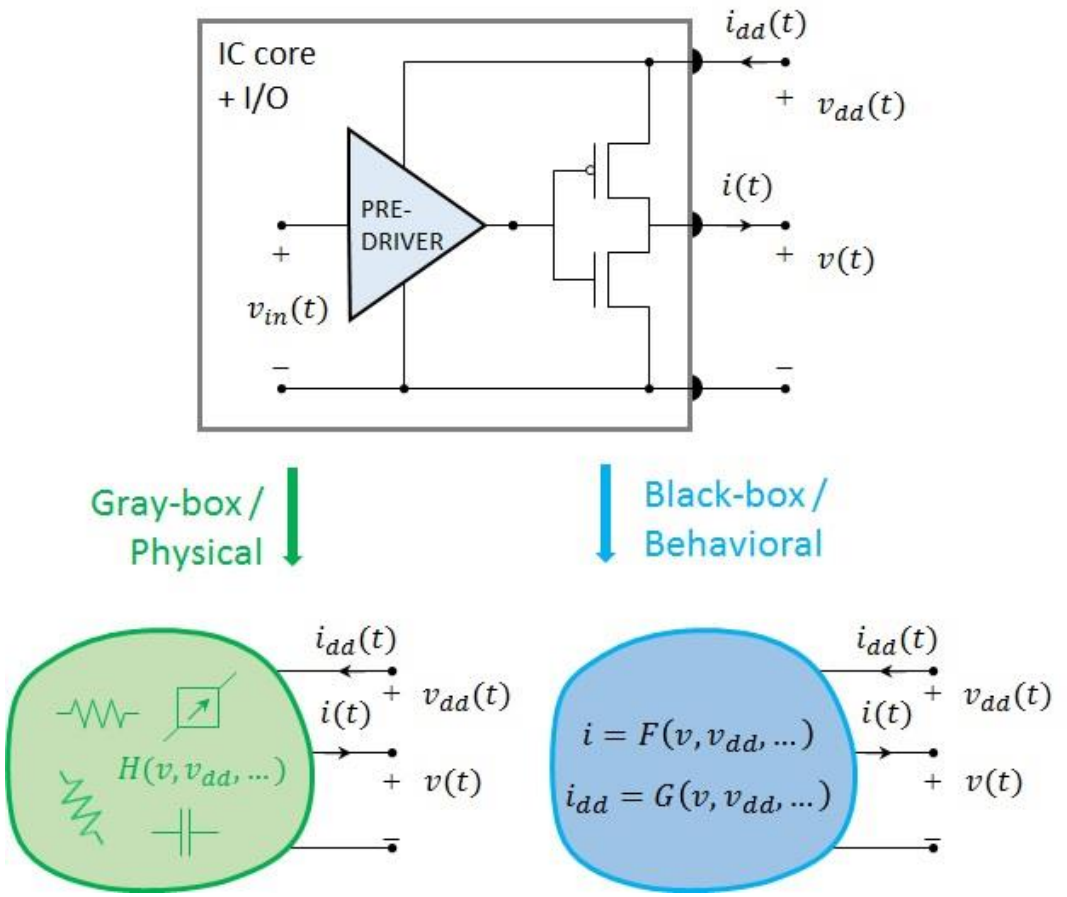

Figure 1: Typical structure of single-ended output-buffer with its relevant electrical variables (top-panel), illustration of the two main macromodeling strategies (bottom-panel).

The challenge that researchers face is to produce a nonlinear dynamic relation that is simultaneously accurate, computationally efficient and easy to implement on mainstream circuit simulators. Two main strategies seem to emerge: a bottom-up approach which aims to design simple equivalent circuits inspired by the internal physics of the device, and a top-down approach seeking to identify an optimal set of parameters for a well-chosen mathematical black-box surrogate. Even though making a comprehensive classification is never an easy task, state-of-the-art solutions available in literature [4-18] do appear to follow either one of these two strategies or rely on the combination of both in an attempt to improve accuracy while keeping parameter estimation procedures simple and robust.

III. IBIS summary and features

In the general framework highlighted above, the Input/Output Buffer Information Specification (IBIS) [3, 4] stands out as the mainstream approach for I/O buffer modeling. Intel Corporation started the development of IBIS in the early 1990s. Few years later, the IBIS Open Forum was created (https://ibis.org/) with the support and contributions from companies, users and academia. The Forum acts as an idea factory, develops and maintains useful documentation and tools, and

continuously works on updating the specification collecting suggestions and improvements via the Buffer Issue Resolution Documents (BIRD). IBIS has now arrived at version 6.1 and is continuously evolving.
IBIS relies on simplified circuit equivalents of typical buffer structures and provides detailed guidelines for the collection of relevant device features via a ready-to-use extraction procedure (e.g., the static characteristics of the output port current, the equivalent capacitance of the silicon die, etc.). IBIS specification has been massively used for generating buffer models in the recent years and it has been continuously updated with additional features and enhancements, becoming a de-facto standard.

Nonetheless, the need for increased accuracy, at least in some specific applications, has encouraged the development of modeling solutions outside the IBIS standard [5-18]. These complementary approaches mostly seek to better account for the dynamic dependence of I/O and supply port voltages on the circuit behavior and a better description of the power supply port current.

As briefly outlined above, rather than directly providing an equivalent circuit description, the IBIS standard [4] suggests a list of characteristics that need to be reported into a structured data file as the one sketched in Fig. 2. The header lists the key elements identifying the IBIS file and the associated device (the latter being a generic digital IC with, possibly, a large number of I/O pins). The specification assumes that each device pin is connected to a corresponding I/O buffer on the silicon die by a lumped RLC electric equivalent of the package. Also, all the parameters are defined by their typical, minimum and maximum values to accommodate for the uncertainties in the fabrication process and variability of operating parameters (temperature and supply-voltage). The silicon data section is the most important one and contains the data sets that describe the behavior of each IC port. For each silicon port, a model or a set of IBIS models are reported in the IBIS file. A complete description of IBIS keywords and features is beyond the scope of this article: readers should refer to dedicated resources such as [3, 4] for the details.

```
                Header section
[IBIS ver]      6.1
[File name]     myIC.ibs
[Date]          01/04/2016
…
|
[Disclaimer]    …
[Component]     xyz
[Manufacturer]  …
[Package]
|            typ     min     max
R_pkg        0.02    0.01    0.03
L_pkg        1.5nH   1.0nH   2.0nH
C_pkg        0.5pF   0.4pF   0.6pF
|
                Pin-map section

|
[Pin]  signal_name   model_name …
|
1      A1            buffer1
2      A2            buffer2
…
100    GND           Ground
|
              Silicon data section

|
[Model]      buffer1
Model_type   Output
Polarity     Non-Inverting
Enable       Active-Low
|

     Data of buffer1, keywords: [C_comp],
   [Pulldown], [Pullup], [Rising Waveform],
             [Falling Waveform], …

|
[end]
```

Figure 2: Example IBIS file.

In the following section the discussion refers to a single-ended output buffer. The IBIS philosophy is based on the observation that such device either operates in a fixed logic-state (*high* or *low*) or transitions across logic states (*low-to-high* or *high-to-low*). The behavior in fixed low or high input logic-state is described, respectively, by pull-up and pull-down components (represented by the pMOS and nMOS transistors in Fig. 1), suitably modeled as voltage-controlled current-sources defined by lookup tables. Their dynamical effects are modeled with a simple capacitor (i.e., the so called C_{comp} capacitor in the standard). During logic-state transitions, the output current can be written as a time-dependent linear combination of the pull-up and pull-down components, suitably weighted with time-depended coefficients to mimic the behavior of the pre-driver stage.

The resulting IBIS model structure may be mathematically written as:

$$i(t) = k_{PU}(t) I_{PU}\big(v(t)\big) + k_{PD}(t) I_{PD}\big(v(t)\big) - C_{COMP}\, \partial v(t)/\partial t \qquad (1)$$

where I_{PU} and I_{PD} are the pull-up and the pull-down static voltage-current characteristics, respectively and K_{PU} and K_{PD} are step-like weighting functions that can be computed form pre-recorded voltage responses observed on lumped resistive loads (e.g., a 50 Ω resistor) and simply embedded in the SPICE model as

voltage-time tables. Figure 3 shows the corresponding equivalent electrical circuit.

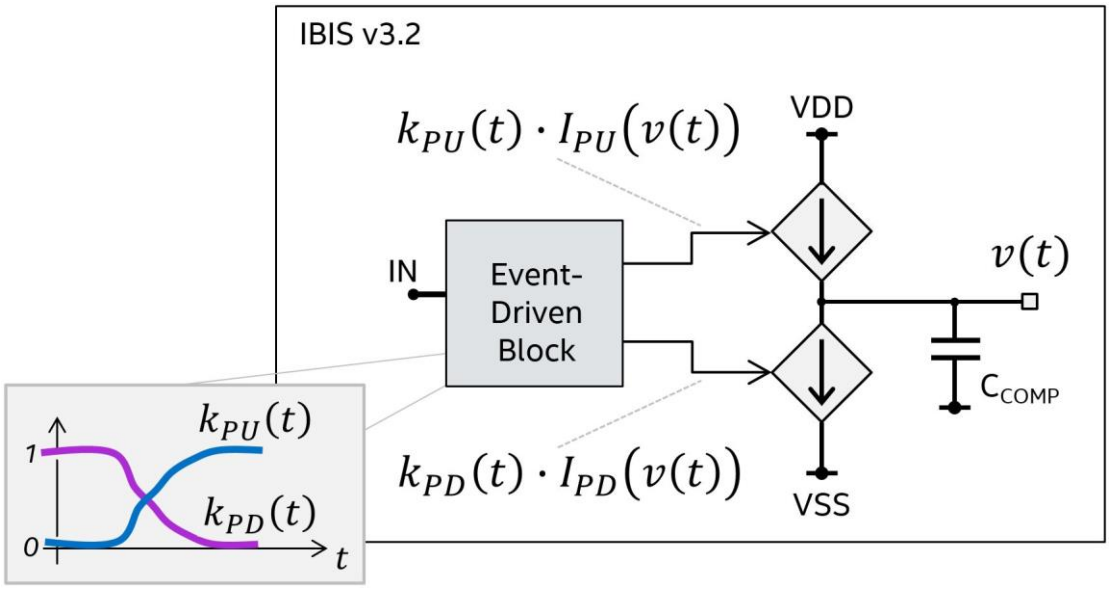

Figure 3: IBIS v3.2 Equivalent Electrical Circuit.

Each component of (1) can be computed from the responses of the device-under-modeling to specific stimuli and test-benches. Specifically, static characteristics are extracted from .DC sweeps, C_{comp} can be calculated with an .AC analysis and transient simulations are performed to collect voltage-time couplets on specific fixture loads.

Several modern high-speed I/O buffers, especially the ones used in memory links, are particularly sensitive to power-supply noise. Because of this, detrimental effects like jitter and signal distortions can dangerously affect system performance. Supply-voltage ripples originate in the interaction of power delivery network parasitics with the dynamic supply-currents related to I/O-buffer switching events. Hence, macromodels should accurately reproduce supply-current profiles and dependency of supply-voltage variations on output characteristics.

In this perspective, the IBIS v3.2 model structure shows an intrinsic limitation, approximating the supply-current with the pull-up static current only (i.e., $K_{PU}(t) \cdot I_{PU}(v(t))$ in (1)). In order to extend accuracy to the power supply port starting from version 5.0, IBIS model structure has been significantly enriched. Two additional sections have been introduced in IBIS files. The [SSO_PU/PD] section contains tables which account for the impact of static supply- and ground-voltage variations on the strength of pull-up and pull-down characteristics. The [Composite Current] tables collect the supply-current profile as it occurs during state transitions, and are used to extrapolate pre-driver and other current contributions that flow through the power-supply port but don't reach the output.

Despite the aforementioned countermeasures, additional enhancements are still needed in order to improve the accuracy of IBIS models in mimicking the effects of the supply-voltage on the timing of output and supply-current switching. For

instance, faster or, on the contrary, slower state-transitions cannot be well reproduced in IBIS-based simulations mostly due to the pre-driver's sensitivity on the power-supply.

In addition, in order to support longer interconnects and higher data-rates, several equalization techniques have been developed and applied to transmitters and receivers of high-speed serializers/de-serializers (SERDES); in order to account for the effects of such complex circuit blocks, the IBIS specification has been extended with the Algorithmic Modeling Interface (IBIS-AMI). An IBIS-AMI consists of a standard IBIS file (so-called *analog part*), a compiled algorithmic code file (*.dll*) and a configuration file (*.ami*). The algorithms mimic the filtering effects introduced by the equalizers, and are coded in a parametric fashion; modifying the *.ami* file, the model user can specify – for each parameter - a desired value among a set of available ones. The rationale behind this strategy is to efficiently use linear time invariant (LTI) system theory to model the entire data communication channel. Transmitter, interconnections and receiver are represented by simplified linear blocks, each with its own frequency response (e.g., defined in terms of impedance, admittance or scattering parameters); the overall channel response is obtained by simply cascading the latter. The impact of equalizers can also be taken into account by extrapolating their filtering effects as described in the *.dll* and *.ami* files. In this way, the channel response to any given bit pattern can be easily and rapidly computed. It is not within the scope of this paper to trace the evolution of IBIS in detail; however, it is important to acknowledge the turning point that IBIS marked in the history of macromodeling and note that it is a living standard, constantly improving itself and spawning interesting off-shoots such as AMI.

IV. Alternative I/O-buffer modeling approaches

This section briefly summarizes the key aspects of a representative set of alternative I/O-buffer macromodeling approaches available in literature (see [5-18] and references therein). "Gray-box" methods rely on a certain level of knowledge on the physical circuit topology of the devices; "Black-box" methods, instead, adopt pure nonlinear input-output identification techniques to solve macromodeling problems. However, the practical situation is quite nuance, and engineers often seek to combine the advantages of both approaches and end-up settling for what they see as an acceptable compromise. Figure 4 provides a general view on how the state-of-the-art methods rank on a "gray level" chart.

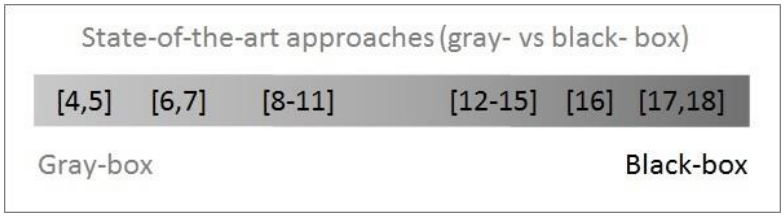

Figure 4: General classification of the available state-of-the-art approaches.

A first natural attempt of providing improved buffer models is to start from an IBIS-based circuit and introduce suitable modifications. In [5], the circuit

equivalent of Fig. 3 is modified with the inclusion of some additional blocks compensating for possible errors of the predicted output and supply port currents. The aforementioned blocks are implemented using standard SPICE elements (e.g., controlled-current sources). This modification improves the model accuracy when the power supply voltages bounce. In [6, 7], enhanced models that still belong to a simplified circuit approach are presented. The values of the circuit elements are defined by means of multivariate tables or surfaces built via standard toolboxes and accounting for the process-voltage-temperature variations. Both single-ended and differential topologies are considered. In [8, 9] IBIS-based models of output buffers are presented, with an enhanced description of the nonlinear dynamical behavior of devices. Specific emphasis is given on the replacement of the output linear capacitance C_{comp} with a nonlinear dynamical element where its estimation via a well-defined procedure. Paper [10] pays specific attention on the model improvements to account for the effects of the pre-driver stage (e.g., see Fig. 1) that possibly introduces device over-clocking operation. The physical based equivalent is supported with a block-oriented description of the pre-driver stage. Similar comments hold for [11] where the same philosophy is used to mimic the detailed circuit structure of the buffers.

All the previous approaches share the same modeling rationale~~,~~ where a specialized equivalent circuit is adopted to accommodate for all the features that are not explicitly included into IBIS. In all these approaches, model estimation relies on an identification procedure similar to the one outlined in the previous section for the native IBIS models. The main drawback in these approaches resides in rigid and restrictive *a priori* assumptions on the model structure. As technology evolves and improves, some of these assumptions may no longer hold and the methods require continuous updates and tunings.

References [17] and [18] suggest instead a fully black-box method. A single-piece model based on a neural network is used to reproduce device port currents as a function of all the port voltages, including the input voltage v_{in} explicitly. The perspective of a general, comprehensive model is attractive. However, particular care and specific tuning are required to compute model parameters for different devices. Furthermore, additional efforts are required to improve model efficiency, robustness and scalability (i.e., accounting for additional ports/pins such as differential outputs or supply ports, etc.). While definitely interesting, pure black-box approaches do not dissipate the burden of keeping up with design evolution, just shifting the required modifications from the model structure to the parametric identification.

Macromodeling via Parametric Identification of LOgic Gates (Mpilog) [12-14] is a well-known alternative to IBIS that has grown over the past ten years and managed to cross the academia-industry boundary. Mpilog attempts to generate models that merge the advantages of both simplified circuit equivalents and fully black-box representations. On one hand, it retains the two-piece paradigm that also IBIS uses, because this feature is instrumental in keeping the models compact and robust. Switching events are modeled with simple weighting functions, avoiding the need for cumbersome identification algorithms. On the other hand, surrogate parametric representations replace the simple elements like the controlled sources and the capacitors in Fig. 2. The parameters of these general-purpose mathematical structures can easily be estimated from the observation of

buffer transient responses only. The nonlinear identification problem is simpler than in purely black-box approaches, while the model still gains a sufficiently high degree of freedom to mimic the dynamic behavior of recent device features (a typical example is the complex dynamical response of recent differential drivers with internal voltage regulators [14]). In [15], a similar approach is used where different basis functions are used to describe the black-box parametric models (e.g., in terms of spline functions). The advantages of this sort of hybrid approach are manifold: both single ended and differential device technologies are handled in the same way, model estimation can be done form either numerical simulation or measurements. Furthermore, device overclocking operations may be reproduced without relying on detailed knowledge of the internal structure. Resulting models benefit from superior accuracy in the prediction of eye patterns and perform outstandingly in SI/PI co-simulations. Mpilog is a mature tool based on a well-defined framework that can be readily used in a design flow.

As a final remark, it is important to notice a recent paper [16] attempting a black-box circuit-theory-inspired representation of IC buffers. The authors use a nonlinear Thévenin-like model in an effort to provide a generalization of most of the existing two-piece structures adopted in IBIS, Mpilog and others [2-13]. The paper is practically an advanced proof of concept, dealing with single-ended devices only, and mainly focusing on accurately mimicking the behavior of buffer circuits during switching events, even when used in overclock scenarios.

V. Application test-case

This section presents the results of a combined signal and power integrity verification for the Command/Address (CA) bus of an LP-DDR3 memory interface; the analysis is first performed using detailed transistor-level netlists for the I/O-buffers, and then repeated using corresponding Mpilog macromodels.
The testbench is depicted in Figure 5. Output and supply ports of CA and CLK I/Os drive an interconnect model that represents parasitic components on signal traces and power delivery network as extracted from an example tablet design; the far-end loads are approximated with simple capacitors. Pseudo-Random-Bit-

Sequences (PRBS) provide the stimuli to the CA pads, while a clock pattern is applied to the CLK pad.

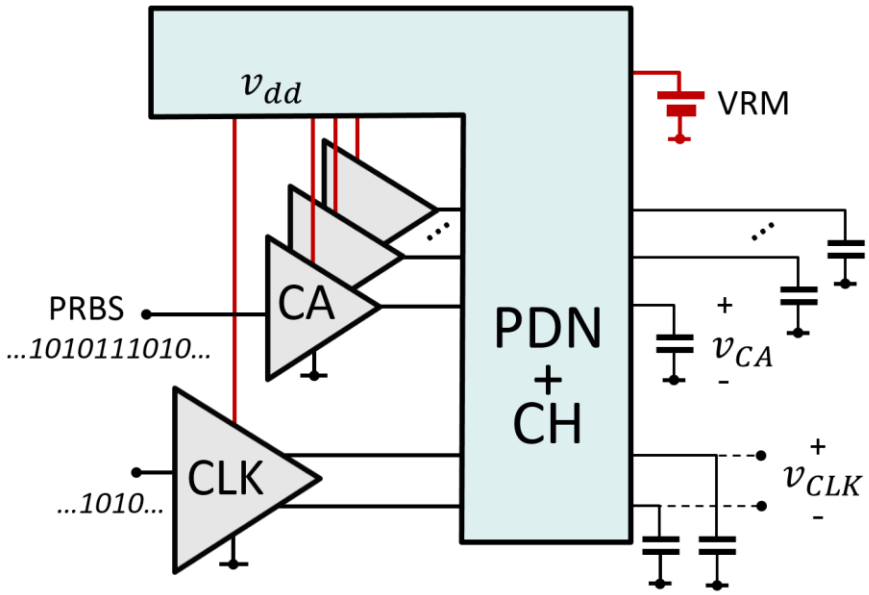

Figure 5: Signal and power integrity co-simulation testbench for an LP-DDR3 Command/Address Bus.

Figure 6 illustrates far-end waveforms for one CA and differential CLK signals (top-panel), I/O supply-current (mid-panel) and supply-voltage ripples (bottom-panel) as they result using transistor-level netlists or Mpilog models. An outstanding accuracy is demonstrated, both in terms of dynamics and timing on all the signals. CA and CLK waveforms are further reported in Figure 7 as clock-triggered eye-diagrams. Note that supply-voltage ripples, due to power delivery network parasitics and switching supply-current dynamics, introduce switching-timing variations on both CA and CLK.

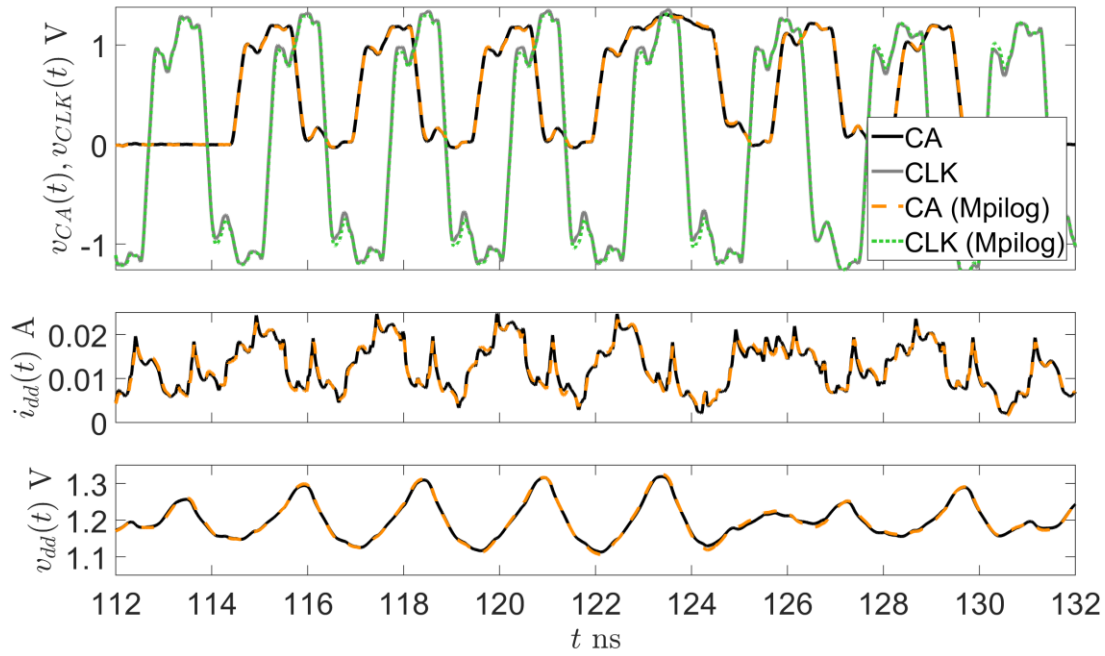

Figure 6: Waveforms resulting from the example SI/PI co-simulation; far-end CA and CLK signals (top-panel), supply-current (mid-panel) and supply-voltage ripples (bottom-panel).

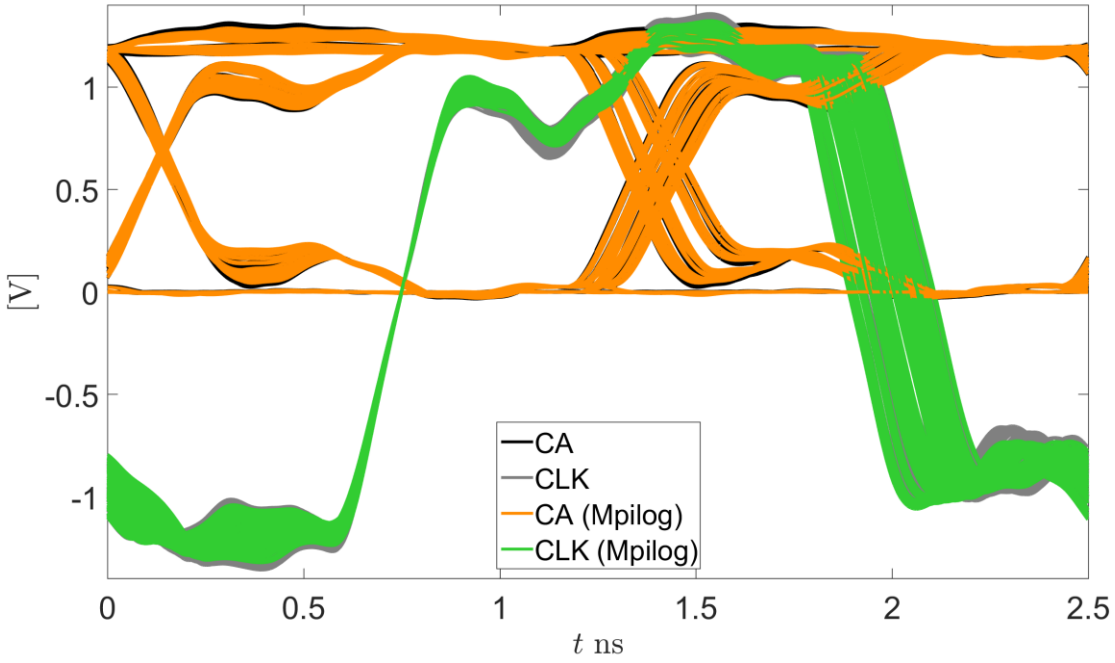

Figure 7: CA and CLK edge-triggered eye-diagrams from transistor-level (right) and Mpilog-based (left) example SI/PI co-simulation.

Table 1 quantifies the peak-to-peak jitter numbers computed from transistor-level and model-based analysis. Table 2 gives an overview of the simulation speed-up offered by Mpilog models that run approximatively over 1000 times faster than transistor-level descriptions. The acceleration is tremendous and the accuracy outstanding. With a fully-reliable macromodel-based signal and power integrity co-simulation framework, design teams are able to efficiently extend system-level verification coverage and increase design-verification cycles.

Table 1: Important LPDDR3 timing parameters as extracted from transistor-level and Mpilog-based example SI/PI co-simulation.

SI/PI Co-Simulation	Eye Width	CA p2p Jitter	CLK p2p Jitter
Transistor-level	1.06 ns	166 ps	221 ps
Mpilog-based	1.06 ns	169 ps	220 ps

Table 2: Run-time and speed-up factors for transistor-level versus Mpilog-based example SI/PI co-simulation.

	Run-Time	Speed-Up
Transistor-level	16h 53m	-
Mpilog-based	53.42 s	1138x

VI. Conclusions

Any researcher conducting a bibliographical study on I/O behavioral models will be impressed by the variety of approaches and the richness of ideas. The present paper references and summarizes the most important and the most recent methods ranging from the dominant industry standard IBIS to techniques described by the latest academic papers. There are some patterns in the emergence and evolution of these methods and algorithms. On one hand general technological progress requires incremental updates such as seen with IBIS. On the other hand accuracy issues in specific applications or in specific circumstances become critical and the need for powerful mathematical tools increases. Circuit modelers, especially academics, try to make better use of multi-linear and nonlinear algebra and turn to fields such as control theory for inspiration. This tendency is checked and balanced by the industry need for robustness and appetite for simple push-button solutions. Computational costs and compatibility with SPICE-based engines are powerful constraints and are likely to remain so in the near future, making macro-modeling a game of smart tradeoffs.

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Biographies

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He was an Electronic Packaging Engineer with the IBM Development, Boeblingen, Germany, from 2008 to 2013. He is currently a Research Assistant with the Electromagnetic Compatibility Group, Politecnico di Torino, where he works on algorithm development for optimization and order reduction of large-scale dynamical systems, and behavioral modeling of nonlinear circuit elements, with a specific application to the characterization of digital integrated circuits. His current research interests include macromodeling of electrical interconnects for electromagnetic compatibility and signal integrity problems.

Mihai Telescu obtained his Engineer's degree in Electronics and Telecommunications from the Polytechnic University of Timisoara in 2003. He obtained a Master of Science degree in France in 2004, jointly delivered by the ENSSAT of Lannion and the University of Brest. He then pursued a doctorate at the University of Brest and successfully defended his thesis in 2007. He worked with the EMC Group at the Politecnico di Torino, Italy, between 2008 and 2009 as post-doc fellow. Ever since, he has been an associate professor with Lab-STICC laboratory at the University of Brest, France. His research interests include linear and non-linear system identification, model order reduction and macromodeling in general.

Igor S. Stievano received the Master degree in electronic engineering and the Ph.D. degree in electronics and communication engineering from the Politecnico di Torino, Torino, Italy, in 1996 and in 2001, respectively. Currently he is an Associate Professor of Circuit Theory with the Department of Electronics and Telecommunications, Politecnico di Torino. He is the author or coauthor of more than 100 papers published in international journals and conference proceedings. His research interests are in the field of Electromagnetic Compatibility and Signal Integrity, where he works on the modeling and characterization of linear and nonlinear circuit elements. His recent activities include the behavioral modeling of digital ICs, transmission lines and PLC channels, the modeling and simulation of switching converters and the development of stochastic methods for the statistical simulation of circuits and systems with the inclusion of the effects of device or manufacturing uncertainties.