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Theoretical and experimental study of a thermal damper based on a CNT/PCM composite structure for transient electronic cooling

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Abstract

The present study focuses on a thermal damper that aims at smoothing the temperature peaks experienced by electronic components during transient solicitations. It consists of a silicon casing containing a densified or undensified carbon nanotube (CNT) array - linking directly both sides of the system - filled with phase change material (PCM). Theoretical consideration enables to define the concept of ideal thermal damper in order to study the foreseeable performance of this kind of system. Its thermal effectiveness can be predicted by means of two non-dimensional numbers, linked to the thermal capacity of the system and to the latent heat of the PCM. A numerical model shows that the behavior of a non-ideal thermal damper can differ from that of an ideal thermal damper: it is mostly affected by the thermal resistance at the interface between the silicon and the CNT and the temperature glide during the PCM phase change. To complete the study, prototypes of thermal dampers are experimentally characterized, in terms of heat storage and heat conduction performance. An estimation method of the total apparent thermal capacity of the tested sample is developed in order to quantify its latent heat storage capacity. The latent energy storage density is 1.6 J cm^{-2} for the best sample and is observed to be preserved after 850 thermal cycles. The total thermal resistance of the thermal damper is estimated by means of a laser flash test and a simple model of the sample. Sensitivity analyses show that the main thermal resistances are located at the interfaces between silicon and CNT.

Keywords: vertically aligned carbon nanotubes, phase change material, thermal energy storage, interfacial thermal resistance, transient electronic cooling

Highlights:

- Two non-dimensional parameters enabling to design an ideal thermal damper are identified
- Latent energy storage capacity of embedded PCM is estimated and reaches 1.6 J cm^{-2}
- Total thermal resistance of thermal damper is estimated via laser flash method
- Dominant thermal resistances are localized at the interfaces between silicon and CNT

Nomenclature

c_p	thermal capacity [$\text{J kg}^{-1} \text{ K}^{-1}$]
e	thickness [m]
f	frequency [Hz]
G	gain of the thermal damper [-]
G_0	gain of the thermal damper without phase change [-]

G_{env}	global thermal conductance [W K^{-1}]
h_{ref}	heat transfer coefficient [$\text{W m}^{-2} \text{K}^{-1}$]
h	specific enthalpy [J kg^{-1}]
h_{ls}	latent heat of liquid-solid phase change [J kg^{-1}]
H	enthalpy [J]
l	thickness [m]
m	mass [kg]
N_{mcp}	non-dimensional thermal capacity [-]
N_{mhlS}	non-dimensional latent heat of phase change [-]
p	length of the CNT cell wall [m]
q	heat flux [W m^{-2}]
q_0	constant part of the heat flux [W m^{-2}]
q_t	transient part of the heat flux [W m^{-2}]
Q	heat transfer rate [W]
r	thermal resistance per unit area [$\text{K m}^2 \text{W}^{-1}$]
R	thermal resistance [K W^{-1}]
S	area [m^2]
t	time [s]
T	temperature [K]
x	liquid fraction [-]
Z	thermal impedance [$\text{K m}^2 \text{W}^{-1}$]

Greek letters

$\alpha, \gamma, \psi, \varphi$	phases [rad]
δ	amplitude
ε	portion of the cavity occupied by CNT [-]
λ	thermal conductivity [$\text{W m}^{-1} \text{K}^{-1}$]
ρ	density [kg m^{-3}]
σ_T	standard deviation of the temperature distribution [K]

Subscript

1/2	related to the half of the maximum temperature rise
abs	absorbed
amb	ambient
b	back
bot	lower plate
cav	cavity
CNT	carbon nanotubes
eff	effective
eq	equivalent
f	front
ff	between both faces of the thermal damper
fus	fusion
m	mean
PCM	phase change material
ref	reference
Si	silicon
top	upper plate
tot	total

1 Introduction

The running miniaturization and the increasing performance of electronic devices lead to higher power densities and higher integration of electronic components with 3D packaging instead of 2D arrangements. For electronic components experiencing intermittent solicitations, these overall higher heat fluxes bring higher temperature peaks. The maximal allowable chip temperature of various electronic components generally ranges between 85°C and 120°C [1]. Exceeding this temperature can reduce the performance and shorten the lifetime of the electronic component. It is of interest to develop passive transient thermal management solutions in order to smooth the chip temperature.

The purpose of the thermal damper presented in this study is to smooth the temperature peaks of electronic components experiencing transient solicitations by means of phase change material (PCM). Indeed, PCMs can

store a large amount of energy at almost constant temperature because of their high latent heat of fusion or solidification. Examples of PCMs are paraffin waxes, fatty acids and sugar alcohols. They are used in various applications like thermal storage of solar energy, passive thermal regulation of buildings, thermal protection of biological products or food and electronic thermal management [2,3]. For electronic thermal management applications, paraffin waxes are often well adapted because their melting temperature can be close to the maximal operating temperature of electronics components [4]. In these conditions, their latent heat of phase change generally ranges from 100 J g^{-1} to 300 J g^{-1} . However, literature shows that the performance of paraffin-type PCMs can be affected after thermal cycling: in some studies, the latent heat of the tested paraffin remained constant during thermal cycling [5,6] whereas in some others, it declined, for example by 20 % after 600 thermal cycles [7] or by 25 % after 1500 thermal cycles [8]. Besides, the temperature of solidification of a PCM is often below its temperature of fusion because of supercooling, a metastable state of the liquid PCM below its temperature of fusion. The range of supercooling temperatures depends mainly on the chosen PCM, on its volume and on the environment (vibrations, walls, impurities...) [9]. Thermal aging and supercooling might affect the performances of the thermal damper and have to be considered when choosing a PCM.

However, the main drawback of PCMs is their low thermal conductivity. Thermal conductivity enhancement through insertion of dispersed high-conductivity nanostructures into PCMs (carbon-based nanostructures, carbon nanotubes, metallic and metal oxide nanoparticles and silver nanowires) leads to an effective thermal conductivity up to only twice that of PCMs [10]. The thermal conductivity of such composite PCMs remains small because of the high thermal resistance between neighboring high-conductivity elements. A much better thermal conductivity enhancement is reported when a thermal link exists between the particles, thus forming a single non-moving conductive matrix like graphite nanofibers with a high aspect-ratio [11], with controlled graphite plane orientation [12] or a graphite matrix [13]. However, the interactions between the PCM, the nanoparticles and a potential additional structure are far from being completely understood and further numerical and experimental studies are still necessary [14].

CNTs can also be implemented within the thermal damper with each CNT linking directly both silicon walls of the cavity containing the PCM. The review paper of Marconnet et al. [15] shows that the thermal conductivity of individual CNTs spans a very large range from $34 \text{ W m}^{-1} \text{ K}^{-1}$ to $13350 \text{ W m}^{-1} \text{ K}^{-1}$, most values ranging from $500 \text{ W m}^{-1} \text{ K}^{-1}$ to $3000 \text{ W m}^{-1} \text{ K}^{-1}$. Thermal conductivity of an individual CNT depends on its geometry (chirality, diameter, length, number of walls), on the quality of its lattice (defects, impurities) and on temperature [15,16]. Likewise, the measured thermal conductivity of vertically aligned CNT arrays spans a wide range from $0.145 \text{ W m}^{-1} \text{ K}^{-1}$ to $267 \text{ W m}^{-1} \text{ K}^{-1}$ [15]. The interfacial thermal resistances at the CNT/substrate contacts are additional variable parameters which are influenced by the fraction of CNTs which is really connected to the substrate and by the phononic coupling between the CNT and the substrate [16]. The reported interfacial thermal resistances at the CNT/substrate contact are of at least the same order of magnitude as the intrinsic thermal resistance of the CNT array alone [15]. The development of thermal interface materials (TIMs) based on vertically aligned CNT arrays shows that the interfacial thermal resistance CNT/substrate can be significantly decreased by using a third material in the contact area like indium for example [17].

Ling et al. [18] and Sahoo et al. [19] performed two extensive literature reviews on the use of PCM for electronic cooling and it appears that the most recent studies on passive cooling of electronics with PCM are based on the addition of PCM in an external structure. PCM can be embedded between the fins of a traditional heat sink [1,20–23] or between high conductivity carbon walls with CNTs added into the PCM [24]. In this configuration, the main issue is to predict the heat transfer in the PCM and particularly the evolution of the phase-change front in the system. PCM integration in an array of micro-reservoirs etched in a silicon substrate in order to stabilize the surface temperature during short transient thermal solicitations is also reported but this type of studies is very rare. For instance Muratore et al. [25] studies micro-inclusions of PCM, but the areal thermal energy storage density remained small (about 800 J/m^2). The design, fabrication and characterization of such systems remain very challenging.

In the thermal damper presented in this study, PCM is integrated into an array of carbon nanotubes (CNT), the whole being embedded in a silicon (Si) casing. This passive cooling system aims at increasing the thermal inertia per unit of volume of the electronic component by means of the latent heat of the PCM while keeping a high thermal conductance by means of the CNT array linking both silicon plates. Compared to traditional systems where the PCM is located within an external structure, the embedding of the PCM in the silicon substrate itself changes the phenomena that have to be taken into account to understand the behavior of this kind of thermal damper.

This paper consists of two main parts. The first part establishes the theoretical bases of the system. The concept of ideal thermal damper is defined and discussed in order to highlight the area of use of the system depending on the frequency and on the amplitude of the thermal solicitation. The causes of thermal performance deterioration between an ideal and a non-ideal thermal damper are discussed based on the results of a numerical model. The second part of the paper presents an experimental characterization of several prototypes of thermal dampers. The tested samples and the experimental setup are first presented. The heat storage properties of the

thermal damper are then quantified and the effect of thermal aging is measured. Finally, the thermal conductance of the vertically aligned CNT arrays embedded in the thermal dampers is characterized and discussed.

2 Theoretical considerations on the thermal performance of a damper

2.1 General design and expected properties of the thermal damper

A thermal damper aims at decreasing the temperature peak of an electronic component subjected to a transient heat flux by increasing the apparent thermal capacity of the system while having a small impact on its overall thermal conductance. It consists of a high thermally conductive matrix filled with phase change material.

The concept and the assembly of such a thermal system has been initially presented by Ollier *et al.* [26]. This paper aims at characterizing this particular system both theoretically and experimentally. Nonetheless, the theoretical analysis does not rely exclusively on this system and can be applied to other dimensions and materials. In the configuration of the present study, the thermal damper is made of two silicon plates of thickness $380\ \mu\text{m}$ (figure 1) located between an electronic component and a heat sink, for example a printed circuit board (PCB). A $100\ \mu\text{m}$ deep cavity is etched in the bottom plate on which carbon nanotubes are grown. The CNTs are oriented along the heat flux lines in order to have an optimized thermal conductive path from the heated to the cooled face of the device. The free CNT tips are bonded into a soft metal layer deposited on the top silicon plate. This technique enables to minimize the interfacial thermal resistance between the CNT and the silicon wafer [17]. As explained in the introduction, the equivalent thermal conductivity of such a composite medium is much better than mixing CNTs with PCM because the thermal path inside the structure is optimally designed and continuous. The densification of the CNTs enhances the solidity of the system and enables to create a hollow structure in which the PCM is introduced (figure 1b). The cavity is filled with paraffin having a melting temperature close to the maximum admissible temperature of the related electronic components. In the work of Ollier *et al.* [26], a paraffin with a carbon distribution of C_{30} to C_{48} is chosen because of its high latent heat and its small supercooling. The properties of this PCM are given in table 1. In order to simplify the modeling of the system, these properties are supposed to be the same when the PCM is solid or liquid. As this paraffin is not a pure substance, the phase change temperature mainly ranges between 60°C and 90°C and reaches a maximum at a temperature of about 80°C . More details of the system are provided in the experimental section of the paper.

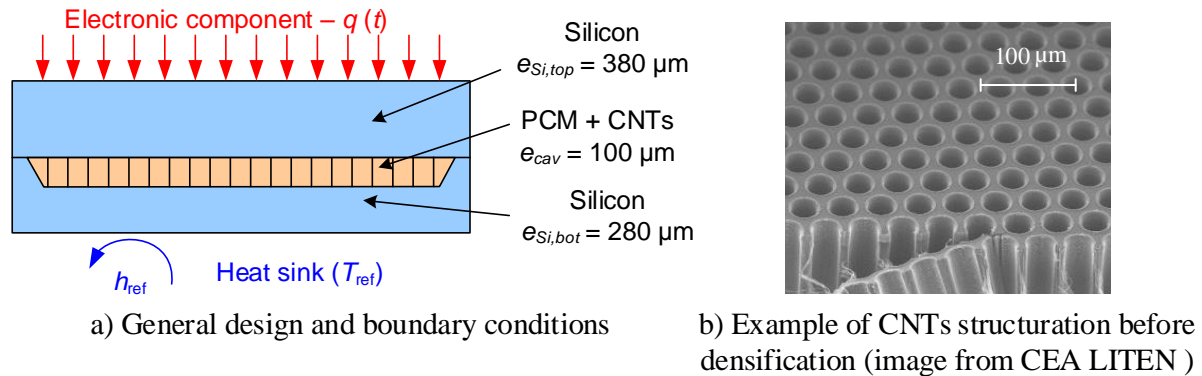


Figure 1: Design of the thermal damper.

Table 1: PCM properties (paraffin C_{30} - C_{48} from Kaplan Energy).

Phase change temperature range	$60\text{-}90^\circ\text{C}$
Density	$800\ \text{kg m}^{-3}$
Latent heat of phase change	$205\ \text{kJ kg}^{-1}$
Sensible thermal capacity	$2.2\ \text{kJ kg}^{-1}\ \text{K}^{-1}$
Thermal conductivity	$0.2\ \text{W m}^{-1}\ \text{K}^{-1}$

In the considered application, the thermal damper is located between an electronic component and a PCB acting as a heat sink. Therefore, an accurate modeling of such a system requires the modeling of the entire thermal path including the PCB and the electronic component. In order to simplify the analysis, the present work focuses only on the thermal damper. The electronic component is supposed to impose a uniform heat flux $q(t)$ on the top face of the thermal damper while an imperfect contact is assumed between the PCB and the bottom plate. This last

condition is modeled by considering a heat transfer coefficient h_{ref} between the PCB - at a constant temperature T_{ref} - and the bottom face. The heat transfer coefficient depends on the contact thermal resistance between the two medium. Orders of magnitude of such thermal resistances can be found in the study of Sartre and Lallemand [27]. In the present study, we assume, as a standard case, a good thermal contact between the PCB and the thermal damper with a contact resistance equal to $5 \times 10^{-4} \text{ K m}^2 \text{ W}^{-1}$, which corresponds to a heat transfer coefficient of $2000 \text{ W m}^{-2} \text{ K}^{-1}$.

The goal of a thermal damper is to increase the thermal capacity of an electronic component with small impact on its overall conductance. As a consequence, the thermal resistance of the thermal damper in steady state conditions must be as low as possible. In the studied configuration, this thermal resistance r_{th} can be written as (figure 1):

$$r_{th} = \frac{e_{Si,top}}{\lambda_{Si}} + \frac{e_{cav}}{\varepsilon \lambda_{eff,CNTNTC} + (1 - \varepsilon) \lambda_{PCM}} + \frac{e_{Si,bot}}{\lambda_{Si}} \quad (1)$$

where λ is the thermal conductivity and ε the portion of the thermal damper cavity occupied by CNTs. The thermal resistance between the CNTs and the silicon plates is integrated in the effective thermal conductivity of the CNTs. It is also possible to define an equivalent thermal conductivity λ_{eq} of the composite medium CNT + PCM as:

$$\lambda_{eq} = \varepsilon \lambda_{CNT} + (1 - \varepsilon) \lambda_{PCM} \simeq \varepsilon \lambda_{CNT} \quad (2)$$

Considering a thermal conductivity of the densified CNTs equal to $750 \text{ W m}^{-1} \text{ K}^{-1}$ [28], a portion of CNTs equal to 0.25 would lead to an equivalent thermal conductivity of the composite medium CNT + PCM equal to $170 \text{ W m}^{-1} \text{ K}^{-1}$. If such a thermal conductivity is achieved for the densified CNTs, the thermal damper would have a thermal conductivity equivalent to that of a silicon plate having the same thickness.

2.2 Definition and modeling of an ideal thermal damper

A thermal damper enables to store heat when the amplitude of the transient thermal solicitation is maximum. Heat is then transferred to the heat sink during the low solicitation phase. Let us define an ideal thermal damper as a system made of components with an infinite thermal conductivity and for which the phase change of the PCM occurs at a well-defined unique phase change temperature T_{fus} (no temperature glide and no supercooling). Under these conditions, the system is able to store a certain amount of heat at constant temperature. As a consequence, the temperature of the thermal damper is uniform and its thermal behavior can be calculated analytically.

2.2.1 Modeling of an ideal thermal damper

The energy balance for the system in the configuration of figure 1 can be written as:

$$\frac{dH}{dt} = qS - h_{ref}S(T - T_{ref}) \quad (3)$$

with:

$$dH = (mc_p)_{tot} dT + m_{PCM} h_{ls} dx \quad (4)$$

where H and T are the enthalpy and the temperature of the ideal thermal damper, q is the heat flux imposed on the upper plate of area S . h_{ref} is the heat transfer coefficient between the thermal damper and the heat sink, which is supposed to be constant. h_{ls} is the latent heat of phase change of the PCM, x is its liquid fraction and $(mc_p)_{tot}$ is the sum of the thermal capacity of all the components of the system (silicon, PCM and CNT).

Considering the single-phase and the two-phase zones independently, equation (3) can be written as:

$$\begin{cases} \frac{dT}{dt} = \frac{qS - h_{ref}S(T - T_{ref})}{(mc_p)_{tot}} & \text{if } T \neq T_{fus} \text{ (single-phase zone)} \\ \frac{dx}{dt} = \frac{qS - h_{ref}S(T - T_{ref})}{m_{PCM} h_{ls}} & \text{if } T = T_{fus} \text{ (two-phase zone)} \end{cases} \quad (5)$$

As an example, the total thermal capacity of the thermal damper described in figure 1 is equal to $1250 \text{ J K}^{-1} \text{ m}^{-2}$ in the single-phase zone. If a constant heat flux equal to $q = 5 \text{ W cm}^{-2}$ is imposed to the top of the system, the bottom being insulated ($h_{ref} = 0 \text{ W m}^{-2} \text{ K}^{-1}$), the rate of temperature increase is equal to 40 K s^{-1} . The PCM filling the cavity has a total latent heat equal to 1.7 J cm^{-2} , which means that with the same heat flux, the PCM melts in about 0.3 s. This example gives an order of magnitude of the type of solicitation that the thermal damper can sustain.

2.2.2 Frequency response of an ideal thermal damper

The frequency response of a system characterizes its behavior when it experiences a sinusoidal heat flux solicitation. In this section, the imposed heat flux is thus considered as the sum of a constant component q_0 and a transient sinusoidal component q_t :

$$q(t) = q_0 + q_t(t) \quad (6)$$

with $q_t(t) = \delta q \cos(2\pi f t + \varphi)$. δq , f and φ are the amplitude, the frequency and the phase of the heat flux oscillation respectively. The energy balance equation (equation (3)) can be rewritten as:

$$\frac{dH}{dt} = q_t S - h_{ref} S (T - T_m) \quad (7)$$

with $T_m = T_{ref} + q_0/h_{ref}$. This equation is similar to equation (3), but the constant part of the thermal solicitation is hidden. Therefore, the thermal damper can be viewed as a system subjected to a sinusoidal solicitation with a mean value equal to zero and a reference temperature equal to T_m , which depends on the constant part of the solicitation.

The behavior of an ideal thermal damper corresponds to that of a low-pass filter: the variation of heat flux imposed on the system is transferred to the PCB after being damped. In order to characterize this filter, the concept of thermal impedance can be used. It is the ratio between the temperature variation amplitude and the heat flux variation amplitude:

$$Z_{th} = \frac{\delta T}{\delta q} \quad (8)$$

with $\delta T = \max|T(t) - T_m|$

The thermal impedance can also be written under the non-dimensional parameter G :

$$G = \frac{h_{ref} \delta T}{\delta q} = h_{ref} Z_{th} \quad (9)$$

G is the gain of the equivalent low-pass filter corresponding to the ideal thermal damper. When $G = 1$, there is no damping of the output heat flux variation and the temperature variation is maximum. When $G = 0$, the variation of the imposed heat flux is totally damped and the thermal damper temperature remains constant.

It is possible to obtain an analytical expression of the thermal impedance and the filter gain for two different cases:

- The thermal damper remains in the single phase zone (solid or liquid),
- The mean thermal damper temperature is equal to the fusion temperature of the PCM (centered two-phase zone)

Temperature response of the thermal damper in the single phase zone

In the single-phase zone, equation (7) becomes:

$$(mc_p)_{tot} \frac{dT}{dt} = \delta q S \cos(2\pi f t + \varphi) - h_{ref} S (T - T_m) \quad (10)$$

If $(mc_p)_{tot}$ is assumed to be constant, this equation can be solved directly. We get:

$$T = T_m + \delta T \cos(2\pi f t + \varphi - \Phi) \quad (11)$$

with $\delta T = \frac{\delta q S}{\sqrt{(h_{ref} S)^2 + (2\pi f (mc_p)_{tot})^2}}$ and $\Phi = \arccos\left(h_{ref} \frac{\delta T}{\delta q}\right) = \arccos(G)$

The thermal damper temperature evolution is sinusoidal around the reference temperature with a phase shift Φ relative to the heat flux variation. In terms of non-dimensional parameter, the filter gain depends only on the parameter N_{mcp} :

$$G = \frac{1}{\sqrt{1 + N_{mcp}^2}} \quad (12)$$

with $N_{mcp} = \frac{2\pi f (mc_p)_{tot}}{h_{ref} S}$. This term corresponds to a non-dimensional total thermal capacity of the thermal damper.

The thermal impedance is equal to:

$$Z_{th} = \frac{1}{\sqrt{(h_{ref})^2 + \frac{(2\pi f(m c_p)_{tot})^2}{S}}} \quad (13)$$

The thermal impedance does not depend on the heat flux. It decreases when the frequency increases: a higher frequency solicitation induces a smaller thermal damper temperature variation. Figure 2 presents the evolution of the thermal impedance of the ideal thermal damper associated to the geometry presented in the first section as a function of the solicitation frequency for different heat transfer coefficients between the thermal damper and the PCB. The case $h_{ref} = 0$ corresponds to an adiabatic system, for which the impedance tends to an infinite value when the frequency tends to zero (steady state). It is possible to define a cut-off frequency $f_{1/2}$ for which the thermal impedance is equal to half the impedance of the steady state in the same conditions ($G = 0.5$):

$$f_{1/2} = \frac{\sqrt{3}h_{ref}S}{2\pi(m c_p)_{tot}} \quad (14)$$

The temperature variations for frequencies higher than $f_{1/2}$ are damped, even without phase change. The thermal impedance tends to zero when the frequency tends to an infinite value. For lower frequencies, a heat flux variation induces an important temperature variation of the thermal damper and, as a consequence, a high maximal temperature of the electronic component that needs to be cooled.

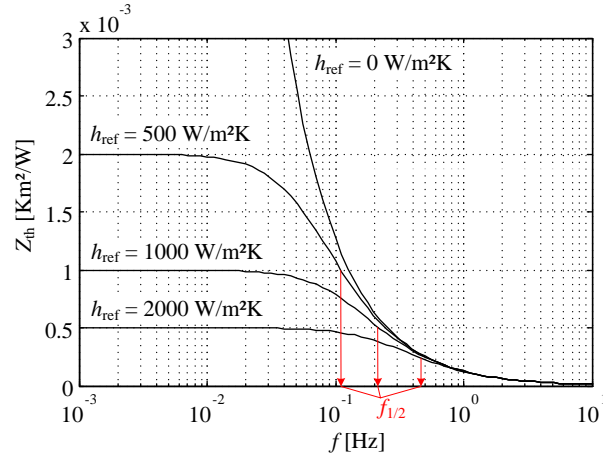


Figure 2: Thermal impedance in the single-phase zone of the ideal thermal damper associated to the geometry considered in figure 1.

Temperature response of the thermal damper in the two-phase zone

If the mean thermal damper temperature is equal to the fusion temperature of the PCM, phase change occurs and the thermal damper temperature keeps constant during a certain time. An analytical expression of the thermal impedance cannot be given directly, but it is possible to show that the filter gain G depends only on two non-dimensional parameters, N_{mcp} and $N_{mhls} = \frac{2\pi f m_{PCM} h_{ls}}{\delta q S}$ (see appendix 1). N_{mhls} represents the latent heat of phase change of the thermal damper in a dimensionless form. Figure 3 presents the evolution of G as a function of these two parameters. Several asymptotic cases can be highlighted:

- For $N_{mhls} = 0$, $G = 1/\sqrt{1 + N_{mcp}^2}$ which is conform to the single phase case.
- For $N_{mhls} \geq 2$, $G = 0$ for any N_{mcp} .
- For $N_{mcp} = 0$, $G = 1$ for $0 \leq N_{mhls} \leq 1$ and $G = \sqrt{1 - (N_{mhls} - 1)^2}$ for $1 \leq N_{mhls} \leq 2$.

The case $N_{mhls} = 2$ corresponds to the situation for which the energy corresponding to half a period of the imposed heat flux variation is equal to the energy stored into the PCM during phase change. As a consequence, and contrary to the single-phase zone, the temperature variations are totally damped for a frequency higher than a threshold value f_0 :

$$N_{mhls} \geq 2 \Leftrightarrow f \geq f_0 \quad \text{with} \quad f_0 = \frac{\delta q S}{2\pi m_{PCM} h_{ls}} \quad (15)$$

The dimensional parameters, and especially the thermal impedance can be calculated from the value of G , N_{mcp} and N_{mhls} . Figure 4 presents the thermal impedance of the ideal thermal damper in the two-phase zone as a function of the oscillation frequency, for different heat transfer coefficients and for different heat flux amplitudes. It can be seen that the cut-off frequency depends strongly on the amplitude of the heat flux oscillations whereas the steady state depends only on the thermal resistance between the thermal damper and the PCB.

The use of a thermal damper for electronic thermal management is worthwhile only if the thermal impedance in the two-phase zone is much lower than the thermal impedance in the single-phase zone. The comparison of figure 2 and figure 4 shows that it is verified for a limited range of frequency that depends on the heat flux amplitude and on the total latent heat of PCM. For small frequencies, the amount of PCM is too small to damp significantly the temperature variations whereas for high frequencies, the temperature variation is always damped by the thermal capacity of the materials composing the thermal damper even without phase change. This result can also be highlighted using non-dimensional parameters. Figure 5 presents the part of the attenuation due to the phase change only, represented by $G_0 - G$, where G_0 is the filter gain with no phase change ($N_{mhls} = 0$). The attenuation can be significant only for $N_{mhls} > 1$ and is larger for N_{mcp} around 1. For $N_{mhls} < 1$, $G_0 - G$ is limited to about 0.3 in the best configuration. This abacus is useful to design a thermal damper for a known thermal solicitation.

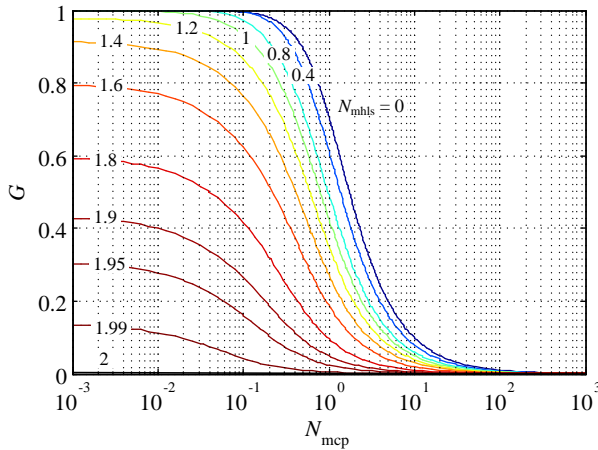


Figure 3: Gain of the equivalent filter of an ideal thermal damper.

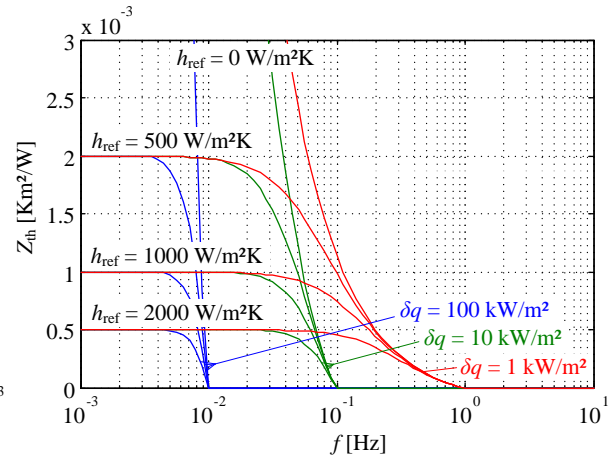


Figure 4: Thermal impedance of an ideal thermal damper in the two-phase zone.

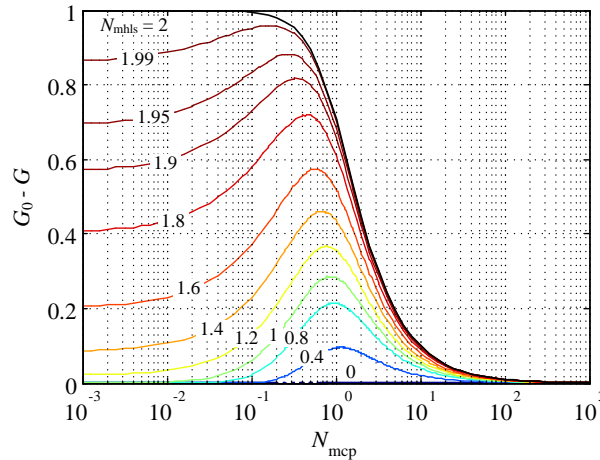


Figure 5: Attenuation due to the phase change.

In practice, the mean temperature of the thermal damper depends on the boundary conditions and is therefore not always equal to the phase change temperature of the PCM. If both temperatures are far from each other, no phase change occurs and the thermal damper behavior corresponds to the single-phase zone (figure 2). If the thermal damper mean temperature is close to the PCM phase change temperature, only a part of the PCM is used to store heat. Figure 6 summarizes different cases of the thermal damper temperature evolution depending on the value of the mean temperature compared to the phase change temperature and on the amplitude of the imposed heat flux compared to the PCM latent heat. For low heat flux amplitude, an ideal thermal damper can be viewed as a thermal barrier that prevents the thermal damper temperature to become higher than the phase change temperature. For high heat flux amplitudes, the thermal damper can only damp partly the temperature variation.

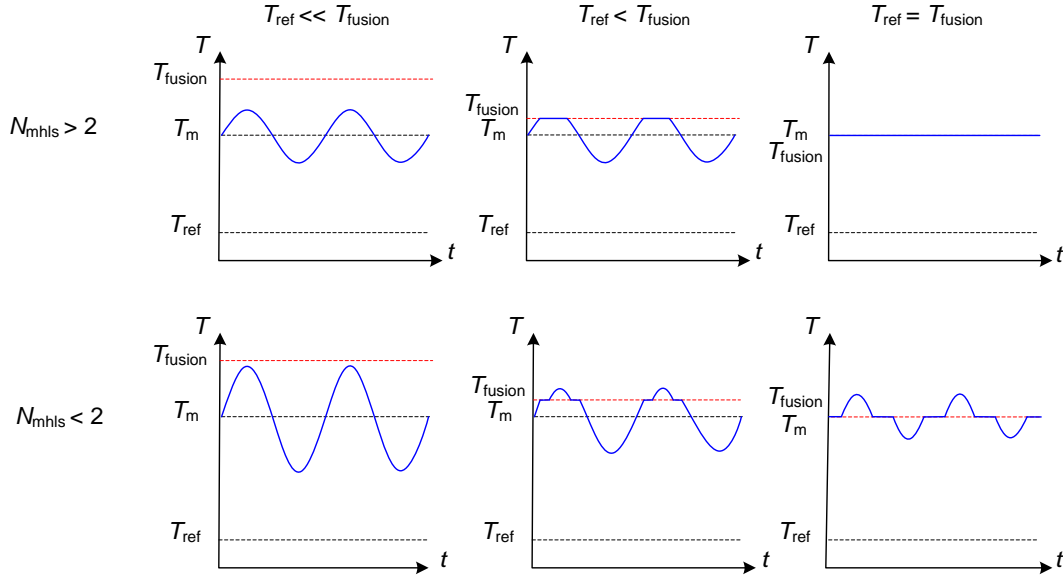


Figure 6: Thermal behavior of an ideal thermal damper subjected to a sinusoidal heat flux.

2.3 Thermal behavior of a non-ideal thermal damper

In a real system, the phase change of the PCM does not occur at a well-defined temperature, but there is a glide of phase change temperature with a range that can reach several degrees. Furthermore, a temperature hysteresis exists between the melting phase and the freezing one due to the supercooling phenomenon. Moreover, the thermal conductivity of the different materials of a thermal damper is finite. Therefore, the effect of the maximum distance between the PCM and the CNTs needs to be studied. Finally, the thermal junction between the CNTs and the silicon plates is not perfect, leading to a contact thermal resistance.

The effect of the contact thermal resistance between the CNTs and the silicon plates can be estimated with the previous model. Adding a thermal resistance is equivalent to decrease the heat transfer coefficient between the heat sink and the thermal damper. Figure 4 shows that when h_{ref} is divided by two, the thermal impedance of the system is doubled. Therefore, this parameter has a huge influence on the thermal performance of the thermal damper and needs to be optimized.

In the next section, a numerical model is developed to show the influence of the other parameters.

2.3.1 Thermal modeling of a non-ideal thermal damper

In order to highlight the difference of behavior between the ideal and the non-ideal system, a simplified numerical model was developed. An elementary cell of the thermal damper is considered. A honeycomb structure is chosen in the present section as an example of densified pattern. Figure 7 summarizes the geometrical properties of the structure, as well as the discretization principle.

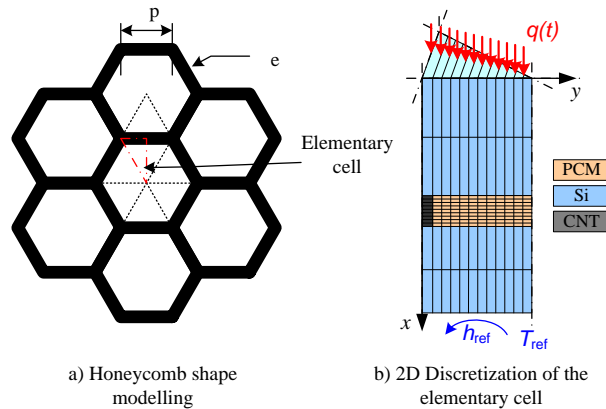


Figure 7: Details of the honeycomb structure of densified CNTs.

The thermal damper is modelled at the scale of an elementary cell, consisting of 1/12 of a honeycomb structure, due to the symmetry of this particular system. A finite difference 2D model is developed to solve the

heat transfer equation in this domain. The thermal conductivity of the CNT is supposed to be isotropic and equal to $750 \text{ W m}^{-1} \text{ K}^{-1}$ [28]. The cavity is supposed to be fully filled with PCM.

The phase change of the PCM is taken into account by means of an equivalent thermal capacity $c_{p,eq}$, which is temperature-dependent and can be obtained by writing the enthalpy balance of the PCM:

$$dh = c_p dT + h_{ls} dx = c_{p,eq} dT \quad (16)$$

By integrating equation (16) between $x = 0$ and $x = 1$, the expression becomes:

$$h_{ls} = \int_{T_{x=0}}^{T_{x=1}} (c_{p,eq} - c_p) dT \quad (17)$$

The PCM equivalent thermal capacity ($c_{p,eq} - c_p$) during the fusion or the solidification can be extracted from a DSC measurement, as it is presented in figure 14 of the experimental part. One can note that the measurements obtained with a DSC have to be carefully analyzed since they may depend on the rate of temperature increase, on the mass of PCM introduced in the system and on the crystalline form adopted by the PCM during the previous solidification. Therefore, an accurate behavior of such materials is difficult to estimate. In the present section, the equivalent thermal capacity of the PCM is modelled using a Gaussian function:

$$c_{p,eq,PCM} - c_{p,PCM} = \frac{h_{ls}}{\sigma_T \sqrt{2\pi}} e^{-\frac{(T-T_{fusion})^2}{2\sigma_T^2}} \quad (18)$$

where σ_T is the standard deviation corresponding to the Gaussian distribution. The behavior of the PCM chosen in the present study can be described using $T_{fus} = 80^\circ\text{C}$ and $\sigma_T = 5 \text{ K}$. The hysteresis of phase change due to the supercooling phenomenon is not taken into account.

2.3.2 Parameter analysis

In this section, the thermal performance of the system is presented for a sinusoidal solicitation with a mean value equal to zero and a reference temperature equal to the mean PCM phase change temperature. The CNT walls thickness is supposed to be equal to $e = 5 \mu\text{m}$ in the entire section (figure 7). When not mentioned, the wall length is equal to $p = 25 \mu\text{m}$.

Figure 8 presents the temperature variation of the topmost plate (where the heat flux is applied) for three different heat flux amplitudes ($\delta q = 0.2 \text{ W cm}^{-2}$, $\delta q = 1 \text{ W cm}^{-2}$ and $\delta q = 5 \text{ W cm}^{-2}$) and for two heat transfer coefficients between the system and the PCB ($h_{ref} = 0 \text{ W m}^{-2} \text{ K}^{-1}$ and $h_{ref} = 2000 \text{ W m}^{-2} \text{ K}^{-1}$). For low solicitation frequencies, the thermal damper behavior is similar to that of an ideal system. Therefore, its temperature can be considered as uniform. Conversely, it can be seen on this figure that the behavior of the thermal damper differs from that of an ideal system for high solicitation frequencies. In that case, the thermal impedance is not equal to zero for frequencies higher than the cut-off frequency. This can be explained by two phenomena:

- The temperature glide during the PCM phase change leads to a variation of the temperature during a transient thermal solicitation.
- The low thermal diffusivity of the PCM prevents the heat to reach the center of the cells for high frequency solicitations. As a consequence, one part of the PCM is not useful for the system. Note that in the present configuration, the high thermal conductivity of the silicon leads to a negligible temperature gradient in the silicon plates.

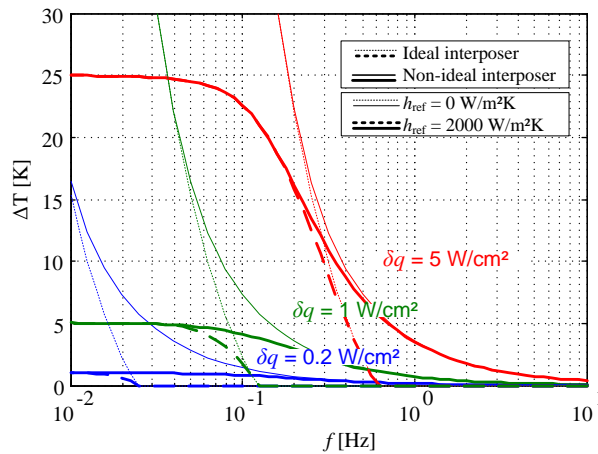


Figure 8: Non-ideal thermal damper behavior compared to the ideal one ($p = 25 \mu\text{m}$, $\sigma_T = 5 \text{ K}$).

The influence of the dimension of the honeycomb structure is presented in figure 9. The size of the honeycomb structure has a very small influence on the overall system properties behavior because the time required for the heat to reach the center of the cell is negligible. On the other side, if the PCM experiences a temperature glide during phase change, the thermal damper does not act strictly as a thermal barrier. The maximum temperature variation due to the temperature glide is of the same order of magnitude as the standard deviation corresponding to this temperature glide.

As a conclusion, the influence of the cell dimensions considered in the present study is negligible compared to the influence of the temperature glide during phase change. The theoretical approach developed in the present section enables to validate the concept and the geometry of the thermal damper. In the next part, experimental results obtained with this device are presented, with a specific attention to the PCM behavior and to the impact of the thermal resistance between the CNT and the silicon plates.

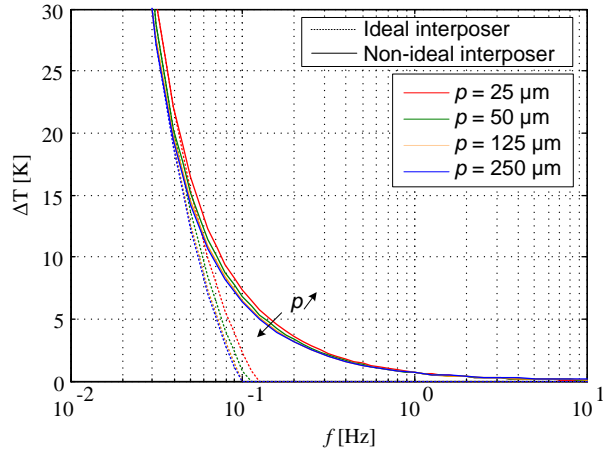


Figure 9: Effect of the honeycomb dimension p ($\delta q = 1 \text{ W cm}^{-2}$; $h_{\text{ref}} = 0 \text{ W m}^{-2} \text{ K}^{-1}$; $\sigma_T = 5 \text{ K}$).

3 Experimental study of the thermal damper

3.1 Test samples and experimental setup description

3.1.1 Test samples

The studied thermal dampers consist mainly of an array of vertically aligned CNTs filled with PCM and integrated between two silicon chips. Typical dimensions of whole samples are $20 \times 20 \times 0.6 \text{ mm}^3$ (figure 10). The area of the cavity etched in silicon and containing the CNT/PCM composite structure is $16 \times 16 \text{ mm}^2$. An additional sealing material (adhesive or SU-8 photoresist) can be added on the periphery of the composite CNT/PCM structure in order to link both silicon chips. The PCM is a paraffin wax with a carbon distribution ranging between C_{30} and C_{48} (table 1). The interface linking the CNTs and the silicon can be the catalyst interface on which the CNTs grew up (Si/Al₂O₃/Fe/CNT) or a bonding interface designed to enhance the mechanical and thermal links between the CNT tips and the silicon (Si/Ti/Au/In/Au/Ti/CNT).

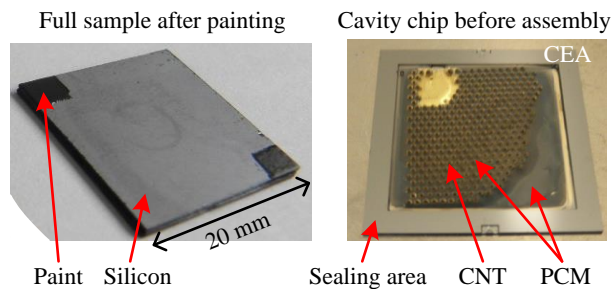


Figure 10. Typical pictures of the studied thermal dampers.

In this study, some samples exhibit a CNT array similar to classical vertically aligned carbon nanotubes arrays (VACNT): CNTs are grown on a catalyst interface (Si/Al₂O₃/Fe), then covered with Ti/Au and finally bonded to the bonding interface (Si/Ti/Au/In) of the mating silicon chip.

More sophisticated samples feature a densified array of CNTs: after the growth step on a sacrificial silicon chip, the CNT array is immersed in a liquid which is then evaporated, thus gathering CNTs in vertical bundles. The geometry of the densified structure is controlled thanks to a preliminary patterning of the catalyst layer enabling the growth of CNTs on selected areas only (figure 11). The densified array of CNTs is then covered with Ti/Au and pressed against the bonding interface (Si/Ti/Au/In) of the silicon cavity. The sacrificial silicon chip is removed and a second bonding with the top silicon chip is processed the same way, resulting in bonding interfaces (Si/Ti/Au/In/Au/Ti/CNT) at both ends of the densified CNT array.

During the assembly, both silicon chips are pressed together, resulting in a compression of the CNT array from the original length ($\approx 200 \mu\text{m}$) to the distance between surrounding silicon surfaces (cavity depth of $150 \mu\text{m}$ + sealing thickness of 10 or 20 μm). For all samples, the order of magnitude of the CNT density in the catalyst area of growth is a few $10^{11} \text{ CNT cm}^{-2}$. More details about the fabrication process of the samples are provided in [26].

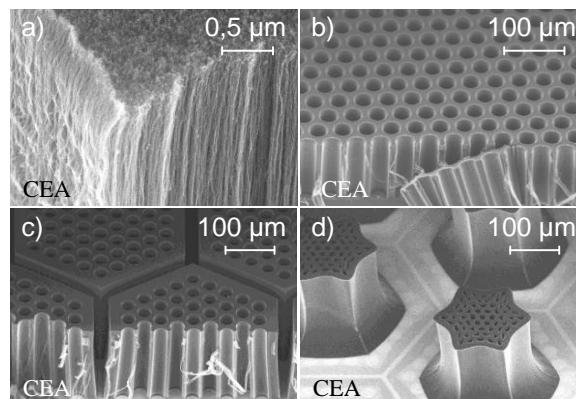


Figure 11. SEM images of different configurations of the CNT array after growth: edge of a standard CNT array (a), array with holes (b), array with holes and hexagonal splits before (c) and after (d) densification (images and fabrication: CEA-Liten).

3.1.2 Test bench

The sample is heated up by means of an 808 nm laser (nLight Pearl TKS). The near-infrared laser beam is shaped using a set of lenses and reflected uniformly toward the front surface of the sample (figure 12). The individual silicon chips of the samples (thickness > 120 μm) are opaque for the wavelength 808 nm.

Both the front and the rear surfaces of the sample are simultaneously visualized by an infrared (IR) camera using a set of four IR mirrors. The IR thermography device (FLIR SC7600) is sensible between 2.5 and 5.5 μm wavelengths. Nevertheless, silicon is semi-transparent in this wavelength range. Therefore, when a measurement of the absolute temperature is required, dull black opaque paint is deposited on the surface of the sample. However, this additional paint thickness of about 60 μm implies additional thermal inertia and thermal resistance.

Spectrometric measurements showed that the black paint used (JELT® NOIR MAT 700°C) is a gray body in the spectral range of the IR camera. The correct emissivity value to apply to the software of the IR camera facing this paint was estimated via a dedicated calibration using a painted copper sample including a calibrated thermocouple and heated up at different temperature levels with the laser. The camera calibration takes into account the real emissivity of the paint, the reflectivity of the IR mirrors and the bias of the IR camera.

A large light-tight enclosure ($\approx 2.4 \times 0.6 \times 1 \text{ m}^3$) consisting mainly of black anodized aluminum contains the laser beam, the sample and the IR camera. It enables to maintain a controlled radiative environment as well as a constant air temperature and undesired optical reflections are reduced at a minimum. The sample is hold by a specific sample holder consisting of three thin steel rods with a V-shape end.

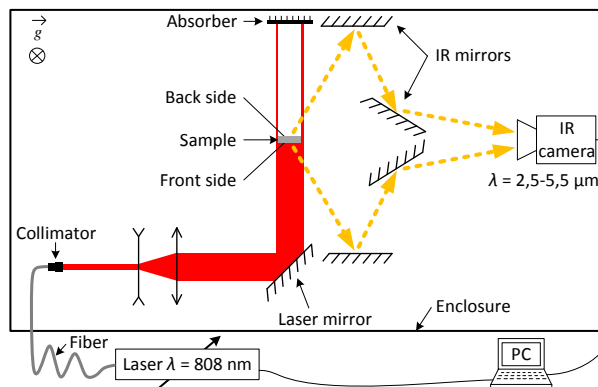


Figure 12. Main components of the test bench (top view, not to scale).

3.1.3 Thermal cycling procedure

Thermal cycling aims at examining the evolution of both main functions of the thermal damper – heat storage and heat conduction – facing accelerated thermomechanical aging. The specifications of the thermal cycle of this study are inspired from the “JEDEC JESD22-A104” standard dedicated to thermal cycling of electronic components [29]. It consists in a repetitive alternating of a hot phase (125 °C) and a cold phase (25 °C). The full thermal cycling includes 850 cycles as well as control tests concerning the heat storage (two crenel solicitations like in section 3.2) and the heat conduction (three flash solicitations like in section 3.3) after respectively 0, 5, 50, 100, 450 and 850 cycles. The test configuration is as illustrated in figure 12 but an additional fan is located above the sample so that the cooling of both sides is equally enhanced. The laser heating, the additional cooling fan and the low thermal inertia of the tested thermal dampers enable to shorten the duration of one cycle to 180 s while keeping the soak times at low and high temperature of 1 minute each, as recommended by the JESD22-A104 standard.

The developed test bench enables to perform three different tests: laser flash measurements in order to estimate the conductive properties of the sample, heating up and cooling down of the sample in order to estimate its heat storage properties, and thermal cycling in order to assess its reliability. Following section deals with the estimation of the heat storage properties.

3.2 Study of the heat storage capacity

In this section, the first main function of the thermal damper consisting in storing thermal energy in the form of latent heat is studied.

3.2.1 Response of the thermal damper facing a crenel-type heat flux

The influence of the PCM on the thermal behavior of the thermal damper facing a crenel-type heat flux is experimentally studied with two samples: one with PCM and one without PCM (table 2). Because of a deeper cavity, the mass of the sample containing PCM is equivalent to the mass of the empty sample, so that their thermal capacities are similar when no phase change occurs.

Table 2: Samples for the heat storage study.

Sample	Full damper		Cavity	
	Dimensions	Mass	Area	Depth
PCM	20 x 20 mm ²	674 mg	16 x 16 mm ²	149 μm
Air	x 760 μm			101 μm

Both samples are subjected to a laser crenel of 18 s. The heating power absorbed by the sample is around 3.2 W. The mean temperature T_m of the sample is estimated by infrared thermography by means of small painted areas located on both sides of the sample (left picture in figure 10). It is defined as the mean temperature of the front and back silicon chips T_f and T_b weighted by their respective masses m_f and m_b , the other masses (PCM, thin layers, paint) being neglected here:

$$T_m = \frac{m_f T_f + m_b T_b}{m_f + m_b} \quad (19)$$

The temperature profiles of both samples are compared in figure 13. At the beginning of the laser crenel, from 20 °C to 60 °C, the increase of the temperature T_m is similar for both samples. This is due to their similar thermal capacity as well as to their similar external dimensions and radiative properties which means similar absorbed heat flux from the laser and similar heat flux evacuated towards the environment by heat radiation, convection and conduction.

From 60 °C to 90 °C, the PCM is melting and thus absorbs a part of the incoming heat flux through its latent heat of fusion. The fusion of the PCM slows down the temperature increase of the thermal damper in comparison to the reference sample without PCM. Despite the low mass fraction of PCM for this prototype sample (2.4 %), the maximum temperature reached at the laser stop ($t = 18$ s) is about 5 K lower than that of the reference sample without PCM. Once the laser stops ($t = 18$ s), both samples cool down due to the convective and radiative heat transfers with the environment. The freezing of the PCM releases heat and thus decreases the speed of cooling of the sample containing PCM. The comparison of the slope of the temperature evolution at a given T_m for both samples enables to identify the temperature range of the phase change during both the heating and the cooling of the sample. It also shows the amplitude of supercooling of the PCM: the start of solidification (82 °C) is 8 K lower than the end of fusion (90 °C). As predicted in section 2.3, the effect of the temperature glide during the phase change is of great importance and has to be taken into account when designing a thermal damper.

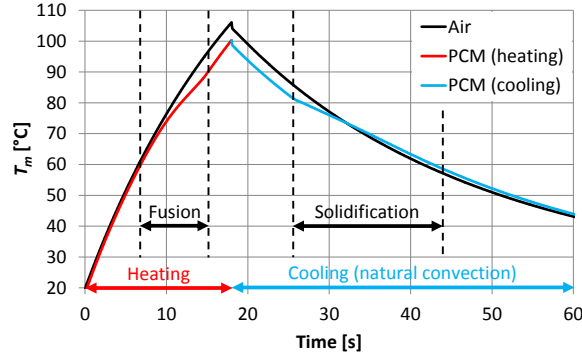


Figure 13. Temperature history of prototype thermal dampers with and without PCM.

3.2.2 Estimation of the latent energy storage

The total apparent thermal capacity of the sample $(mc_p)_{tot}$ including the standard thermal capacities (sensible heat) and the equivalent thermal capacity due to the phase change (latent heat) can be estimated based on the measured temperatures and their derivatives. It is assumed that:

- The temperature of the sample is uniform and equal to T_m .
- The temperature of the ambience (enclosure, air, sample holder) T_{amb} is constant.
- The radiative, convective and conductive heat transfer between the sample and its environment are included in a global thermal conductance G_{env} depending only on T_m and not on the time.

The energy balance of the sample located in the test bench is then:

$$(mc_p)_{tot} \frac{dT_m}{dt} = Q_{abs} - G_{env}(T_m - T_{amb}) \quad (20)$$

with Q_{abs} being the laser flux absorbed by the sample. Both samples have similar external dimensions as well as similar envelopes in terms of materials (silicon, paint) and thus similar radiative properties. For a given sample temperature T_m , it leads to a similar absorbed laser power (Q_{abs}) and a similar global thermal conductance (G_{env}). For a given sample temperature T_m , the storage term of equation (20) is then similar for the sample with PCM and the sample without PCM:

$$\left[(mc_p)_{tot} \frac{dT_m}{dt} \right]_{with\ PCM} = \left[(mc_p)_{tot} \frac{dT_m}{dt} \right]_{without\ PCM} \quad (21)$$

Equation (21) is valid during the heating phase but also during the cooling phase when $Q_{abs} = 0$ for both samples. The derivatives dT_m/dt of both samples are computed from the measurements and the total thermal capacity of the sample without PCM $(mc_p)_{tot}$ is known. The estimated total apparent thermal capacity of the sample with PCM is presented in figure 14. The one estimated during the heating phase (fusion of the PCM) differs from the one estimated during the cooling phase (solidification of the PCM) because of supercooling. Out of the temperature range of phase change, these thermal capacities are similar to that of the sample without PCM ($\approx 0.5 \text{ J K}^{-1}$).

A baseline corresponding to the thermal capacity that the sample would have with a null latent heat can be calculated, as for Differential Scanning Calorimetry (DSC) analysis. In figure 14, the baseline of the sample with PCM is similar to the thermal capacity of the sample without PCM. In the general case of two samples with two different thermal capacities out of the phase change range, the baseline is computed by interpolation of the thermal capacity out of the phase change range. The integration of the difference between the thermal capacity and its baseline gives the estimated quantity of heat involved in the phase change of the entire PCM. For the tested sample, the estimated quantity of latent heat is 3.2 J for the fusion curve as well as for the solidification curve. Considering the latent heat of fusion of the PCM measured by DSC ($200\text{-}210 \text{ J g}^{-1}$), the estimated mass of embedded PCM is about 15-16 mg. Depending on the tested sample, the quantity of stored latent heat ranges from 1.2 to 4.1 J, which corresponds to a mass of PCM ranging from 6 to 20 mg. The highest corresponding latent energy storage density is 1.6 J cm^{-2} , which is 20 times higher than the system presented by Muratore et al. [25].

The robustness of the estimation method presented above was checked by means of two distinct measurements. Firstly, the estimated masses of PCM are consistent with the masses of PCM directly weighted during the assembly of the samples (typical difference $< 5\%$). Secondly, the estimated total apparent thermal capacities are close to DSC measurements of the sole PCM (figure 14). One can note that the supercooling effect is similar for both the DSC measurements and the measurements on our test bench, which is consistent with the fact that the quantity of PCM is of the same order of magnitude in both cases. Further measurements showed that the amplitude of supercooling is of the same order of magnitude for samples containing no CNT, undensified CNTs or densified CNTs.

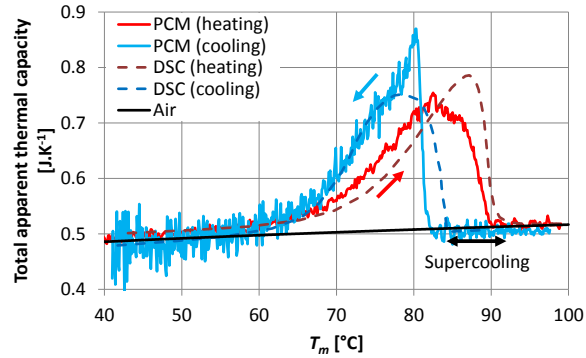


Figure 14. Estimated total apparent thermal capacity $(mc_p)_{tot}$ of the samples with and without PCM versus DSC measurements (DSC curves = baseline of the thermal damper + latent capacity of the PCM measured alone by DSC).

3.2.3 Thermal cycling of the heat storage function

A sample containing composite CNT/PCM material is subjected to a full thermal cycling test as described in 3.1.3 in order to study the evolution of the heat storage capacity of the thermal damper facing thermal aging. Figure 15 displays the quantity of latent heat estimated with the method presented in section 3.2.2 with respect to the number of fusion/solidification cycles of the PCM. The dispersion of the values is due to the uncertainty of the measurement which is amplified by the low quantity of PCM embedded in the tested sample. Nevertheless, figure 15 shows that there is no significant evolution of the latent heat storage. One can conclude that the latent heat storage function of the thermal damper is preserved after 850 thermal cycles.

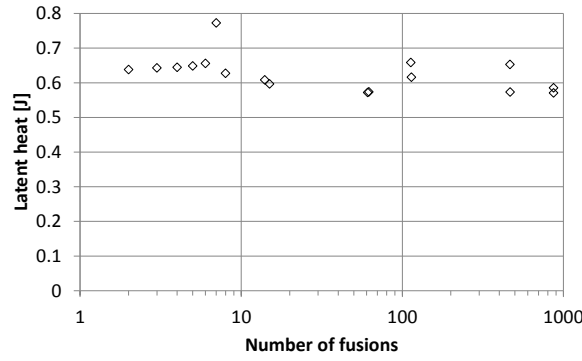


Figure 15. Latent heat storage capacity of the CNT/PCM material as a function of the number of fusion/solidification cycles.

3.2.4 Analysis of the damping effect of the PCM

The theoretical study presented in the first part of this paper showed that the effectiveness of the PCM embedded in the thermal damper is strongly dependent upon the amplitude and frequency of the heat flux generated by the electronic component. As an illustration, figure 16 shows the effectiveness of the damping effect of the PCM embedded in the sample containing the highest estimated mass of PCM for different heat fluxes and assuming an ideal behavior of the thermal damper. The embedded PCM is well suited to damp heat fluxes of frequency f around 0.1 Hz and of amplitude δq around 0.1 W cm^{-2} .

From this point in figure 16, the increase of f decreases the damping effect of the PCM: for a high frequency ($f = 10 \text{ Hz}$; $\delta q = 0.1 \text{ W cm}^{-2}$), the temperature variations of the electronic component are still damped ($G \approx 0$) but this is due to the low-pass filter behavior of the materials and not to the phase change of the PCM ($G_0 \approx 0$).

The decrease of f also decreases the damping effect of the PCM: for a low frequency thermal flux ($f = 0.01 \text{ Hz}$; $\delta q = 0.1 \text{ W cm}^{-2}$), the energy contained in a half period of the thermal flux is much higher than the energy of phase change of the embedded PCM ($N_{mhs} = 0.64$) so that the temperature variations are not damped ($G \approx G_0 \approx 1$). In this case, a higher quantity of PCM (higher N_{mhs}) would enhance the damping effect of the PCM and thus the attenuation of the temperature variations of the whole thermal damper.

An increase of the amplitude of the thermal flux δq decreases the damping effect of the PCM. This could be compensated by an increased quantity of embedded PCM in order to keep the ratio $m_{PCM}/\delta q$ constant, so that the energy contained in a half period of the thermal flux is similar to the energy of phase change ($N_{mhs} \approx 2$).

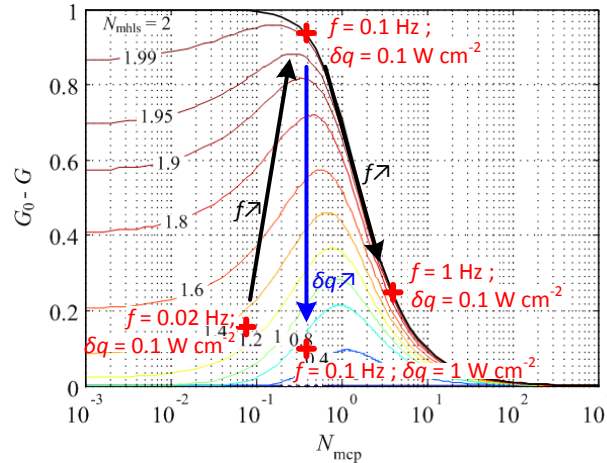


Figure 16. Theoretical assessment of the damping effect of the PCM of the sample with the highest mass of PCM for different combinations of frequency f and amplitude δq .

The benefit of the embedded PCM is summarized for the sample containing the highest mass of PCM: for a temperature variation of 50 K, e.g. for a heating from $50 \text{ }^\circ\text{C}$ to $100 \text{ }^\circ\text{C}$, the sensible heat stored (silicon, PCM...) is 25.5 J and the heat stored in latent form is 4.1 J. This corresponds to an increase of 16 % of the thermal storage capacity of the system with a mass fraction of PCM of only 3 %.

The PCM has to be associated with a conductive structure in order to let the heat flow from the heat source to the heat sink when the thermal damper is located in between. The thermal resistances associated to this conductive structure are studied in following section.

3.3 Study of the heat conduction performance

In this section, the second main function of the thermal damper is studied: it consists in conducting heat efficiently through the system by means of the CNT array. The total thermal resistance between both silicon chips is estimated and analyzed and its sensitivity to some processing features is examined.

3.3.1 Estimation method of the total thermal resistance

The total thermal resistance R_{ff} between both silicon chips of the thermal damper is estimated by combining experimental results with an analytical model of the system. The experiment is inspired by the flash method initially developed by Parker et al. [30]. A pulse of radiant energy is emitted towards the front face of the sample with the laser and the temperature history of the back face is recorded with the IR camera (figure 12). Figure 17 shows a typical temperature history of the back side of a thermal damper (external dimensions of $20 \times 20 \times 0.77 \text{ mm}^3$, total mass of $662 \text{ mg} + 4 \text{ mg}$ paint). The area of measurement is restricted to the central region where the temperature rise is uniform so that the border effects (sealing region) are not taken into account. The characteristic time $t_{1/2}$ is defined as the time required for the back side to reach half of the maximum temperature rise.

Paint is not required when the thermal damper includes a bonding interface (thin layers of Ti/Au/In) on the back silicon chip because it was observed that it is opaque in the wavelength range of the IR camera. Moreover, it is assumed that the temperature of the bonding layers is equal to that of the related silicon chip. The IR camera is thus facing an opaque material (semi-transparent back silicon chip + opaque bonding interface) of unknown emissivity. The temperature rise of the tested samples is low enough ($< 0.2 \text{ K}$) so that the variation of radiance is proportional to the variation of temperature. Thus, the emissivity of the back side is not required since characteristic times like $t_{1/2}$ can be determined directly from the radiance history, as it is shown in figure 17. The temporal profile of the laser solicitation is a crenel of 10 ms which is short enough to be considered as a flash solicitation and long enough in terms of absorbed energy and thus of low signal/noise ratio.

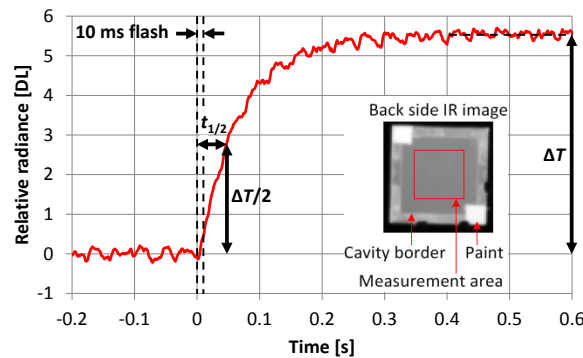


Figure 17. Measured temperature history of the back side of a prototype thermal damper subjected to a 10 ms laser crenel (DL: digital level of the IR camera). Picture: IR image of the sample uniformly heated above the ambient temperature.

The analytical model of the thermal damper consists of two silicon chips of masses m_f and m_b , of thermal capacities $(mc_p)_f$ and $(mc_p)_b$ and linked by a thermal resistance R_{ff} (figure 18). The source Q_{abs} corresponds to the absorbed laser power. The intrinsic thermal resistances of the silicon chips are assumed to be zero, as well as the thermal capacity of the CNT array. Following additional assumptions are made:

- The initial sample temperature ($t < 0$) is equal to the ambient temperature.
- The duration of the laser flash is negligible so that the energy pulse is absorbed instantaneously and uniformly by the front side at $t = 0$.
- The thermal damper is an adiabatic system after the flash ($t > 0$). This assumption is confirmed by the slow temperature decrease of the sample after the end of the temperature rise ($\approx -0.005 \text{ K s}^{-1}$).
- The thermal structure of the thermal damper is 1D: edge effects are neglected and the local thermal resistances between both silicon chips are uniform.
- The temperature of each silicon chip is uniform. This is the case if the previous assumption is verified and if the absorbed laser flux is uniform.
- Half of the mass of the materials located between both silicon chips (sealing, PCM...) are attributed to the front mass m_f , half to the back mass m_b .

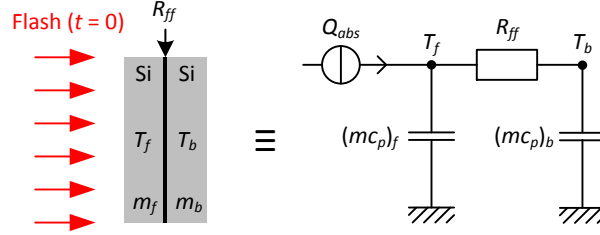


Figure 18. Thermal model of the thermal damper subjected to a laser flash.

The analytic resolution of the temperature history of the back silicon chip T_b gives the following relation between the characteristic time $t_{1/2}$ and the parameters of the thermal model:

$$R_{ff} = \frac{t_{1/2}}{0.693 c_{p,si}} \left(\frac{1}{m_f} + \frac{1}{m_b} \right) \quad (22)$$

The thermal resistance per unit area can be calculated as:

$$r_{ff} = R_{ff} S_{eff} \quad (23)$$

S_{eff} is the effective area of the CNT array. It is defined as the macroscopic area occupied by the CNT array considering neither the void between CNTs nor the influence of the densification process.

The estimation method of r_{ff} presented above is very simple and it is precise enough for the samples tested in this study. Nevertheless, the relative error on the estimated resistance r_{ff} increases with decreasing $t_{1/2}$ because it is assumed that energy is absorbed instantaneously at time $t = 0$. For samples exhibiting a rise time $t_{1/2}$ getting close to the duration of the laser flash (10 ms), a numerical model should be used instead of the analytical model in order to take the duration of the laser crenel into account.

3.3.2 Thermal resistance of thermal dampers compared to literature

The total thermal resistance of six samples is estimated with the method described in 3.3.1. Their main features are summarized in table 3. Three samples (*A*, *B*, *C*) feature an undensified CNT array with a catalyst interface (Si/Al₂O₃/Fe/CNT) and a bonding interface (Si/Ti/Au/In/Au/Ti/CNT). The three others (*D*, *E*, *F*) feature a densified CNT array with two bonding interfaces. Indeed, a previous study showed that the bonding interface seems to have a better potential in terms of heat conduction than the catalyst interface [31].

Table 3: Specifications of the samples considered for the thermal resistance estimation.

Sample	CNT length before assembly	CNT densified	Si/Si distance	Si/CNT interfaces	
<i>A</i>	Unknown	No	100 μm	catalyst + bonding	
<i>B</i>					
<i>C</i>					
<i>D</i>	Unknown	Yes	160 μm	bonding + bonding	
<i>E</i>					200 μm
<i>F</i>					210 μm

Figure 19 shows the estimated total thermal resistances of the thermal dampers of table 3 as well as those of CNT arrays reported in the review article of Marconnet et al. [15]. Samples *D*, *E* and *F* exhibit a lower thermal resistance than samples *A*, *B* and *C*. This might be due to the densification of the CNT array which enhances the mechanical strength and thus the mechanical interaction between the CNT and the bonding layer and/or due to the double bonding of the CNT array. The lowest total thermal resistance per unit area of CNT array was measured for sample *F* and it is equal to $8 \times 10^{-5} \text{ m}^2 \text{ K W}^{-1}$. The estimated values for the samples of the present study are consistent with the values reported in [15] even if the total thermal resistances of the best samples are two orders of magnitude higher than those of the best systems. However, the best samples of the present study exhibit the lowest total thermal resistance among systems with CNTs longer than 60 μm .

Note that the intrinsic thermal resistances l_{si}/λ_{si} of the individual silicon chips of the tested samples range between $10^{-6} \text{ m}^2 \text{ K W}^{-1}$ and $4 \times 10^{-6} \text{ m}^2 \text{ K W}^{-1}$ (individual thickness from 150 μm to 550 μm), which is at least one order of magnitude lower than the lowest measured total thermal resistance r_{ff} . So the intrinsic thermal resistance of the silicon chips is negligible along the thermal flux direction and the estimated total resistance r_{ff} corresponds to the sum of both interfacial thermal resistances Si/CNT and of the intrinsic thermal resistance of the CNT array.

The dashed line in figure 19 shows that the experimental thermal resistances are much higher than the theoretically achievable ones. Possible explanations to this statement are given by Marconnet et al. [15]: imperfection of the CNTs themselves (reduction of the transport of phonon because of defects and impurities in the lattice of CNTs and because of CNT/CNT interaction) and substantial thermal resistance at the Si/CNT interfaces (fraction of CNT connected to the silicon lower than 1, theoretical limitation of the phonon transmission between the bulk substrate and the almost 1D CNT).

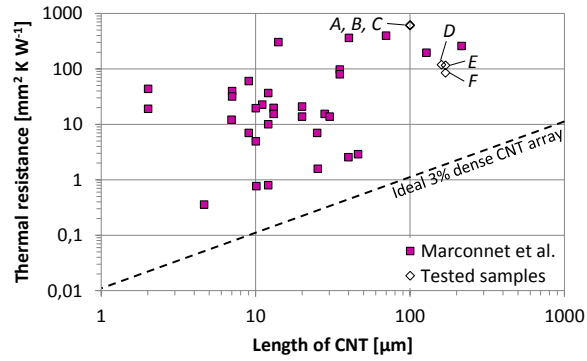


Figure 19. Estimated total thermal resistance of the studied samples compared to those of the CNT arrays reported in the review article of Marconnet et al. [15]. The total thermal resistance includes both interfacial thermal resistances CNT/substrate at both ends of the CNT array plus the intrinsic thermal resistance of the CNT array. The dashed line shows the thermal resistance of an ideal CNT array at a packing density of 3 %, with zero interfacial thermal resistances and with each individual CNT having a thermal conductivity of $3000 \text{ W m}^{-1} \text{ K}^{-1}$.

Figure derived from [15].

3.3.3 Sensitivity analyses of the total thermal resistance

Sensitivity to the bonding parameters

The aim of this sensitivity analysis is to identify the bonding parameters (temperature, pressure and duration of the pressing step) leading to a low thermal resistance. Each bonding parameter is set to two possible values, leading to eight possible combinations. Two similar sets of eight samples each were fabricated by the CEA: one for the mechanical tests and one for the thermal tests.

These samples include a catalyst interface and a bonding interface. The silicon chips of these samples are linked only by the CNT array since they contain neither PCM nor sealing material. Therefore, the total thermal resistance of these samples corresponds to that of the Si/CNT/Si structure alone. The fabrication of the samples, the mechanical tests and the results for a part of the samples as well as a structural analysis of the interface material are presented by Ollier et al. [26]. It emerges from the mechanical and thermal tests that the total thermal resistance per unit area r_{ff} decreases with increasing assembly pressure as well as with increasing assembly temperature. Furthermore, a low thermal resistance is correlated with an increasing breaking force of the Si/CNT/Si samples during the pull-off test and with an increasing transfer rate of the CNT to the bonding interface after the pull-off test. Conversely, the duration of the pressing step seems to have no influence on the thermal resistance.

Only one sample does not follow the correlation between thermal and mechanical performances. This might be due to the reproducibility of the fabrication process between both sets of samples. More test samples would give a better statistical weight to these results. However, these results show that the bonding parameters and thus the quality of the bonding between the CNT and the silicon coated with the bonding layers Ti/Au/In impact drastically the total thermal resistance r_{ff} and consequently the interfacial thermal resistance at the bonding interface.

Sensitivity to the length of CNTs

The thermal conductivity of the CNTs of this study is unknown. The thermal conductivities of individual CNTs reported in the literature do not give indication since they span a very large range from $34 \text{ W m}^{-1} \text{ K}^{-1}$ to $13350 \text{ W m}^{-1} \text{ K}^{-1}$ [15]. Consequently, a sensitivity analysis is performed in order to evaluate the significance of the intrinsic thermal resistance of the CNT array as a part of the total thermal resistance r_{ff} . To do this, four samples with four different lengths of CNT were manufactured by the CEA with 11, 46, 93 and 133 μm before bonding. These samples and the fabrication process are similar to those previously described: both silicon chips are linked by the CNT array only and the samples are fully painted. So these four Si/CNT/Si samples are similar except the length of CNT.

The half-rise times $t_{1/2}$ measured on the back side of the samples are 76, 51, 44 and 51 \pm 5 ms for the respective CNT lengths of 11, 46, 93 and 133 μm . The given uncertainty corresponds to the reproducibility of the measurement. The corresponding estimated total thermal resistances r_{ff} are plotted in figure 20. There is clearly no correlation between the length of CNT and r_{ff} . Since the intrinsic thermal resistances of silicon and paint are the same for all samples, this result shows that the intrinsic thermal resistance of the CNT array is negligible in comparison to the sum of both serial interfacial thermal resistances Si/CNT.

As a conclusion, the total thermal resistance of the studied thermal dampers can be considered as the sum of both interfacial thermal resistances Si/CNT. Even for the samples featuring two bonding interfaces, the values of total thermal resistance measured in 3.3.2 show that there is still a potential of optimization of the interfacial thermal resistances Si/CNT, which should be confirmed by further studies.

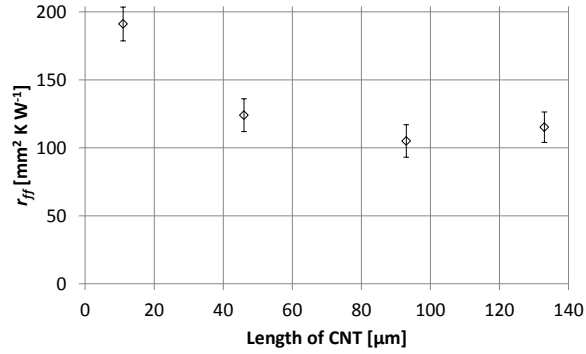


Figure 20. Total thermal resistance of Si/CNT/Si samples with various lengths of CNTs.

4 Conclusion

In this paper, the concept of ideal thermal damper was firstly developed to define the area of use of this device and especially its response to thermal solicitations of various amplitudes and frequencies. The frequency analysis and the impedance calculation enabled to calculate the gain and the cut-off frequencies of the corresponding low-pass filter. This approach is of great interest for systems where the PCM is directly embedded in the substrate as the sensible heat of the system is not negligible compared to the latent heat of the PCM. A supplementary numerical model showed the strong influence of the temperature glide of the phase change material and of the thermal resistance at the junction between the CNT and the casing on the overall thermal performance of the system. Contrarily to thermal dampers consisting of a finned heat sink filled with PCM, the heat diffusion in the PCM is not an issue thanks to the small dimensions of the cells containing the PCM.

Then, various prototypes of thermal damper were thermally characterized by means of flash measurements, crenel heating and thermal cycling tests. An estimation method was developed in order to access the total apparent thermal capacity including the phase change effect with respect to temperature. For the best sample, the stored latent heat was equal to 4.1 J, which corresponds to a latent thermal storage density of 1.6 J cm^{-2} , which is 20 times higher than the system presented by Muratore et al. [25]. PCM enables an effective increase of the thermal inertia per unit of volume equal to 16 % with a mass fraction of PCM as low as 3 %. The observed amplitude of supercooling is similar to that of the sole PCM measured in a DSC apparatus. The latent heat storage property of the thermal damper was preserved after 850 thermal cycles oscillating between $25 \text{ }^\circ\text{C}$ and $125 \text{ }^\circ\text{C}$.

A simple parameter estimation method was developed in order to quantify the total thermal resistance of the thermal damper. The estimated values of the total thermal resistance of tested thermal dampers are consistent with those reported in literature for comparable systems. Sensitivity analyses confirm that the contact thermal resistances at the interfaces between the CNT array and the silicon chips are dominant compared to the intrinsic thermal resistances of the CNTs and of the silicon.

As a next step, the latent thermal storage density could be increased with a PCM filling rate of the cavity higher than the 60 % achieved in this study, with a cavity deeper than $150 \text{ } \mu\text{m}$ and with a PCM of higher latent heat. Thermal dampers including optimized Si/CNT interfaces might enable to further decrease the total thermal resistance of the system.

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Appendix 1: Thermal impedance of an ideal thermal damper

The temperature of an ideal thermal damper experiencing a sinusoidal heat flux is developed in this appendix. The transient part of the imposed heat flux is equal to:

$$q_t(t) = \delta q \cos(2\pi f t + \varphi) \quad (24)$$

Figure 21 presents q_t and the transient part of the heat flux transferred to the PCB q_{PCB} :

$$q_{PCB} = h_{ref}(T - T_m) \quad (25)$$

In this figure, time $t = 0$ corresponds to the end of the melting, time $t = -t_0$ to the maximum of q_t and time $t = t_2$ to the start of the freezing (figure 21). Only half of a period is considered in the present analysis. The second part can then be deduced by symmetry.

Between $t = 0$ and t_2 , there is no phase change and the energy balance can be written as:

$$\frac{(mc_p)_{tot}}{S} \frac{dT^*(t)}{dt} = \delta q \cos(2\pi f t + \varphi) - h_{ref} T^*(t) \text{ for } 0 < t < t_2 \quad (26)$$

with $\varphi = 2\pi f t_0$ and $T^* = T - T_m$. This equation can be written using Laplace transformation:

$$\frac{(mc_p)_{tot}}{S} (p\bar{T}(p) - T^*|_{t=0}) = \delta q \frac{-2\pi f \sin \varphi + p \cos \varphi}{(2\pi f)^2 + p^2} - h_{ref} \bar{T}(p) \quad (27)$$

where \bar{T} is the Laplace transformation of T^* . $T^*|_{t=0}$ being equal to 0, we eventually get:

$$\bar{T}(p) = \frac{\delta q (-2\pi f \sin \varphi + p \cos \varphi)}{\left(\frac{(mc_p)_{tot}}{S} p + h_{ref} \right) ((2\pi f)^2 + p^2)} \quad (28)$$

Using the inverse Laplace transformation, we obtain:

$$T^*(t) = \frac{\delta q}{h_{ref} \sqrt{1 + N_{mcp}^2}} \left(\sin(2\pi f t + \varphi + \alpha) - \sin(\varphi + \alpha) e^{-\frac{2\pi f t}{N_{mcp}}} \right) \text{ for } 0 < t < t_2 \quad (29)$$

with $\alpha = \arctan\left(\frac{1}{N_{mcp}}\right)$ and $N_{mcp} = \frac{2\pi f (mc_p)_{tot}}{h_{ref} S}$.

During the constant temperature period, the stored energy is equal to the latent heat of phase change of the PCM. Thus, we obtain:

$$m_{PCM} h_{ls} = S \delta q \int_{t_2}^{\frac{1}{2f}} \cos(2\pi f t + \varphi) dt \quad (30)$$

Using the non-dimensional parameter $N_{mhlS} = \frac{2\pi f m_{PCM} h_{ls}}{S \delta q}$ and the angle $\psi = 2\pi f t_2$, it leads to the equation:

$$N_{mhlS} = \sin(\varphi) + \sin(\psi + \varphi) \quad (31)$$

This equation is valid only for $N_{mhlS} \leq 2$.

For $N_{mhlS} > 2$, the latent heat of phase change of the PCM is larger than the energy corresponding to half a period of the heat flux variation. As a consequence, the thermal damper temperature is always constant whatever N_{mcp} .

Considering that $T^*(t_2) = 0$, the following equation is also verified:

$$\sin(\psi + \varphi + \alpha) = \sin(\varphi + \alpha) e^{-\frac{\psi}{N_{mcp}}} \quad (32)$$

Equations (31) and (32) form a system of transcendental equations that cannot be solved analytically. However, the variables φ and ψ depend only on N_{mhlS} and N_{mcp} (through α) and can be calculated numerically.

The maximum temperature of the thermal damper is reached for $t = t_1$ and can be found noting that $\left. \frac{dT^*}{dt} \right|_{t=t_1} = 0$. By introducing $\gamma = 2\pi f t_1$, the following equation is verified:

$$N_{mcp} \cos(\gamma + \varphi + \alpha) + \sin(\varphi + \alpha) e^{-\frac{\gamma}{N_{mcp}}} = 0 \quad (33)$$

This equation is also transcendental but γ depends only on N_{mcp} and N_{mhlS} and can be calculated numerically. Eventually, the filter gain can be directly calculated with:

$$G = \frac{h_{ref} \delta T}{\delta q} = \cos(\gamma + \varphi) \quad (34)$$

The evolution of G as a function of N_{mcp} and N_{mhlS} is plotted on figure 3.

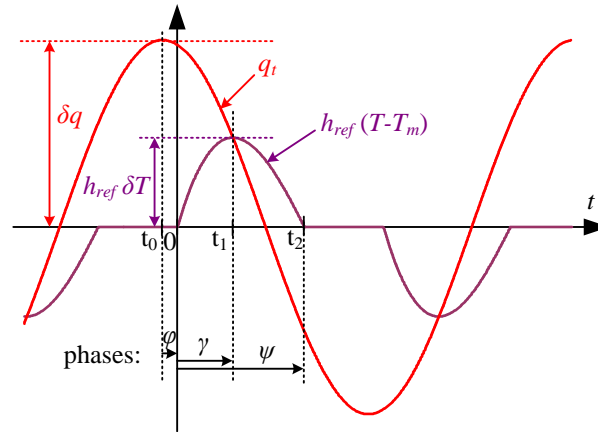


Figure 21: Temporal evolution of the heat flux and the thermal damper temperature

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