Low defect InGaAs quantum well selectively grown by MOCVD on Si(100) 300 mm wafers for next generation non planar devices

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Metal organic chemical vapor deposition of GaAs, InGaAs, and AlGaAs on nominal 300 mm Si(100) at temperatures below 550 °C was studied using the selective aspect ratio trapping method. We clearly show that growing directly GaAs on a flat Si surface in a SiO_2 cavity with an aspect ratio as low as 1.3 is efficient to completely annihilate the anti-phase boundary domains. InGaAs quantum wells were grown on a GaAs buffer and exhibit room temperature micro-photoluminescence. Cathodoluminescence reveals the presence of dark spots which could be asso-ciated with the presence of emerging dislocation in a direction parallel to the cavity. The InGaAs layers obtained with no antiphase boundaries are perfect candidates for being integrated as channels in n-type metal oxide semiconductor field effect transistor (MOSFET), while the low temperatures used allow the co-integration of p-type MOSFET.

Metal oxide semiconductor field effect transistor (MOSFET) scaling has entered in a power constrained phase, as the power density dissipated by logic chips hits 100 W cm^{-2}.[1] A reduction in the operating voltage seems necessary in order to follow the increase of transistor density. One possible solution is to introduce materials with high carriers' velocity like SiGe alloys or III-V materials which have a strong potential to be used for high performance p-MOS and n-MOS devices.[2–6] At the same time, transistor architectures such as trigate,[7] FinFET,[5] gate all-around,[8] or ultra-thin body III-V/OI (Ref. 9) have been developed to improve electrostatic control of the device's channel. Among the variety of III-V compounds, In rich InGaAs channel integrated in different device architectures have shown promising electrical characteristics.[10,11] Nevertheless, there are still challenges to be solved in order to integrate InGaAs channel with fully very large scale integration (VLSI) compatible processes and toolsets. Among these challenges, obtaining a high crystalline quality InGaAs channel is still under consideration. Two main routes are currently under development, the InGaAs layer transfer from a III-V donor substrates,[6] and direct growth of III-V on Si or Ge buffers/Si substrates.

The major challenges in direct III-V epitaxy onto nominal Si(100) substrates currently used in complementary metal oxide semiconductor (CMOS) VLSI processes is to reduce the threading dislocation density coming from a high lattice mismatch (about 4% with GaAs and about 11% with InAs) and the antiphase boundary (APB) density coming from the growth of a polar semiconductor on a non-polar one.[12] As for CMOS applications, the objective is to use very thin III-V layers, a few hundred of nanometers thick, so that the difference in thermal expansion coefficient is not a major issue. Several studies have been done to try to circumvent these questions by employing different strategies such as cycled thermal annealing,[13] epitaxial lateral overgrowth,[14] growth on compositional graded SiGe buffers,[15] insertion of strained layer lattices,[16] insertion of quantum dot dislocation filters,[17] AlSb buffer layers,[18] compliant substrates,[19] and selective growth in trenches using the aspect ratio trapping (ART) method.[20,21] But to date, these methods require the growth of thick III-V buffer layers and/or high thermal budget that may not be acceptable for the co-integration of NMOSFET and PMOSFET processes.

In this paper, we have studied the ART selective epitaxy by metal organic chemical vapor deposition (MOCVD) of GaAs/InGaAs/AlGaAs multilayers in SiO_2 cavity with a limited thickness (<200 nm) and a limited growth temperature (<550 °C). The layers are epitaxially grown on patterned 300 mm Si(100) substrates. We clearly show that within these constraints, single crystalline InGaAs quantum well (QW) exhibiting room temperature photoluminescence can be grown in low aspect ratio cavities ($AR < 2$), on flat nominal Si(100).

The III-As based compound semiconductors were selectively grown in SiO_2 trenches of different widths on (100) oriented 300 mm diameter Si substrates. The growth was performed in a 300 mm Applied Materials MOCVD reactor

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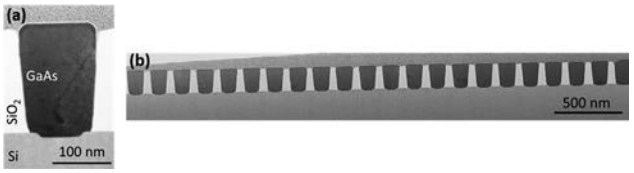

FIG. 1. (a) Cross-sectional STEM image on a single trench, (b) low magnification cross-sectional STEM image of a GaAs layer grown in 140 nm wide SiO_2 trenches on (100)-oriented Si substrate showing a good uniformity of the selective growth. The trenches are oriented along the [011] direction and are 180 nm deep.

using trimethylgallium (TMGa), -aluminium (TMAl), and -indium (TMIn) as group-III precursors, and tertiarybutylarsine (TBAs) as group-V precursor. 200 nm deep SiO_2 trenches aligned along the [110] direction with widths ranging from 100 nm to 1000 nm were patterned on 300 mm Si (100) substrates using standard e-beam lithography and plasma etching. After removing the native oxide by dry NF_3/NH_3 based chemical etching in a Siconi^{TM} preclean chamber, the growth proceeds with a thin GaAs nucleation layer grown at low temperature. Then the temperature was increased to a higher temperature ($<550\,^{\circ}C$) where a stack of GaAs/AlAs/InGaAs/AlAs/GaAs layers was grown. The morphology of the selectively grown layers (mainly affected by APBs) was characterized in top-view by scanning electron microscopy (SEM). The structural properties were characterized in cross-section view by scanning transmission electron microscopy (STEM/TEM) across thin lamellas prepared with FIB (focused ion beam) SEM tool combining focused ion and electron beams. Chemical composition depth profiles were obtained by means of secondary ion mass spectrometry (SIMS) analysis using 1 keV Cs^+ sputtering at 63° to the sample normal. The raster size was $200 \times 200\,\mu m^2$, of which the central area of $44 \times 44\,\mu m^2$ was analysed. Optical properties were investigated by room temperature micro-photoluminescence (μPL) and cathodoluminescence (CL) performed at low temperature (5 K).

Initially, we have studied the selective growth in trenches of pure GaAs layers, which will be used as a buffer layer for further epitaxy of InGaAs QWs. Figure 1(a) shows a typical FIB-STEM image of a GaAs layer grown in the SiO_2 cavity with an aspect ratio of 1.3. In our case, the 300 μm long lines are oriented in the [110] directions. The trenches are 140 nm in width and the SiO_2 thickness is 180 nm. Note that we use a flat Si(100) surface as a bottom nucleation surface and that we directly grow GaAs on Si without any other buffer layers or Si surface structuration. The growth temperature was optimized in order to decrease the (111) faceting and thus get a top flat (100) surface. The GaAs layer thickness thus obtained is highly uniform all over the 300 mm wafer as attested by Figure 1(b). In accordance with the ART principle, a large part of the misfit dislocations initiated at the Si/GaAs interface were blocked by the SiO_2 sidewalls and do not propagate vertically in the GaAs layer. Thus, a low dislocations density is expected in the upper part of the GaAs epilayer. These results are in accordance with those reported earlier by Li *et al.*[20] As it is very difficult to perform plan view TEM to measure the emerging dislocation density, we have chosen to use μPL as an alternative to characterize the material quality at a local scale.

Then, we have studied the influence of the line width and of the AR of the cavity on the APB density ($130 < W < 1000$ nm and $0.2 < AR < 1.3$). Figure 2 shows top view SEM pictures of GaAs selectively grown in SiO_2 trenches with different aspect ratios ranging from 0.2 to 1.3. We have measured the APB density for each cavity width. This density decreases from 3.9 μm^{-1} to 0.25 μm^{-1} for cavities with a width of 1000 nm ($AR = 0.18$) and 300 nm ($AR = 0.6$), respectively. For narrower cavities, APBs are no longer observed. An aspect ratio of 1.3 is sufficient to completely annihilate the APBs. Using the same approach, Loo *et al.* have studied the growth of InP on a thin Ge layer selectively grown on a nominal Si(100) surface in SiO_2 cavities.[22] In their case, the APB density was reduced but not completely suppressed. We propose that selective growth of GaAs directly on Si(100) is an efficient way to suppress completely at least the surface penetrating APBs. The GaAs lines thus achieved within our 90 000 μm^2 (0.09 mm^2) areas have a nearly flat and flawless

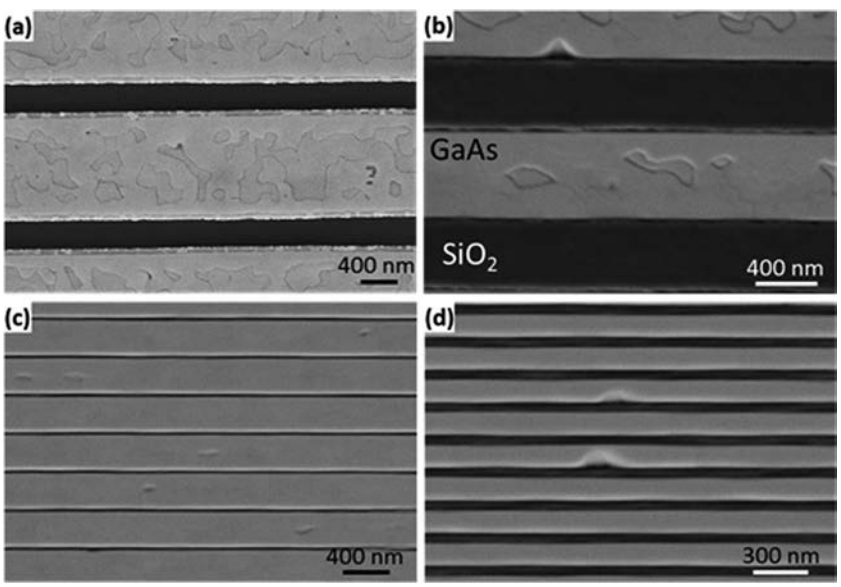

FIG. 2. Top view SEM images of GaAs selectively grown in 180 nm deep SiO_2 trenches with different widths: (a) 1000 nm ($AR = 0.18$), (b) 570 nm ($AR = 0.32$), (c) 300 nm ($AR = 0.6$), and (d) 140 nm ($AR = 1.3$). The APB density decreases when increasing the aspect ratio from: (a) 3.9 μm^{-1}, (b) 1.6 μm^{-1}, (c) 0.25 μm^{-1}, and (d) no APBs.

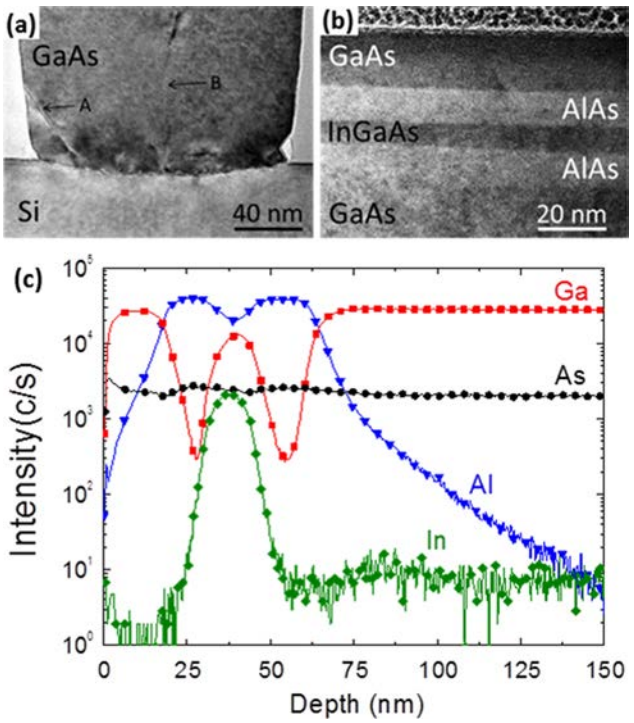

FIG. 3. (a) Cross-sectional TEM image of the bottom part of the cavity showing two structural defects: a stacking fault blocked by the oxide sidewall labeled as A, and a dislocation labeled as B. (b) Cross-sectional TEM image of the top layers showing the stack of GaAs/AlAs/InGaAs/AlAs/GaAs layers with no crystalline defects. (c) SIMS depth profiles of major elements, Ga, As, Al, and In averaged over many trenches.

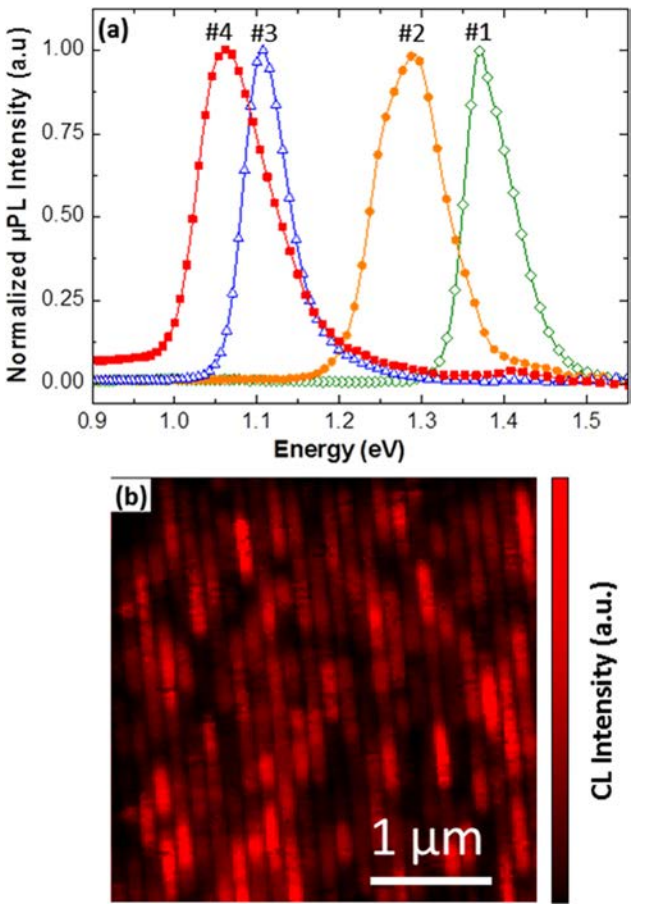

FIG. 4. (a) Normalized room temperature μPL spectra of different InGaAs QWs having different composition of Indium of (#1) 10%, (#2) 20%, (#3) 30%, and (#4) 40%. (b) 5 K panchromatic CL mapping of sample 1.

surface. Furthermore, the SEM images of the patterns with the lowest aspect ratios show an exclusion zone of the APBs. This area is included within a few tens of nanometers from the SiO_2 sidewalls, suggesting that the annihilation mechanisms occurring at the edge of the patterns could be a key point in the removal of APBs. This point needs further investigation to be understood.

The crystalline quality of the GaAs buffer layer was investigated by TEM. Figure 3(a) shows the low magnification cross-sectional TEM image of the bottom part of the cavity. The crystalline defects are localized in the first 20 nm of the GaAs layer. Such defects are generated in the crystal to accommodate the large lattice mismatch (4%) existing between the GaAs layer and Si substrate. Defects are also generated due to the polar/non polar character of this interface. (111) oriented defects such as threading dislocations, twins, and stacking faults (labeled A on Fig. 3(a)) can be trapped on the SiO_2 sidewalls. Sometimes, a few structural defects (labeled B) are observed and propagate through the film. Indeed, they are normal to the growth interface and therefore will propagate to the surface instead of ending on the cavity's sidewalls.

We will now use these GaAs layers as a buffer to grow and study the properties of InGaAs QWs grown in the same cavities with variable aspect ratio. Figure 3(b) shows a cross-section TEM image of the top part of the trench where every layer of the GaAs/AlAs/InGaAs/AlAs/GaAs stack is clearly identified and no crystalline defects are observed. This result emphasizes the efficiency of the ART method which leads to high structural quality material on the top part of the layers.

In order to gain more information on the quality of hetero-interfaces, SIMS measurements were carried out. Figure 3(c) depicts the SIMS depth profiles of major elements (Ga, As, Al, and In) averaged over many trenches (approximately 200 trenches) and reveal quite abrupt interfaces. All profiles appear quite symmetrical with respect to the center of the InGaAs QW indicating that the two AlAs/InGaAs and InGaAs/AlAs interfaces are almost identical in abruptness. As a matter of fact, the quality of these two interfaces can be estimated from the In intensity profile, where the interface width (λ) of both interfaces is defined by the distance over which the In intensity changes from 14% to 86% of its maximum value. We found $\lambda = 2.5$ nm and $\lambda = 2.9$ nm for the upper and the lower interface, respectively.

Investigation of InGaAs quality was done by room temperature μPL measurements on the GaAs and on the InGaAs QW structures (Fig. 4(a)). The excitation was provided by a continuous wave He-Ne laser beam (632.8 nm) focused by a microscope objective to a spot size of about 5 μm. The PL emission was collected by the same microscope objective and sent to a monochromator equipped with a nitrogen cooled InGaAs photodiode array detector. First of all, all the patterns which still exhibit APBs do not show any μPL signal (AR < 1.3). We thus focused our measurements on patterns with AR $= 1.3$ corresponding to Figure 2(d). For pure GaAs, one peak centered at 1.43 eV which corresponds to the GaAs band-to-band emission was observed. The full-

TABLE I. Characteristics of the samples studied in this work by μPL.

	Targeted In content (%)	Measured InGaAs thickness (nm)	μPL peak energy (eV)	FWHM (meV)	Extracted In content (%)
Sample 1	10	15	1.37	68	7
Sample 2	20	13	1.29	95	16
Sample 3	30	10	1.10	60	35
Sample 4	40	8	1.06	100	42

width at half-maximum (FWHM) is about 50 meV. But the μPL intensity is quite low compared to that of InGaAs QW. Indeed the structure is not optimized for light emission, and nothing is done to prevent non radiative recombination at the defective GaAs/Si interface or at the oxidized GaAs surface. Then, InGaAs QWs with different In content and QW thicknesses were characterized. The QW parameters are presented in Table I. For each sample, a single peak is observed and as expected its position varies with In content and thicknesses (Fig. 4(a)). For 10% In targeted the position is centered at 1.37 eV, whereas for 40% In targeted it is centered around 1.06 eV. The QWs thicknesses were measured by STEM and knowing the peak position, we can calculate the exact In composition. Very close values to the ones targeted were found (see Table I). The calculation is performed using the 3D nano device simulator "Nextnano."[23] The investigated structure is a 1D GaAs/AlAs/InGaAs/AlAs/GaAs heterostructure where all the layers are grown pseudomorphically on GaAs. The QW ground state energy is determined with the single-band effective mass approximation. The value of the FWHM is also measured and is around 60 meV. The enlargement of the FWHM comes from an averaging on QWs grown inside dozen of lines ($5\,\mu m \times 5\,\mu m$ laser spot) and indicates the good QW quality. The ART strategy combined with an ultra-thin 150 nm GaAs buffer layer seems efficient to block most of the defects such as dislocations and antiphase boundaries. It has been shown that an aspect ratio of 2 is required to effectively suppress the defects in selective epitaxy.[22] But even in our below 1.5 aspect ratio patterns, defect densities are strongly decreased leading to a room temperature photoluminescence. This demonstrates that single InGaAs QW selectively grown on a 150 nm GaAs buffer layer directly on flat Si(100) surface produces high quality materials. μPL is very powerful characterization technique to access to the global quality on the InGaAs QWs but the observation of local defects is not possible.

For the purpose of observing those localized defects, we have used low temperature top-view CL to observe InGaAs QW in individual lines for sample 1. The luminescence was collected using scanning electron microscope (SEM) with an integrated light microscope. The light microscope is embedded within the electron objective lens so that their fields of views match. The spatial resolution conferred by this technique allows us to image the luminescence along the lines. All the wavelengths have been detected with a CCD camera, and the total intensity of the signal is measured. The measurement can be seen in Figure 4(b). Bright zones correspond to luminescent areas, whereas dark ones correspond to non-luminescent areas. As APBs are not present in our smallest cavity, we can assume that emerging dislocations in the direction of the patterned line are not completely blocked and could go through the whole sequence of layers. These dislocations are known as non radiative recombination centers[17] and could explain the presence of dark zone in the CL measurements. This measurement in complement of μPL is very useful as it reveals the presence of non radiative centers. Further work is in progress to adapt the cavity aspect ratio and size, and the growth parameters, in order to block the remaining defects and to form defect free QWs.

In conclusion, we have studied the selective growth of GaAs/AlAs/InGaAs/AlAs/GaAs/Si multilayers using the aspect ratio trapping technique in SiO_2 cavities on 300 mm substrates. We have demonstrated that growing a thin GaAs buffer layer directly on nominal flat Si(100) in cavities with width of 130 nm and an aspect ratio of 1.3 is an efficient way to eliminate the APB defects. Room temperature micro-photoluminescence signal was obtained for InGaAs QWs of different composition for a total thickness of deposited III-V of 180 nm and with a growth temperature below 550 °C. Those results are promising for the realization of NMOSFET with InGaAs channel with the co-integration of PMOSEFT with Ge based channels due to the low temperatures used to grow InGaAs channels.

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