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## Spurious phenomena occurring during current measurement on ultra-thin dielectric layers: From electro-thermal effects to surface damage

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In this paper, the conduction properties of dielectric ultra-thin layers are studied using atomic force microscopy. Especially, the conductive-atomic force microscope allows to measure the leakage current at the nanoscale and to study the degradation mechanisms locally. Nonetheless, the dielectric layer seems to be damaged by a technique's specific phenomenon: hillocks appear when a positive tip bias is applied on different dielectrics. In this paper, the formation of these hillocks is studied. Contrary to what is observed during the dielectric breakdown, the conductivity is reduced after hillocks formation which occurs after the dielectric breakdown. Moreover, we have observed the formation of cavities in the silicon substrate linked to the formation of hillocks, which is not compatible with a swelling process (as dielectric breakdown induced epitaxy). We propose that these results may be explained by an electro-thermal effect due to the large dissipated energy, maybe combined with the oxidation of the substrate. Finally, the interdependence of measurements is demonstrated during serial acquisition.

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### I. INTRODUCTION

Thin dielectric layers are essential components in microelectronic devices and the study of the mechanisms which govern dielectric breakdown provides crucial information about their reliability and life-time. The continuous progression of the devices integration requires to replace SiO<sub>2</sub> layers by new materials with larger dielectric constant, so called “high-k” materials. Classically, the leakage current and the oxide degradation (and breakdown) are studied at the device scale. However, it has been shown<sup>1-3</sup> that these phenomena take place at the nanometer scale. Therefore, more and more investigations are carried out with a nanometric resolution with techniques derived from the atomic force microscope (AFM) like Conductive-AFM (C-AFM). It is possible to perform Intensity-Voltage (I-V) measurements locally and make maps of localized leakage current. Leakage current mapping allows a comparison of the current level with topographic maps obtained simultaneously. For example, some studies have shown that in certain cases the leakage current appears at the grain boundaries.<sup>1</sup> Time dependent dielectric breakdown studies (TDDDB) with the C-AFM tip used as nanoscale electrode can also be performed.<sup>4</sup> Using AFM allows to simplify the experimental set-up and to highlight different breakdown modes when the dielectric layer is not homogeneous (thickness, defect density and distribution, stoichiometry.).

A lot of results available in the literature were obtained in ambient atmosphere. In this case, a water layer exists on the sample surface and a meniscus appears at the tip-sample contact.<sup>5</sup> These experimental conditions are different from a macroscopic experimentation where the oxide layer is protected by the large size electrode. In the case of AFM measurements, on the one hand, the water meniscus determines the effective electrical contact area. On the other hand, this water layer can also be at the origin of electrochemical

effects: dissociation of water molecules by the electric field and injection of ions in the sample.

When a negative bias is applied to the AFM tip relatively to the substrate, some OH<sup>-</sup> ions may be injected through the oxide layer, inducing silicon substrate oxidation. Then an hillock appears on the stressed area.<sup>6</sup>

When the bias applied to the tip is positive (or the bias applied to the backside of the sample is negative), OH<sup>-</sup> ions cannot to be injected through the oxide layer, so the substrate oxidation must be impossible. Nonetheless, a hillock is observed too.<sup>3</sup>

The first proposed explanation is that the observation of a sample surface inflation is only due to injection of electric charges in the dielectric which influences the topographical mapping.<sup>7</sup> The second theory supposes a phenomenon similar to dielectric breakdown induced epitaxy (DBIE) where the substrate atoms migrate in the charge carriers direction under the action of heating.<sup>8</sup> It has been proven that, the first theory is not sufficient to fully explain observation of the hillock.<sup>9</sup>

In this paper, we propose a theory that allows a better understanding of mechanisms that induce the apparition of hillocks under positive AFM bias relatively to the substrate.

### II. EXPERIMENTS

Experiments were performed using a Dimension 3100 AFM from Veeco (now Bruker) with TUNA 2 module which allows to measure currents from a few tens of fA up to 1 μA through four ranges. A NT-MDT Ntegra AFM was used too. All experiments have been performed in air and at room temperature.

In this study, the sample is a thermal SiO<sub>2</sub> grown on a n-type (10<sup>18</sup> cm<sup>-3</sup>) substrate. The dielectric layer thickness is 4.2 nm. We have chosen to work on such a very simple system in order to take advantage of its well controlled

growth conditions, so that we dispose of a homogeneous layer with certified properties, and with minimal amount of defects. Nonetheless, note that abnormal hillocks have been already observed on different dielectrics.<sup>10,11</sup>

The electrical stress is obtained by applying a bias ramp on the backside of the sample, which is defined by the voltage range, the number of measurement points, and the voltage sweep rate. The current is measured in order to obtain Intensity-Voltage (I-V) curves. These parameters play a role on the noise level and the sample's stress. In order to use similar conditions in different experiments, voltage sweeps are applied to the backside of the sample from 0 V to  $-10$  V. The voltage sweep rate is  $0.5 \text{ V s}^{-1}$ . Parameters of backward voltage sweep (from  $-10$  V to 0 V) are the same. To adjust the electrical stress level, in some cases the current level is limited by a current compliance: as soon as the current reaches the limitation value, the current sweep is stopped and the bias is switched down to 0 V. The sweep rate is also  $0.5 \text{ V s}^{-1}$ .

C-AFM characterization of oxide layers requires a lot of measurements because the results have to be interpreted statistically. That is why, in our studies, series of 25 independent curves are automatically obtained on a 25 points matrix. Measurements on 3 identical samples, denominated A, B, and C, are presented in this paper. More specific details will be given in Sec. III.

### III. TOPOGRAPHIC ASPECTS

A first set of measurement has been obtained on sample A with the 100 pA range. With this range, it is possible to detect a small current (few tens of fA) in order to identify the conduction mechanisms at moderate bias voltage. Furthermore, a few pA current compliance can be applied. Yet, the electrometer is easily saturated.

Three series of 25 voltage ramps have been performed on three different areas. The first series was obtained using a 10 pA current limitation (series A1). The two next series were obtained without current limitation (A2 and A3 series), which means that the voltage ramp was applied until the maximum value whatever the current level. The A2 series was performed on the right part of A1 series area, and the A3 series was performed on the left part of A1 area.

In order to distinguish between the three series, the distances between the measurements points are different for each.

After applying the voltage ramps, the three series were scanned in intermittent-contact AFM with a specific intermittent-contact AFM tip. The result for the series A2 is shown in Figure 1. The surface, the volume, and the height of the hillocks formed on the surface were extracted from these topographic maps. The distribution of hillocks volumes of the series A1 alone and from the series A2 and A3 are presented in Figure 2. For series A1, when the electrical stress is limited, no surface deformation was observed in some cases. The average hillock's volume is  $3100 \text{ nm}^3$  while the larger volume is  $24400 \text{ nm}^3$ . The scattering of the volume value is important.

When the stress is not limited (series A2 and A3), hillocks are systematically observed, with an average volume

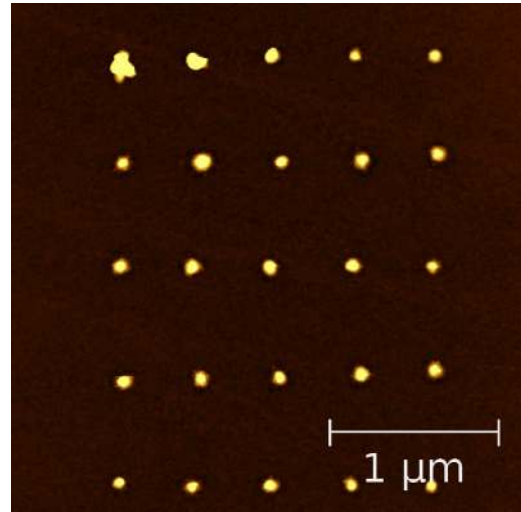
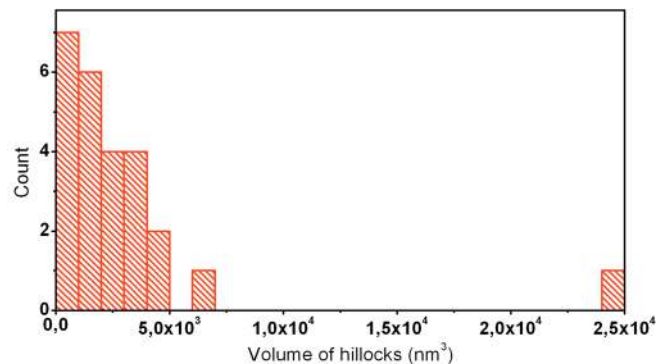


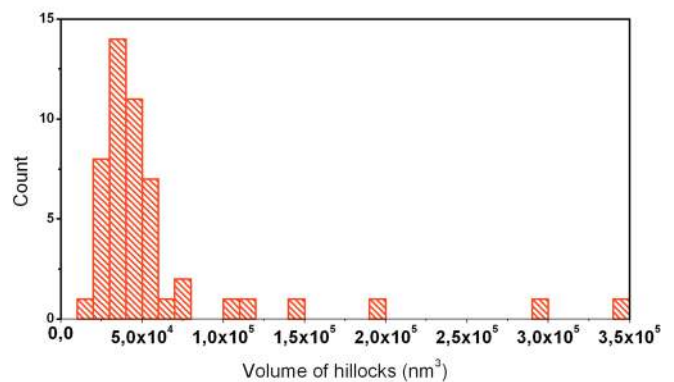
FIG. 1. Hillocks observed by AFM for the series A2.

of  $60000 \text{ nm}^3$ . The scattering is important too, the volumes range from  $22000 \text{ nm}^3$  to  $342000 \text{ nm}^3$ .

From these experiments, it can be pointed out that the volume of the hillock increases with the stress level (ramp parameters), but the scattering is large, so we suppose that the hillock formation is not only influenced by the applied voltage but also by other parameters.



a) Volumes of hillocks distribution for limited current serie (A1)



b) Volumes of hillocks distribution for non-limited current serie (A2, A3)

FIG. 2. Volumes of hillocks distribution for the series A1 (left) and A2 + A3 (right). The volumes are higher for the series without current limitation. In all cases, the scattering is important.

**IV. I-V CHARACTERISTICS**

For the series A1, A2, and A3, the current reaches 10 pA for  $-5.93$  V on average. For every curves, the voltage values are in the range  $-4.53$  V to  $-6.29$  V (an example is shown in Figure 3). Then the saturation is quickly reached. In some cases, the leakage current can be fitted with Fowler-Nordheim tunneling current model. In some cases, the current increase is steep, which is representative of dielectric breakdown. The measurements scattering can be explained by the intrinsic random nature of the dielectric breakdown.<sup>12</sup> Since the saturation is always reached, we cannot measure the electrical characteristic at high voltage bias and we cannot estimate the dissipated energy in the sample which may play an important role in thermal or electro-thermal phenomena.

In order to measure the current at high voltage (up to  $-10$  V), we have made the same experiment with the 10 nA range on the sample B. At first, two individual I-V curves (measurements labeled RVS1 and RVS2) have been performed on two fresh area of the sample. Then two series of 25 I-V measurements have been performed on two other fresh areas (measurement sets B1 and B2). Finally, two new individual I-V curves have been obtained (labeled RVS3 and RVS4). Only one tip has been used for all B series. The individual ramps help us to understand the scattering of the results and the interdependence of the measurements series as will be shown later. The first four I-V from B1 area is presented in Figure 4. It can be pointed out that the current reaches a maximum value before a stabilization or decreasing. The maximum value of current can reach 1 nA or higher before to decrease down to a value of  $\sim 100$  pA. The current peak happens not a long time after the current exceeds the noise level. The current arises from tunneling effect or from the breakdown of the oxide. In either case, the voltage is similar because the dielectric breakdown is largely due to hot carriers passing through the oxide layer.<sup>13</sup>

This shows that the hillocks' appearance leads to the decrease of the layer's conductivity. A possible sudden destruction of the AFM conductive tip cannot explain this observation because the phenomenon is reversible. The

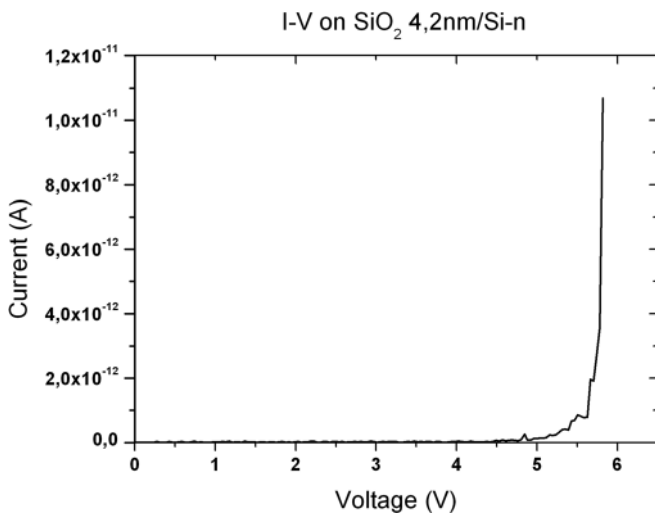


FIG. 3. I-V characteristics extracted from the series A1.

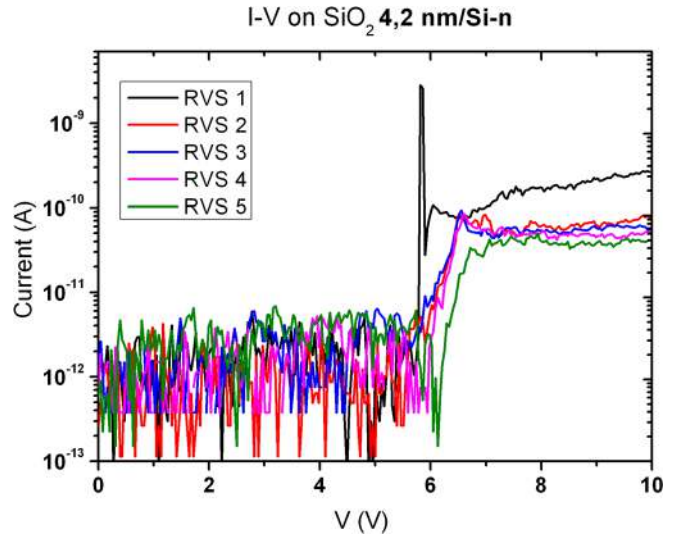


FIG. 4. I-V characteristics extracted from the series B1. The 4 opening curves are presented. The current increases suddenly and reaches a maximum. There is a current peak in the first curve.

decrease of the conductivity occurs quickly after the large increase of current, so we assume that the hillock formation is linked to this high value of the current.

**V. HILLOCK GROWTH**

A third group of experiments was performed (sample C) in order to get a more precise idea of the exact moment where the hillocks appear during the voltage sweep. These experiments were performed with the NTEGRA AFM from NT-NDT. The voltage sweep parameters are the same as previous experiments. The cantilever deflection signal was recorded in parallel with the current measurement. During the voltage sweep, the deflection feedback is turned off so that the deflection signal is linked to the tip displacement and thus surface motion. By doing so, we can track the hillock growth.

The measurements show that the current peak occurs at the same time as the beginning of the hillock growth (Figure 5). Force curves attest the relationship between the height of

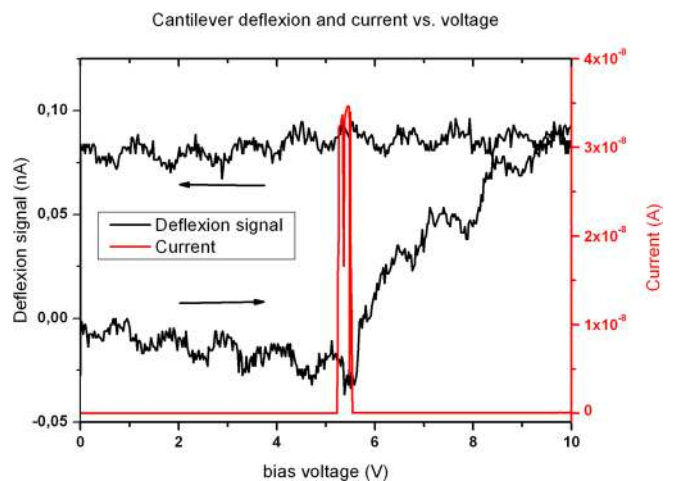


FIG. 5. Measurement of the cantilever deflection simultaneously to I-V acquisition. The hillock apparition is linked with the current peak.

the hillock and the measured deflection. The noise level on the deflection signal prevents from detecting precisely the beginning of the hillock growth in order to determine whether it precedes with the current peak. The hillock formation lasts a few seconds. Nonetheless, this experiment confirms the relationship between the high current level and the hillock formation.

## VI. IMPACT ON THE SUBSTRATE

In order to try and select the best explanation between the substrate oxidation theory and the electro-thermal theory, we focused on the degradation of the substrate after the formation of a hillock. If an oxidation of the substrate occurs, a cavity in the substrate should appear because of the consumption of the substrate during oxidation process. On the contrary, if it is a DBIE phenomenon, silicon atoms migrate with the electrons and an inflation of the substrate should appear.

To try and answer the question, the sample B has been treated with fluorhydric acid (HF) solution (concentration: 5% mass), during approximately 30 s in order to suppress the SiO<sub>2</sub> layer. Then, the sample has been rinsed with distilled water and dried.

After oxide suppression, the area has been scanned in intermittent-contact AFM mode. In these conditions, no electrostatic artifact may disturb the topography because there are no trapped charges. We did not observe any substrate deformation for the series A1 (I-V measurements limited current). However, most of the time, holes are observed in the substrate when the stress has not been limited (series A2 and A3). The result of series A2 is shown in Figure 6. The dimensions of these cavities are variable. The cavities' average volume is 17 200 nm<sup>3</sup>. The minimum value is 3400 nm<sup>3</sup> (trace) and the maximum is 73 000 nm<sup>3</sup>. The hillocks' average volume/hole ratio is 3.5 and the ratio (*r*) average is 4. *r* ranges between 0.76 and 10.15. 74% of the values of *r* are between 2 and 4, 14% is lower than 2, and 12% higher than 4 (Figure 7). The extreme values are probably due to measurement incertitude.

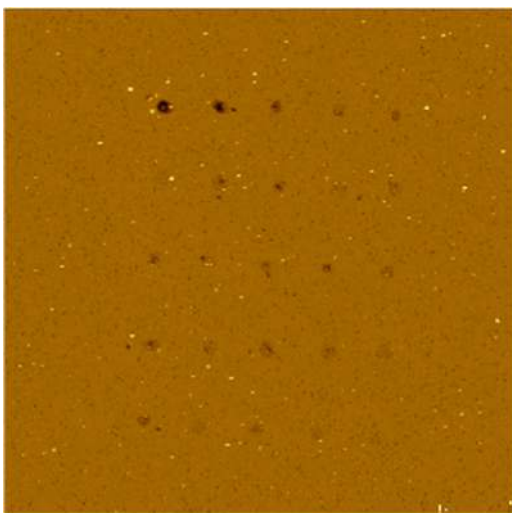


FIG. 6. Substrate topography of the series A2. Holes are observed when the electric stress is maximum.

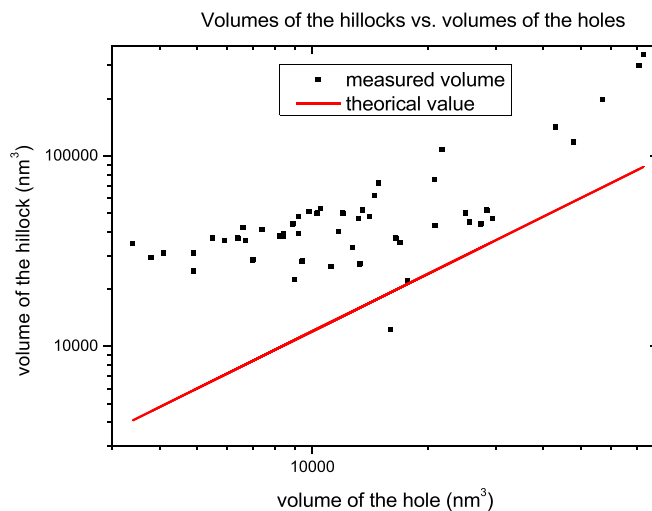


FIG. 7. Comparison of the hillocks volumes and the corresponding holes volumes (sample B). The hillocks volumes are four times higher than the holes volumes in average with large scattering.

If a compact and stoichiometric oxide is formed, the hillock/cavities volume ratio must be 1.2. In our experiments, the oxide formed during the hillock's growth should be extremely non compact and non stoichiometric to explain the ratio between the volume of the cavity and the volume of the hillock.

It has to be pointed out that the cavities volumes may be under-evaluated owing to their very small dimensions (a few tens of nanometers large and a few nanometers deep) compared to the tip dimensions. Nonetheless, the hillocks volume seems to be under-evaluated too because electric charges are injected in the layer during the electrical stress. So, during scanning, an image charge appears in the AFM conductive tip. Therefore, an attractive electrostatic force reduces the visible volume.<sup>14</sup> Independently of the role of the injected charges on the mechanisms which lead to the formation of the hillocks, the observation of the hillocks is not solely due to the electrostatic interaction arising from the presence of trapped charges in the volume of the oxide, although they may play a role on the apparent volume of the protuberances because injected charges may reduce the observed deformation.

The cavities in the silicon substrate could be explained by an oxidation mechanism but their volume is indeed small. Furthermore, there are no cavities when the stress is limited even though hillocks appear. We can conclude that a phenomenon different from oxidation cause the observed hillock's growth. This phenomenon and oxidation can coexist as it has been already proposed.<sup>14</sup>

## VII. DISSIPATED ENERGY

The energy dissipated in the oxide layer has been extracted from experiments obtained with sample B. The 10 nA range was used here. We assume that all the energy is dissipated in the dielectric layer. The energy is calculated by time integration of the product of the current and the voltage.

The values of dissipated energies are very scattered: from  $1.1 \times 10^{-9}$  to  $1.9 \times 10^{-7}$  J with an average value at

$1.1 \times 10^{-8}$  J. The weak relationship between the hillocks volumes and the dissipated energies is shown in Figure 8. The hillock's volume seems to show a logarithmic increase with dissipated energy. It seems that the hillock growth saturates.

Silicon and SiO<sub>2</sub> specific heat capacities are almost identical  $711 \text{ J kg}^{-1} \text{ K}^{-1}$  and  $712 \text{ J kg}^{-1} \text{ K}^{-1}$ , respectively. Their densities are close too with  $2.33 \text{ g cm}^3$  and  $2.27 \text{ g cm}^3$ , respectively. The silicon melting point is 1414 K and the SiO<sub>2</sub> melting point is near 1650 K. The thermal conductivity of silicon ( $140 \text{ W m}^{-1} \text{ K}^{-1}$ ) is higher than the SiO<sub>2</sub> thermal conductivity ( $1.4 \text{ W m}^{-1} \text{ K}^{-1}$ ). If we take into account a  $20\,000 \text{ nm}^2$  surface, which corresponds to the average surface of the hillocks, and a  $4.2 \text{ nm}$  layer thickness, the considered volume of the oxide is equal to  $840\,000 \text{ nm}^3$ . The energy required to reach the melting point from 300 K is  $1.8 \times 10^{-13} \text{ J}$ . So, the dissipated energy is much larger than the required energy to reach the melting point. This energy is dissipated in the dielectric layer and the SiO<sub>2</sub> has a low thermal conductivity. The silicon melting point is lower than the SiO<sub>2</sub> melting point but evacuates the heat more efficiently than the oxide. That is why we assume that during the passage of an important current in such a little surface significant increase of temperature should happen and the temperature may be higher in the oxide than in the substrate. At first, the oxide atoms under the AFM tip become more mobile. The material is reorganized (like a phase transition) and the compactness decreases. It is possible that the temperature passes the melting point as it has already been proposed.<sup>15</sup> If the dissipated energy is important enough, the substrate may be affected too. The silicon is locally weakened and a matter exchange occurs with the oxide layer. When the bias is removed, oxygen atoms may be able to penetrate the damaged volume. The potential barrier is more important because the layer thickness is larger. We assume that the material created after this process is a non-stoichiometric and non-compact oxide.

If the current level is limited, the substrate is never damaged and a large energetic gap between both scenarios exists.

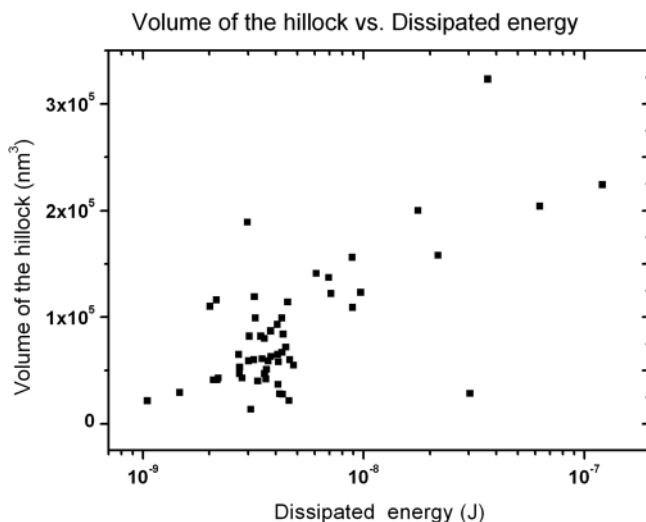


FIG. 8. Comparison of the hillocks volumes and the corresponding dissipated energies. There is a low relationship between the both parameters.

The required energy for substrate damaging is far higher than the required energy for dielectric layer damaging.

In a first phase, the passage of the charge carriers through the dielectric causes the apparition of oxide defects which favors the conduction. This is the classical degradation mechanism. In our case, as soon as the current is sufficiently large, a hillock grows and the conduction decreases. We can note that if the material melting point is reached, the AFM tip coating must melt too. An important damage to the AFM tip is shown in Figure 9.

### VIII. INTERDEPENDENCE OF THE MEASUREMENTS

A large scattering of electrical results, hillocks dimensions, and dissipated energy have been mentioned in this paper. The first explanation is statistical: the scattering is due to the sample inhomogeneity and the dielectric breakdown is a random phenomenon.

We can also note the large degradation of the AFM tip during voltage sweep. That is an important problem for the reproducibility.<sup>15</sup> The tip heating is a possible explanation: after the first ramp, the tip is hot, and the collection of the current may be influenced. Considering the situation, one important problem may arise from the short delay between two individual measurements.

During our experiments, we have pointed out that the acquisition of series of measurements (instead of individual I-V curves) affects the results. Indeed, the ramp voltage sweeps are applied in a row on different points located in a few micrometers wide area. In order to verify the influence of this experimental protocol, two individual measurements have been operated on sample B before and after two series of 25 measurements.

Figure 10(a) illustrates the impact of serial acquisitions. Generally, during serial acquisition, the very first ramps produce bigger hillocks compared to the following. Besides, the individual ramps produce big hillocks just like the very first ramps of the series. The same tendency is observed for energy dissipation which is higher for the first ramps and the individual ramps (Figure 10(b)) compared to the others. Also, the current increases quickly at lower voltage for these

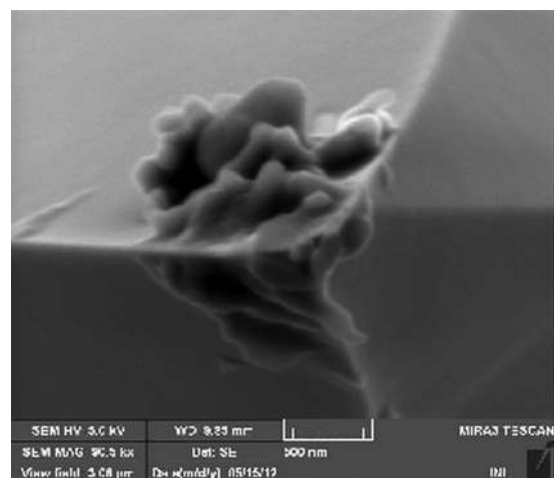


FIG. 9. SEM image of an AFM conductive tip after use. The PtIr coating is strongly damaged.

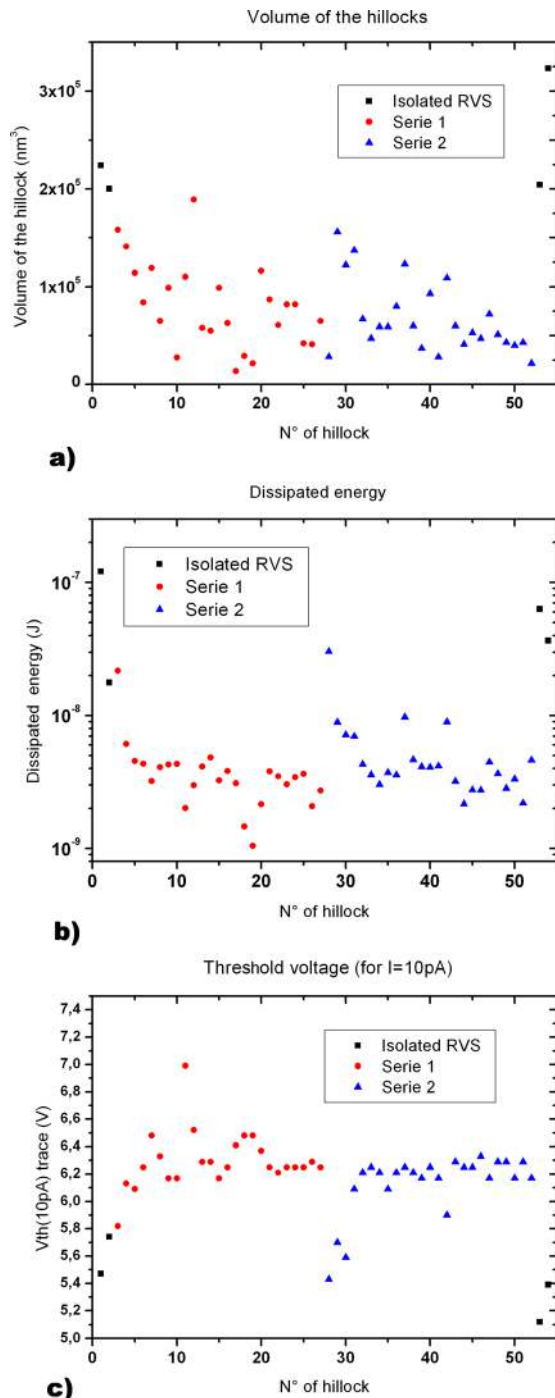


FIG. 10. (a) Volumes of the hillocks for sample B. (b) Dissipated energies. (c) Voltage values for 10 pA. The opening ramps and the individual ramps give different results as the next ramps.

ramps as it shown in Figure 10(c). This result is not due to the tip coating degradation because the same result is reproduced with the same tip at different moments.

It has been proved that the water layer on the sample facilitates the hillocks growth.<sup>15</sup> Moreover, the hillocks obtained in vacuum are smaller and rare but they still exist. The water layer and meniscus are not directly responsible for the hillocks apparition but facilitate the dielectric layer degradation and the onset of higher leakage current. It was proposed that the  $H^+$  ions arising from water dissociation are

injected in the oxide layer and create traps for charges carriers,<sup>16–18</sup> which facilitate the injection of current.

We propose that during the experiments operated in series, the first voltage ramp is responsible for the increase of the temperature at the micrometer scale on the surface under investigation. As a consequence, the water layer is partially desorbed. During the following measurements, the damaging of the oxide is reduced due to the reduced amount of water (onset of high current at higher voltage). Consequently, the leakage current is lower as well as the dissipated energy, leading to a smaller hillock.

Furthermore, as the AFM tip is hot, the water meniscus is also reduced. The dielectric breakdown is less affected by the presence of water. In other words, a progressive current increase generates a moderate hillock growth.

As a conclusion, the hillock formation is largely linked to the breakdown dynamics which is itself linked to the presence of water.

## IX. CONCLUSION

In this paper, we have considered the formation of abnormal hillocks on the surface of ultra-thin dielectric layer during C-AFM measurements at positive tip bias (or negative sample bias).  $SiO_2$  samples have been studied in order to work with a perfect, well defined dielectric layer. By means of deflection measurements, we have shown that the hillock growth occurs when the current becomes large. This hillock is highly resistive and impinges the injection of current. If the electric stress is moderate, only the oxide is damaged but if the electric stress is higher (voltage ramp fully applied), cavities appear on the substrate. The cavity is smaller than the corresponding hillock, which does not seem to correspond to an oxidation phenomenon. The dissipated energy is important so we may suppose an important increase of temperature. The hillock may be linked to the thermal expansion of the oxide layer and a great increase of the temperature of the layer and the substrate.

Finally, we have demonstrated a interdependence between results during serial measurements. For the very first voltage ramps, the hillocks are bigger as well as the dissipated energy, and the breakdown voltages are lower. It may be explained by the heating of the surface under investigation which reduces the amount of water on the surface. Water enhances the damaging process of the layer and accelerates the breakdown which leads to higher leakage currents and bigger hillocks. To conclude, we can infer that, electric measurements on thin dielectric layers with C-AFM are largely affected by the ambient atmosphere because of the humidity.

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