A 40-nm CMOS, 1.1-V, 101-dB Dynamic-Range, 1.7-mW Continuous-Time Sigma Delta ADC for a Digital Closed-Loop Class-D Amplifier

A. Donida, Rémy Cellier, A. Nagari, P. Malcovati, A. Baschirotto

A 40-nm CMOS, 1.1-V, 101-dB Dynamic-Range, 1.7-mW Continuous-Time ΣΔ ADC for a Digital Closed-Loop Class-D Amplifier

Achille Donida, Rémy Cellier, Angelo Nagari, Piero Malcovati, Andrea Baschirotto

***Abstract*—This paper presents a continuous-time third-order ΣΔ modulator designed for closing the feedback loop of a digital class-D audio amplifier. The closed-loop digital class-D amplifier fully exploits the potential of the used 40-nm CMOS technology to achieve at the same time the flexibility of digital implementations and the performance of analog solutions. The proposed ΣΔ modulator consumes 1.7 mW from a 1.1-V power supply, achieving 101-dB dynamic-range (*DR*) and 72-dB peak signal-to-noise and distortion ratio (*SNDR*). The active-RC implementation allows the 1.1-V ΣΔ modulator inputs to be directly connected to the 5-V class-D amplifier power stage outputs and inherently guarantees third-order anti-aliasing filtering.**

***Index Terms*—Sigma-delta modulation, Audio systems, Amplifiers, Analog-digital integrated circuits.**

I. Introduction

Mixed-signal systems-on-chip (SoC) for digital-input audio signal processing have to face challenging constraints for integration in deep sub-micron technologies (down to 40 nm and beyond). In such nodes low-noise and low-voltage blocks can be addressed, while medium power circuits such as hand-free amplifiers encounter severe problems to deliver the required acoustic output power. Typical specifications of 1 W over 8-Ω speaker can be achieved with a closed-loop switching class-D amplifier only using a high-voltage (HV) power stage supply of about 5 V [1]–[3].

A solution for handling HV signals in submicron technologies could be to move the class-D amplifier loop-filter into the digital domain [4], [5]. This optimizes the interfacing with the digital signal source with respect to analog solutions, that would require a challenging input D/A converter (DAC) and an analog loop filter [6]. On the other hand, the high-density and high-speed logic available in scaled technologies enables mixed-signal (mainly digital) architectures with smaller area and power consumption [7].

Achille Donida was with Department of Electrical, Computer, and Biomedical Engineering, University of Pavia, Pavia, Italy, now he is with SUPSI, Lugano, Switzerland, E-Mail: achille.donida@supsi.ch.

Rémy Cellier is with CPE-INL, CNRS UMR 5270, University of Lyon, Lyon, France, E-Mail: remy.cellier@cpe.fr.

Angelo Nagari is with STMicroelectronics, Grenoble, France, E-Mail: angelo.nagari@st.com.

Piero Malcovati is with Department of Electrical, Computer, and Biomedical Engineering, University of Pavia, Pavia, Italy, E-Mail: piero.malcovati@unipv.it.

Andrea Baschirotto is with Department of Physics "G. Occhialini", University of Milano-Bicocca, Milano, Italy, E-Mail: andrea.baschirotto@unimib.it.

Digital class-D amplifiers can be easily implemented with an open-loop architecture [1], [8], by implementing the pulse-width modulation (PWM) in the digital domain and diving directly the power stage with the obtained PWM signal. Open-loop class-D amplifiers, however, have some practical drawbacks, which prevent their use in high-performance audio systems. First of all, the overall gain of the amplifier depends on the supply voltage of the power stage, which has to be clean and accurate, since any noise or disturbance on the power rails is transferred directly to the load, leading to a degradation of the signal-to-noise ratio (*SNR*) [9]. Moreover, all the power stage non-idealities, such as delay mismatch, dead time, and rise/fall time mismatch, affect the output signal quality, degrading the total harmonic distortion (*THD*) [10], [11]. To overcome these limitations, most class-D amplifiers are used in a closed-loop configuration, so that the overall amplifier gain is only determined by the feedback factor and, therefore, it is constant and well defined, independently of the power stage supply voltage. Moreover, all the non-idealities of the power stage are strongly attenuated by the loop gain [12]. In order to close feedback loop in a digital class-D amplifier, the analog output signal has to be fed back in the digital domain, thus requiring an A/D converter (ADC) with challenging specifications [13].

The paper is organized as follows: Section II describes the overall architecture of the proposed class-D amplifier, as well as the most important building blocks implemented in the digital domain. The architecture and the detailed implementation of the ADC used to close the feedback loop of the class-D amplifier are then illustrated in Section III and Section IV, respectively. Finally, Section V reports the achieved experimental results.

II. Digital Class-D Amplifier Architecture

Fig. 1 illustrates the complete block diagram of the proposed digital closed-loop class-D amplifier. The forward path, implemented in the digital domain, fully exploits the potential of the 40-nm CMOS node, operating with a 38.4-MHz master clock frequency (f_{MCLK}), in order to produce an accurate digital PWM signal. The digital circuit consists of four main blocks: an interpolation block with an oversampling ratio (*OSR*) equal to 8, which is necessary for the following ΣΔ modulator (ΣΔM) and to improve the linearity of the PWM [6], a digital loop filter (corrector), a discrete-time digital ΣΔM, which reduces the signal word-length for the following digital PWM

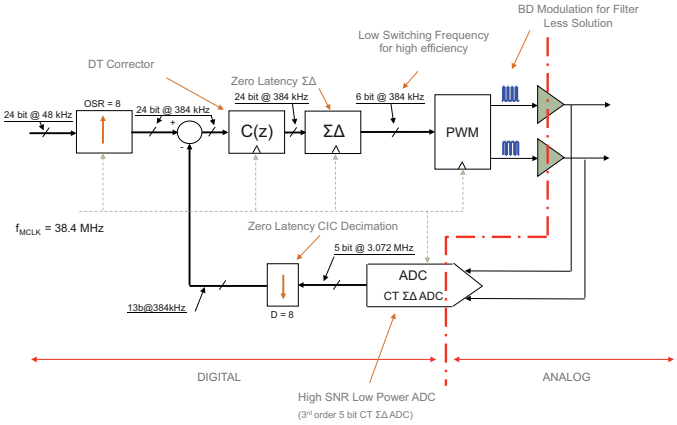

Fig. 1. Block diagram of the digital class-D amplifier

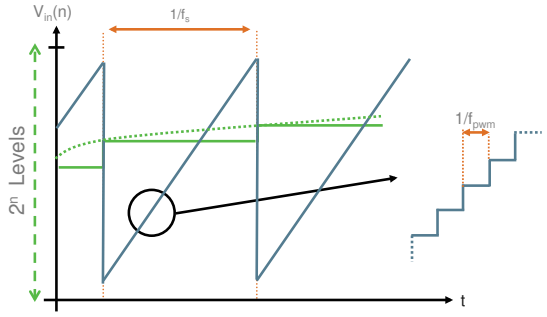

Fig. 2. UPWM frequency limitation

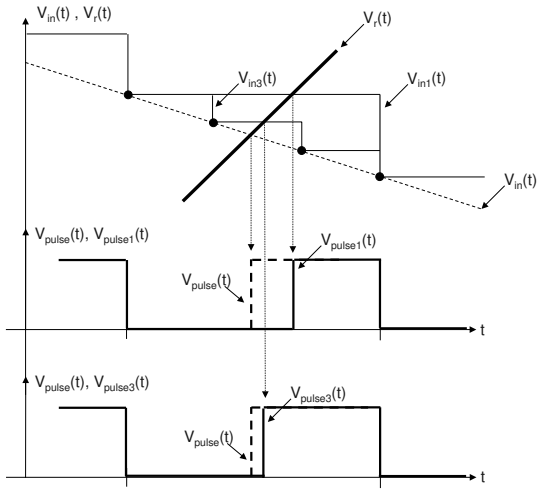

Fig. 3. Timing error in digital UPWM due to the sampled input signal

generator, a counter-based differential digital PWM generator.

The feedback loop is closed by feeding the digital corrector $C(z)$ with an accurate representation of the output signal, through an ADC. This ADC has challenging performance requirements. Indeed, the ADC input signal is coming directly from the output power stage of the class-D amplifier and, therefore, it is a large swing (5-V) square wave signal. whereas the ADC voltage supply is 1.1 V. In addition, the ADC must provide efficient anti-aliasing filtering (AAF) in order to prevent the PWM spur components from folding back into audio band. Finally, the ADC delay must be minimum to relax the loop stability requirements and hence allow the loop to have a more aggressive transfer function.

Since the ADC is the most important contributor to audio performance limitations (any error introduced by an element in the feedback path cannot be corrected), ADC linearity and noise must fit the overall audio performance, which are 100 dB_A of *SNR* and less than 0.1% of *THD*.

The class-D amplifier PWM frequency is fixed to 384 kHz, as a trade-off between power stage efficiency and loop linearity.

A. PWM Generator

In embedded applications, the audio input signal comes from a digital baseband processor or a digital CODEC (e. g. a voice processor or an MP3 decoder) and its resolution n ranges usually from 16 to 24 bits (PCM, I^2S format). A straightforward solution for implementing a digitally-controlled class-D amplifier is to modulate this signal directly in a PWM bitstream V_{pulse} to drive the power stage of the amplifier. This solution, called direct uniform PWM (UPWM), is actually unpractical, because of frequency limitations for the UPWM carrier and linearity errors.

As shown in Fig. 2, direct UPWM involves the use of a digital saw-tooth signal, generated by an n-bit counter, as carrier, in order to create a PWM bitstream from the n-bit digital input signal sampled at frequency f_s. The clock frequency f_{pwm} required to generate the carrier signal is, therefore, given by

$$f_{pwm} = 2^n f_s. \quad (1)$$

Considering n equal to 24 bits and f_s at least equal to 48 kHz, f_{pwm} turns out to be as large as 805 GHz. Obviously, such a value of frequency is unreachable in standard CMOS technologies. In addition, due to the sampled nature of the input audio signal, the UPWM process introduces an error when compared to the ideal analog natural PWM (NPWM). In Fig. 3, the error due to the sampled input signal is illustrated in three cases: with a continuous-time (analog) input signal $V_{in}(t)$ and with two sampled versions of $V_{in}(t)$, namely $V_{in1}(t) = V_{in}(iT_s)$ and $V_{in3}(t) = V_{in}(iT_s/3)$, $T_s = 1/f_s$ being the sampling period. Each of these signals is compared with a carrier $V_r(t)$, in order to generate the modulated output signal $V_{pulse}(t)$, $V_{pulse1}(t)$, and $V_{pulse3}(t)$, respectively. In this example, the carrier signal is assumed continuous-time, but in reality it is also a sampled signal and, therefore, the resulting error is actually worse. As NPWM is a linear process, the timing error due to sampling makes the UPWM process inherently non-linear. The higher is the sampling frequency of the audio signal, the less important is the error. In other words, NPWM is equivalent to UPWM with infinite sampling frequency. Therefore, to improve the linearity of the UPWM, the digital audio signal V_{in} can be oversampled by a defined *OSR*. However, according to (1), this further increases the clock frequency requirement for carrier generation, unless at the same time a significant reduction of n is implemented.

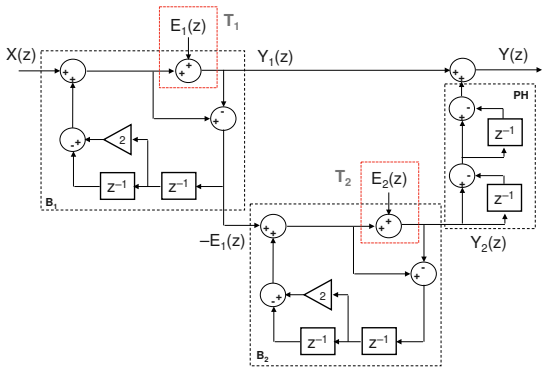

Fig. 4. Architecture of the fourth-order MASH 2-2 digital ΣΔM

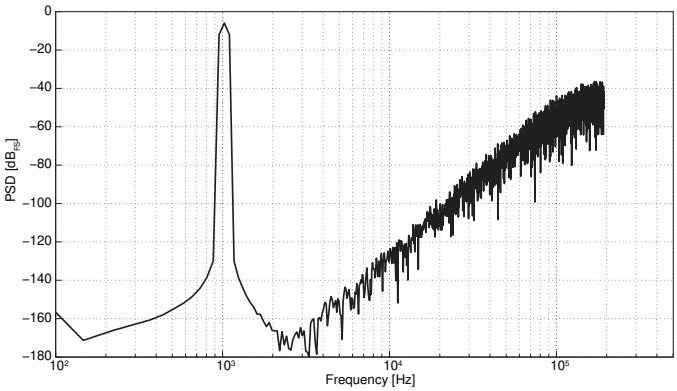

Fig. 5. Output spectrum of the fourth-order MASH 2-2 digital ΣΔM

These drawbacks of direct UPWM can be overcome by using ΣΔ modulation before the UPWM. Indeed, ΣΔ modulation provides oversampling of the digital signal, thus increasing the UPWM linearity, as well as a reduction of the signal resolution from 24 bits to m bits (generally m is chosen between 4 and 8), thus leading to acceptable values of f_{pwm}. Obviously, a suitable ΣΔM architecture has to be chosen in order to guarantee that, with the target values of OSR and m, the signal-to-noise ratio (SNR) of the original audio input signal is maintained by shaping the quantization error with a noise transfer function (NTF) which sufficiently attenuates the in-band components. Indeed, the choice of OSR, output resolution m, order k and structure (e. g. CIFF, CIFB, MASH) of the ΣΔM depends on the required NTF. Trade-offs between performance and complexity, considering stability issues and global power consumption, have to be found.

B. Digital ΣΔ Modulator

The ΣΔM used in front of the UPWM in the proposed class-D amplifier is based on a digital fourth-order MASH 2-2 architecture, with $OSR = 8$ and $m = 6$, as shown in Fig. 4. The MASH 2-2 structure features only second order loops, thus relaxing the stability issues inherent in a single-loop fourth-order ΣΔM. Moreover, the implemented solution uses only power of two multiplications and pure delays, which make the hardware implementation easier. The value of OSR is limited to have a moderate switching frequency (384 kHz), thus maintaining high power efficiency in the power stage [14].

The output signal $Y(z)$ of this zero latency ΣΔM is given by

$$Y(z) = X(z) + E_2(z)\left(1 - z^{-1}\right)^4, \tag{2}$$

where $X(z)$ and $E_2(z)$ are z-domain representations of the input signal and of the second-stage truncation error, respectively. The quantization noise E_2 is shaped by a fourth-order high pass filter, whereas the quantization noise E_1 (i. e. the truncation error of the first stage of the MASH structure) is removed. The simulated spectrum of $Y(z)$ is shown in Fig. 5. With theses parameters, the required frequency value of f_{pwm} for the UPWM is then reduced to

$$f_{pwm} = 2^m f_s OSR = 24.576 \text{ MHz}. \tag{3}$$

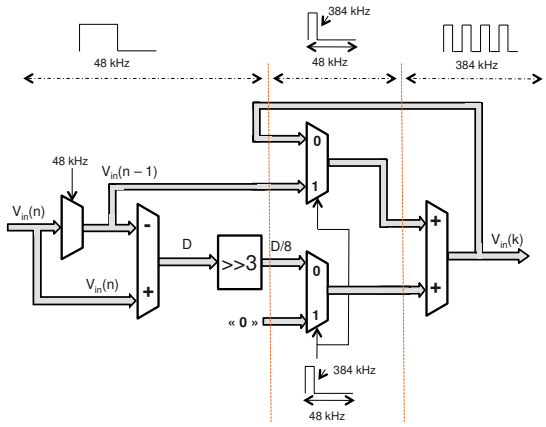

Fig. 6. Block diagram of the interpolator

C. Interpolator

The interpolator, required at the input of the forward path of the digital class-D amplifier to increase the sampling frequency from $f_s = 48$ kHz to $f_s OSR = 384$ kHz, is a two-stage structure based on a piece-wise linear function, as shown in Fig. 6. The frequency response of this structure features a sinc^2 shape with an in-band ripple too large to meet audio specification (±0.1 dB). To fix this issue, a pre-filter is added before the interpolator to compensate for the ripple. The pre-filter is a simple biquadratic FIR digital filter with 9 coefficients, as shown in Fig. 7.

Fig. 8 shows the simulated and measured interpolator frequency responses with the in-band ripple correction.

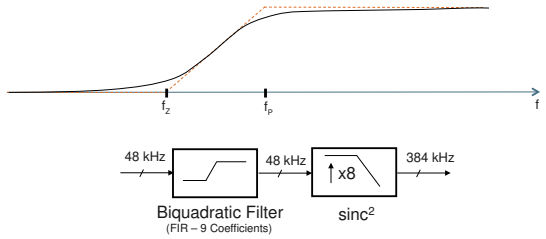

Fig. 7. Block diagram and frequency response of the FIR digital pre-filter

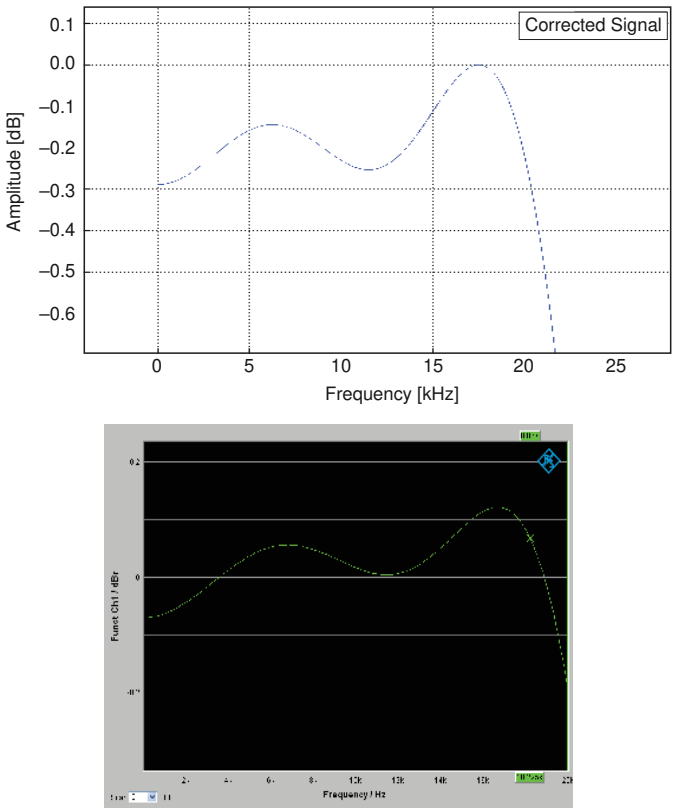

Fig. 8. Simulated and measured frequency response of the interpolator with the in-band ripple correction

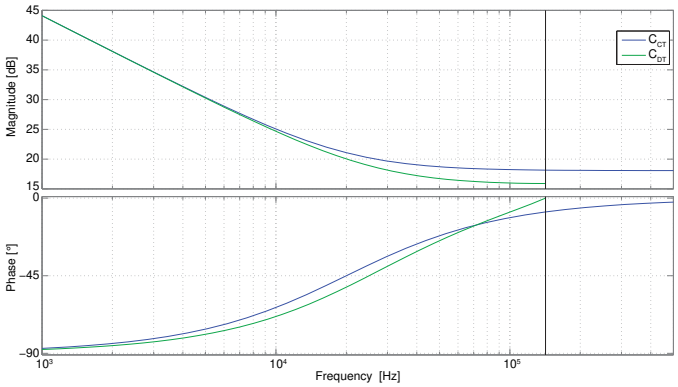

Fig. 9. Bode diagrams of the continuous-time C_{CT} and discrete-time C_{DT} correctors

TABLE I
ADC SPECIFICATIONS

Parameter	Value
SNR	> 100 dB
THD	< 0.1%
Output word-length	5 bits
Sampling frequency (f_{ADC})	3.072 MHz
OSR	64
Signal bandwidth (f_b)	24 kHz
AAF	Third-order, low-pass
Delay (latency)	< 1 µs
Input voltage range	5 V
Power supply voltage	1.1 V
Power consumption	< 2 mW
Technology	40-nm CMOS

D. Digital Corrector

The loop filter characteristics are derived from Bode plot analysis of the control-loop transfer function and depend on where the feedback is tapped. As shown in Fig. 1, in the proposed digital class-D amplifier, the feedback is taken at the output of the power stage, thus removing the cost of an extra pin. If the feedback is taken after the output low-pass filter, extra phase shift has to be taken in account in the stability analysis of the whole loop.

For this particular application, a lag compensator [15] of the form,

$$C_{CT}(s) = K_0\left(1 + \frac{2\pi f_I}{s}\right), \tag{4}$$

is sufficient to verify system performance. This kind of compensator is used to increase the loop gain such that the output is better regulated at low frequency (i. e. below f_I). It is often called proportional-integral (PI) corrector. For frequencies below f_I, $C(s)$ act as a pure integrator.

Increasing the low-frequency loop gain leads to better immunity to the disturbances on the power-bridge supply voltage in the audio band, but at the expense of worse loop stability. The optimal values of K_0 and f_I are, therefore, the result of a trade-off between performance and stability. For the proposed class-D amplifier, we chose $K_0 = 8$ and $f_I = 20$ kHz.

Pole zero matching [16] transform $C(s)$ into $C(z)$ for digital implementation. The resulting digital coefficients values obviously depend on the sampling rate (f_c). Applying pole-zero matching to $C(s)$ with $f_c = 384$ kHz leads to

$$C_{DT}(z) = \frac{8 - 4.46z^{-1}}{1 - z^{-1}}. \tag{5}$$

Fig. **??** shows the Bode diagrams of the continuous-time C_{CT} and discrete-time C_{DT} correctors. In the audio band, both behave as pure integrators. With this corrector, the theoretical *PSRR* is around −25 dB at 20 kHz and −65 dB at 217 Hz, which match standard *PSRR* requirements.

III. A/D Converter Architecture

The most important specifications of the ADC required to close the feedback loop of the proposed digital class-D amplifier are summarized in Tab. I. In view of these specifications, the best candidate for implementing the SDC is a continuous-time (CT) ΣΔM. Indeed, CT ΣΔMs allow large *SNR* to be achieved with lower power consumption and lower latency than any other ADC topology, while providing inherent AAF.

A k^{th}-order CT ΣΔM with m-bit quantizer theoretically achieves a *SNR* given by

$$SNR = \frac{2^{2m}3\,(2k+1)\,OSR^{2k+1}}{2\pi^{2k}}. \tag{6}$$

With $OSR = 64$ and $m = 5$, in order to achieve the required $SNR > 100$ dB, the order k of the ΣΔM has to be at least 3.

A third-order CT ΣΔM can be implemented using different architectures. All of them are derived from two basic

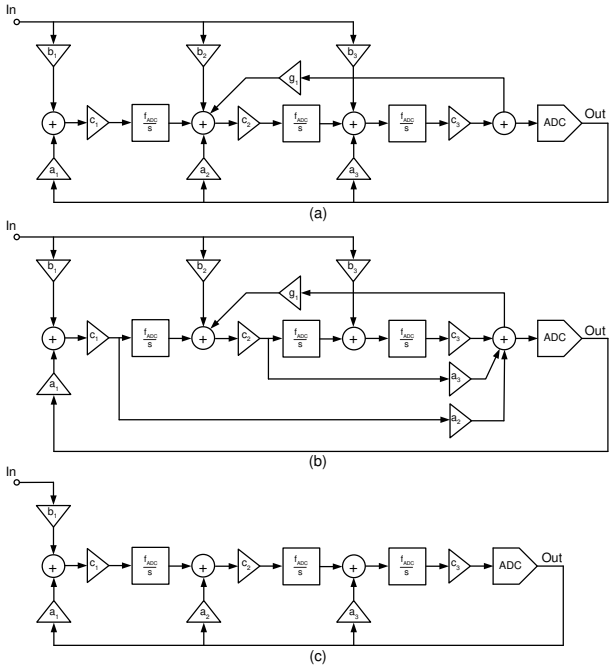

Fig. 10. Third-order CT ΣΔM implemented with the CIFB architecture (a), with the CIFF architecture (b), and with the adopted architecture (c)

structures: the cascade of integrator with feedback (CIFB) structure, shown in Fig. 10a, and the cascade of integrators with feedforward (CIFF) structure, shown in Fig. 10b. With the CIFB approach, stability is guaranteed by feedback paths from the modulator output to the input of each integrator (coefficients a_i in Fig. 10a), whereas with the CIFF approach stability is obtained by means of feedforward paths from the output of each integrator to the input of the quantizer (coefficients a_i in Fig. 10b). While from the *NTF* point of view CIFB and CIFF architectures are totally equivalent, they are different in the implementation. Indeed, CIFB structures require two additional DACs to implement the feedback paths, while CIFF structures require an additional adder at the input of the quantizer to combine the different feedforward paths. In both approaches, additional feedforward paths from the modulator input to the input of each integrator (coefficients b_2 and b_3) can be introduced to optimize the output voltage swing of the integrator output signals, at the expense of the filtering action of the signal transfer function (*STF*). Indeed, with $b_2 \neq 0$ and $b_3 \neq 0$, and in general in the presence of feedforward paths (e. g. in CIFF structures), the *STF* tends to be unitary, actually canceling the inherent AAF feature of CT ΣΔMs. Therefore, as a trade-off between AAF action and ΣΔM latency, we adopted a CIFB architecture without feedforward paths ($b_2 = b_3 = 0$), featuring all the *NTF* zeros in the origin ($g_1 = 0$), as shown in Fig. 10c.

The ΣΔM coefficients, determined using the *DelSig* toolbox [17] and the Euler transformation

$$\frac{1}{z-1} \rightarrow \frac{f_{ADC}}{s}, \tag{7}$$

are summarized in Tab. II. The input and output spectra of the ΣΔM achieved in simulation with a PWM output signal, as

TABLE II
COEFFICIENTS OF THE CT ΣΔM

Coefficient	Value
a_1	0.044
a_2	0.287
a_3	0.8
b_1	0.044
c_1	1
c_2	1
c_3	1

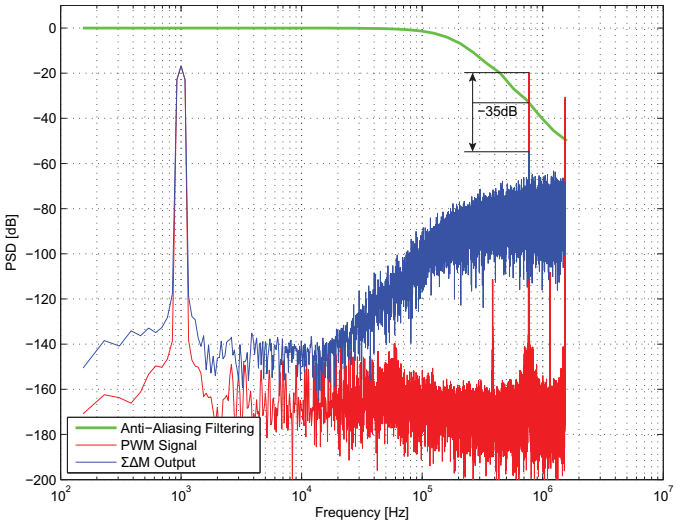

Fig. 11. Simulated input and output spectra of the CT ΣΔM with a PWM output signal and obtained *STF*

well as the obtained *STF*, are illustrated in Fig. 11. The ΣΔM achieves third-order noise shaping, as expected, and, thanks to the low-pass behavior of the *STF* (cut-off frequency around 150 kHz), attenuates the PWM spur components present in the input signal by more than 35 dB.

IV. A/D CONVERTER IMPLEMENTATION

The schematic of the proposed CT ΣΔM is shown in Fig. 12. Active-RC implementation is used for performance robustness and to allow direct connection of the ΣΔM input to the

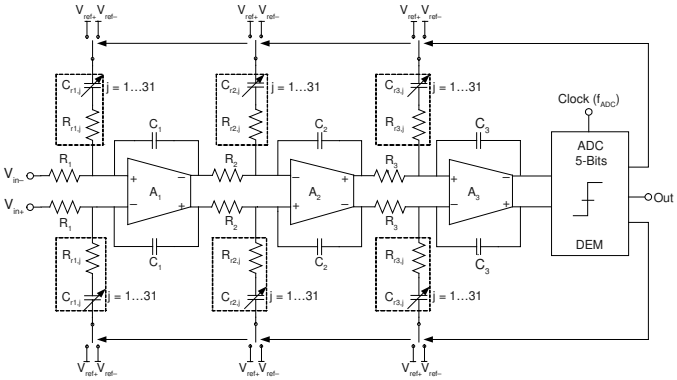

Fig. 12. Schematic of the CT ΣΔM

HV power bridge output. Indeed, since with the active-RC topology the ΣΔM input signals (V_{in+}, V_{in-}) are only connected to resistors (R_1), which can withstand voltages larger than the power supply, they can be directly tied to the 5-V power bridge outputs, without requiring any additional circuit, even if the ΣΔM is realized with 1.1-V devices.

The first integrator resistors and capacitors have been sized to satisfy the thermal noise requirements, taking into account the signal attenuation by a factor of 12 required to accommodate the 5-V power bridge output swing within the 400-mV ΣΔM input range. In particular, the first stage has been sized with R_1 = 163 kΩ and C_1 = 81 pF. The resistors and capacitors of the second and third integrators have been scaled to optimize area, power consumption, and output swing: R_2 = 160 kΩ, C_2 = 13 pF, R_3 = 25 kΩ, and C_3 = 6.5 pF.

A. D/A Converters

The first integrator feedback DAC is the most critical block in a CT ΣΔM, since its linearity affects the linearity of the entire circuit and any noise components injected by the DAC cannot be distinguished from the input signal, thus degrading the *SNR*. Moreover, a typical problem in CT ΣΔMs is the jitter sensitivity. Indeed, generally, the feedback DAC pulses remain constant over the whole clock period, and, therefore, their integral varies linearly with the integration time, which is modulated by the clock jitter. This leads to an error which affects both the *SNR* and the *THD*. The effect of the clock jitter strongly depends on the DAC implementation, thus requiring a careful choice of the best topology to use.

The current steering DAC, is most common solution adopted in CT ΣΔMs. In this circuit, a set of current mirrors are connected to the switches controlled by the quantizer output, thus adding or subtracting a given amount of current from the integrator summing node [18]. This solution is quite simple, since it does not require any reference voltage, but it is very sensitive to clock jitter. This problem can be partially alleviated using the return-to-zero (RZ) code (i. e. the current goes back to zero at the end of each sampling period), which makes the error due to clock jitter at least independent of the input signal. However the major drawback of this solution is the switch charge injection which depends on the size of the switches and leads in any case to distortion. Another solution to implement the DAC is to use resistive feedback branches [19]. This solution is expensive in terms of power consumption, since the resistors should have small size to reduce the thermal noise ($4kTR$) and the parasitic capacitance, which causes excess delay in the feedback loop.

Considering the drawbacks of current steering and resistive DACs, the solution adopted in the proposed CT ΣΔM is the switched-capacitor-resistive (SCR) topology, shown in Fig. 12 and, in more detail, in Fig. 13 [20]. The circuit operates with two non-overlapping clock phases (ϕ_1 and ϕ_2). During each clock cycle, capacitors $C_{ri,j}$ ($i = 1 \cdots 3$, $j = 1 \cdots 31$) store a precise amount of charge ($Q = C_{ri,j}V$, V being equal to $V_{ref+} - V_{CM}$ or $V_{ref-} - V_{CM}$, depending on the value of bit B_j). The capacitors are then discharged into the integrator summing node through a resistor $R_{ri,j}$ ($i = 1 \cdots 3$, $j = 1 \cdots 31$),

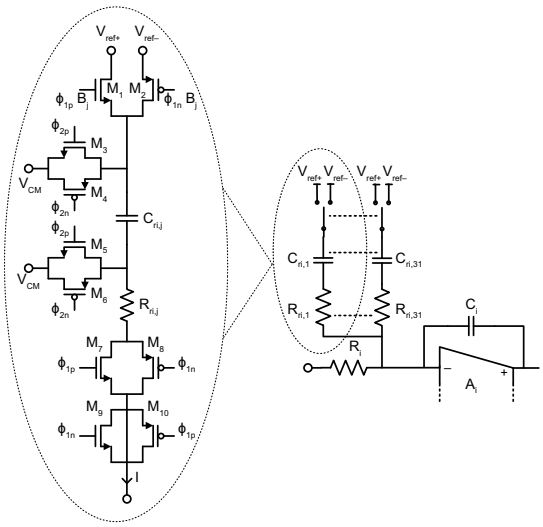

Fig. 13. Schematic of a single cell of the SCR DAC

which defines an exponentially decaying current pulse, with time constant $\tau_i = R_{ri,j}C_{ri,j}$, according to

$$I = \frac{V}{R_{ri,j}} \mathrm{e}^{-t/\tau_i}. \tag{8}$$

The main advantage of this structure is the insensitivity to clock jitter. Indeed, if the time constant τ_i is sufficiently smaller than the sampling period ($T_{ADC} = 1/f_{ADC}$), the current injected in the integrator summing node goes inherently to zero before the end of each cycle and, therefore, the amount of charge transferred is well controlled and constant (given by Q), independently of clock jitter. Obviously, the on-resistance R_{on} of switches M_1-M_2 and M_7-M_8 must be negligible with respect to $R_{ri,j}$ ($R_{on} \ll R_{ri,j}$), so that the value of τ_i is well defined. To limit the charge injection, dummy switches (M_9-M_{10}) have been used.

Being the quantizer resolution 5 bits, 31 DAC levels are required, which are obtained with 31 identical SCR branches. To ensure a constant capacitive load, independently of the input signal level, 31 capacitors are always connected to both V_{ref+} and V_{ref-} in the fully-differential structure. This is achieved by properly encoding the output signal of the quantizer in order to always connect the capacitors to the reference voltages in complementary mode.

The feedback branch of the first integrator is the dominant jitter error source in the CT ΣΔM and, therefore, τ_i should be sized accurately. On the other hand, the feedback branches of the other integrators can be sized less aggressively, because the jitter error is shaped. An analytical calculation of the resulting input-referred in-band jitter noise [20] for the first integrator feedback path leads to

$$V_{n,J}^2 = \frac{\Delta^2 \sigma_t^2 \mathrm{e}^{-T_{ADC}/\tau}}{T_{ADC}^2 OSR}, \tag{9}$$

where σ_t^2 is the variance of the clock period and Δ is the DAC step amplitude. Furthermore, the capacitor size used in the DAC cannot be arbitrary, but depends on the input-referred

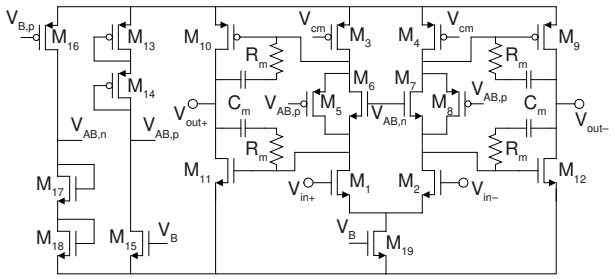

Fig. 14. Schematic of the operational amplifier used in the first integrator

noise contribution tolerated to meet the *SNR* requirement, which for the first integrator is given by

$$V_{n,C}^2 = \frac{2kT}{31C_{r1,j}OSR}, \tag{10}$$

where k is the Boltzmann constant and T the absolute temperature. Using (9) and (10) the values of τ_i have been chosen as $\tau_1 = 7.5T_{ADC}$, $\tau_2 = 1.5T_{ADC}$, and $\tau_3 = 3T_{ADC}$, leading to $R_{r1,j} = 20$ kΩ, $C_{r1,j} = 600$ fF, $R_{r2,j} = 30$ kΩ, $C_{r2,j} = 55$ fF, $R_{r3,j} = 25$ kΩ, and $C_{r3,j} = 153$ fF.

B. Integrators

The SCR DAC introduces more stringent settling requirements in the integrator than a resistive or current steering DAC. Indeed, to follow correctly the feedback pulse, the integrator bandwidth and slew-rate have to be larger than in conventional solutions. However, they can still be smaller then in a switched-capacitor ΣΔM, since the rising and falling times of the DAC pulses are limited by τ_i. Moreover, the first integrator determines the overall noise and linearity of the modulator and, hence, low flicker noise and high linearity are also required. Therefore, in order to minimize the power consumption, a two-stage unfolded class-AB operational amplifier is used in the first integrator. This operational amplifier, whose schematic is shown in Fig. 14, achieves better power efficiency than a folded-cascode or two-stage, class-A topology, requiring a lower quiescent current for the same performance [21]. Two important parameters of the push-pull, rail-to-rail output stage of this operational amplifier, formed by M_9-M_{10} and M_{12}-M_{11}, are the output voltage range and the maximum output current that can be supplied to the load. Indeed, the integrator output swing required in the CT ΣΔM without feedforward paths is pretty large. Therefore, in order to allow proper operation, the maximum differential input voltage has been fixed to 400 mV (−8 dB_{FS}) and the aspect ratio of the output transistors has been chosen as large as possible to achieve rail-to-rail output swing. The virtual battery inserted between M_9-M_{10} and M_{12}-M_{11} ensures the proper biasing (quiescent current), while the available output current is determined by the aspect ratio of M_9-M_{10} and M_5-M_8. In the used class-AB topology each gain stage requires a separate common-mode feedback (CMFB) circuit, which is realized with a conventional CT structure. Miller-compensation (R_m and C_m) is used to guarantee stability. The simulated Bode diagram

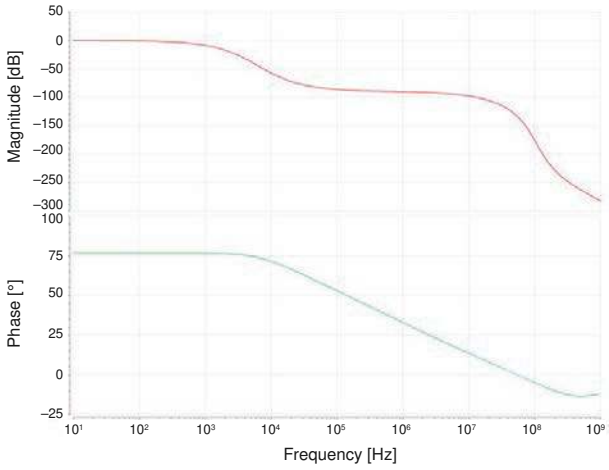

Fig. 15. Simulated Bode diagram of the operational amplifier used in the first integrator

TABLE III
SIMULATED PERFORMANCE OF THE OPERATIONAL AMPLIFIERS

Parameter	Integrator		
	First	Second	Third
GBW [MHz]	50	80	80
DC Gain [dB]	66	50	50
Phase Margin [°]	50	58	58
Current [μA]	800	170	170

of the amplifier is reported in Fig. 15. The achieved gain-bandwidth product (*GBW*) is 50 MHz with 50° phase margin.

The performance required for the operational amplifiers used in the second and third integrators are more relaxed and can be easily obtained with a conventional two-stage operational amplifier. Moreover, the noise introduced by these amplifiers is attenuated by the first integrator gain. The performance obtained for the different operational amplifiers are summarized in Tab. III.

C. Quantizer

The quantizer in a ΣΔM is not a very critical circuit block in terms of noise and distortion, because of the large gain of the preceding integrators. Therefore, a flash ADC is the natural choice, since it allows the A/D conversion to be performed in just one clock period. The implemented flash ADC, shown in Fig. 16, features 32 levels, realized with 31 comparators that compare the input signal with a reference voltage ladder.

The reference voltages ($V_{ref,0} \cdots V_{ref,30}$) are realized through a resistive divider connected to a dedicate power supply. The 31 voltage levels are centered around the common mode voltage ($V_{CM} = 550$ mV) and cover the required signal swing with 20-mV steps. The unit resistance of the divider has been fixed to 1 kΩ to reduce the quiescent current consumption (24 μA). With the used technology, this resistance value guarantees a mismatch $\Delta R/R < 1.8\%$.

The schematic of the comparator used is shown in Fig. 17. The circuit consists of two stages. The first stage, a continuous-time fully differential pre-amplifier, performs the difference

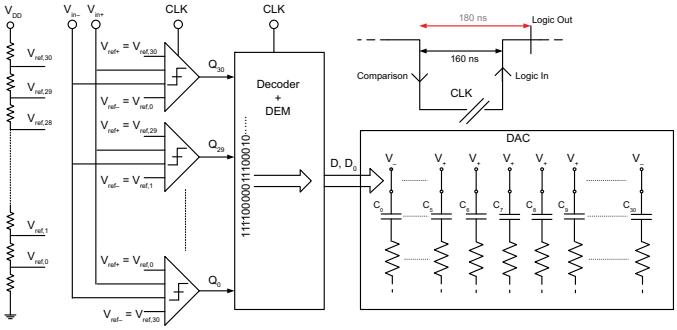

Fig. 16. Schematic of the quantizer

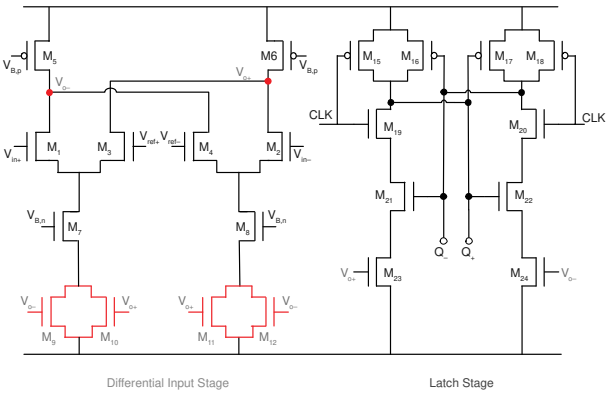

Fig. 17. Schematic of the comprator

between the input signals and compares it with the difference between the threshold voltages, according to

$$V_{o-} = A\left[\left(V_{ref+} - V_{in+}\right) - \left(V_{ref-} - V_{in-}\right)\right], \quad (11)$$

$$V_{o+} = A\left[\left(V_{ref-} - V_{in-}\right) - \left(V_{ref+} - V_{in+}\right)\right], \quad (12)$$

where A is the DC-gain of the pre-amplifier. The output common-mode voltage of the pre-amplifier is controlled by a CMFB based on MOS transistors working in the triode region (M_9, M_{10}, M_{11}, and M_{12}). The amplified difference between the input signals and the threshold voltages ($V_{o+} - V_{o-}$) is then passed to the latch stage, which, on the positive edge of the clock, determines the digital output signals (Q_+ and Q_-). The continuous-time pre-amplifier reduces the comparator kick-back on the third integrator output and guarantees a constant input capacitance. The total current consumption of the comparator is equal to 10 µA.

D. Dynamic Element Matching (DEM)

To improve the matching of the feedback DAC capacitors, a dynamic element matching (DEM) technique is used [22] for the first integrator. DEM techniques are based on cyclic exchanges of reference elements in the DAC. As a result, the mismatch among the elements is averaged out, thus avoiding signal distortion.

The main problem in the implementation of DEM techniques in CT ΣΔMs is the excess loop delay eventually introduced by the DEM, which may lead to instability. For this reason, we implemented a simple data weighted averaging (DWA) algorithm, that only requires one logical step to achieve the randomization of the elements. Basically, as shown in Fig. 16, the thermometric code produced by the quantizer ($Q_0 \cdots Q_{30}$) is transformed into a binary code D. As a consequence, in the DAC, for one branch of the differential structure D elements are connected to V_{ref+}, while $31 - D$ elements are connected to V_{ref-}, and viceversa for the other. A pointer stores the position of the last used DAC element (D_0), so that the next D required elements are selected starting from D_0. The value of D_0 is then updated to $D_0 + D$.

This solution ensures that the DEM introduces just a small fixed time delay. Indeed, the total time required to generate the DAC control bits from the comparator input is just over half clock period, which ensures the stability of the CT ΣΔM.

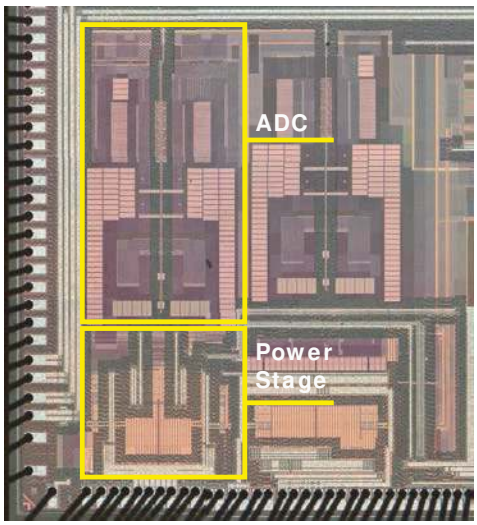

Fig. 18. Micrograph of the test chip including the CT ΣΔM and the HV (5-V) power stage

V. Experimental Results

The critical part of the digital class-D amplifier, that includes the CT ΣΔM and the HV (5-V) power stage, has been integrated with a 40-nm CMOS technology. Fig. 18 shows the test chip micrograph. The CT ΣΔM area is 0.66 mm^2, while the power bridge occupies 0.33 mm^2.

The CT ΣΔM operates from a 1.1-V power supply and consumes 1.6 mA, achieving 101-dB *DR* and 72-dB peak *SNDR*, as shown in Fig. 19. The *SNDR* degradation for input signals above −40 dB$_{FS}$ is due to an increase of the noise-floor, while above −20 dB$_{FS}$ distortion becomes dominant, as shown in the spectra reported in Fig. 20. The noise floor increase for large signals is due to cross-coupling between the digital output and the DAC reference voltages, since the reference buffers have been undersized to save power (and increase the class-D amplifier efficiency). This noise floor increase has little effect on the class-D amplifier performance, considering the requirements illustrated in Fig. 19 (for large signals more noise is tolerated since it is not perceived on the loudspeakers). Tab. IV summarizes the achieved performance.

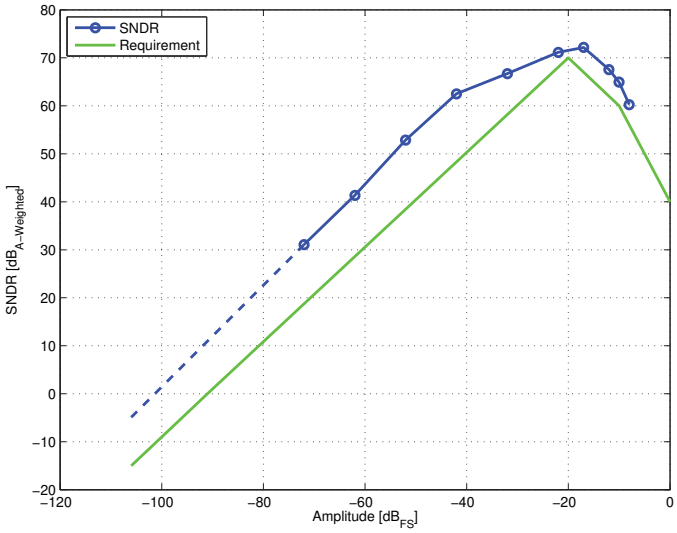

Fig. 19. *SNDR* of the CT ΣΔM as a function of the input signal amplitude at 1 kHz and *SNDR* requirements

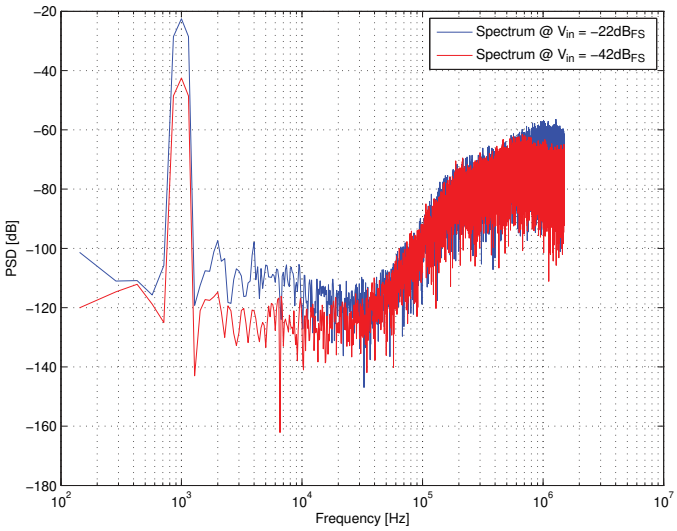

Fig. 20. Spectra of the CT ΣΔM output signal with −42-dB$_{FS}$ and −22-dB$_{FS}$, 1-kHz input signals

TABLE IV
PERFORMANCE SUMMARY OF THE CT ΣΔM

Parameter	**Value**
Technology	40-nm CMOS
CT ΣΔM area	0.66 mm^2
Power stage area	0.33 mm^2
CT ΣΔM supply voltage	1.1 V
Power stage supply voltage	5 V
CT ΣΔM power consumption	1.7 mW
CT ΣΔM full-scale signal	0.4 V
CT ΣΔM bandwidth	24 kHz
CT ΣΔM *DR*	101 dB
CT ΣΔM peak *SNDR*	72 dB
CT ΣΔM AAF	Third order
CT ΣΔM AAF cut-off frequency	150 kHz

VI. CONCLUSIONS

In this paper we introduced a closed-loop digital class-D amplifier for portable audio application, focusing, in particular, on the CT third-order ΣΔM used to close the feedback loop. The proposed ΣΔM, implemented in a 40-nm CMOS technology, occupies 0.66 mm^2 and achieves 101 dB of *DR* and 72 dB of peak *SNDR*, consuming 1.7 mW from a 1.1-V power supply. Thanks to the active-RC implementation the 1.1-V ΣΔM inputs can be directly connected to the 5-V class-D amplifier power stage outputs. The inherent third-order AAF of the ΣΔM attenuates by at least 35 dB the PWM spur components present in the class-D amplifier output voltage.

REFERENCES

[1] L. Dooper and M. Berkhout, "A 3.4-W digital-in class-D audio amplifier in 0.14-μm CMOS," *IEEE Journal of Solid-State Circuits*, vol. 47, no. 7, pp. 1524–1534, Jul. 2012.

[2] D. Cartasegna, P. Malcovati, L. Crespi, K. Lee, L. Murukutla, and A. Baschirotto, "An audio 91-dB THD third-order fully-differential class-D amplifier," in *Proceedings of European Solid-State Circuit Conference (ESSCIRC)*. Helsinki, Finland, Sep. 2011, pp. 91–94.

[3] M. Berkhout and L. Dooper, "Class-D audio amplifiers in mobile applications," *IEEE Transactions on Circuits and Systems—Part I: Regular Papers*, vol. 57, no. 5, pp. 992–1002, May 2010.

[4] B. H. Gwee, J. S. Chang, and V. Adrian, "A micropower low-distortion digital class-D amplifier based on an algorithmic pulse-width modulator," *IEEE Transactions on Circuits and Systems—Part I: Regular Papers*, vol. 52, no. 10, pp. 2007–2022, Oct. 2005.

[5] V. Adrian, J. S. Chang, and B. H. Gwee, "A low-voltage micropower digital class-d amplifier modulator for hearing aids," *IEEE Transactions on Circuits and Systems—Part I: Regular Papers*, vol. 56, no. 2, pp. 337–349, Feb. 2009.

[6] R. Cellier, E. Allier, A. Nagari, C. Crippa, R. Bassoli, G. Pillonnet, and N. Abouchi, "A fully-differential digital input class-D with EMI spreading method for mobile application," in *Proceedings of Audio Engineering Society Convention (AES)*, vol. 37, Aug. 2009, p. 17.

[7] F. Guanziroli, R. Bassoli, C. Crippa, D. Devecchi, and G. Nicollini, "A 1-W 104-dB SNR filter-less fully-digital open-loop class-D audio amplifier with EMI reduction," *IEEE Journal of Solid-State Circuits*, vol. 47, no. 3, pp. 686–698, Mar. 2012.

[8] T. Ido, S. Ishizuka, L. Risbo, F. Aoyagi, and T. Hamasaki, "A digital input controller for audio class-D amplifiers with 100 W 0.004% THD+N and 113 dB DR," in *IEEE International Solid-State Circuit Conference Digest of Technical Papers (ISSCC)*. San Francisco, CA, USA, Feb. 2006, pp. 1366–1375.

[9] W. Shu and J. S. Chang, "Power supply noise in analog audio class-D amplifiers," *IEEE Transactions on Circuits and Systems—Part I: Regular Papers*, vol. 56, no. 1, pp. 84–96, Jan. 2009.

[10] T. Koeslag, F.; Mouton, "Accurate characterization of pulse timing errors in class-D audio amplifier output stages," in *Proceedings of International AES Conference on Class-D Audio Amplification*, vol. 37, Aug. 2009, p. 15.

[11] D. Cartasegna, P. Malcovati, L. Crespi, K. Lee, and A. Baschirotto, "A design methodology for high-order class-D audio amplifiers," *Analog Integrated Circuits and Signal Processing*, vol. 78, no. 3, pp. 785–798, Mar. 2014.

[12] W. Shu and J. S. Chang, "THD of closed-loop analog PWM class-D amplifiers," *IEEE Transactions on Circuits and Systems—Part I: Regular Papers*, vol. 55, no. 6, pp. 1769–1777, Jul. 2008.

[13] A. Donida, P. Malcovati, R. Cellier, A. Nagari, and A. Baschirotto, "A 40-nm CMOS, 1.1-V, 101-dB DR, 1.7-mW continuous-time ΣΔ ADC for a digital closed-loop class-D amplifier," in *Proceedings of IEEE International Conference on Electronics Circuits and Systems (ICECS)*. Abu Dhabi, United Arab Emirates, Dec. 2013, pp. 437–440.

[14] R. Cellier, G. Pillonnet, A. Nagari, and N. Abouchi, "A review of fully digital audio class-D amplifiers topologies," in *Proceedings of IEEE Northeast Workshop on Circuits and Systems (NEWCAS)*. Toulouse, France, Jun. 2009, pp. 1–4.

[15] R. W. Erikson and D. Maksomovic, *Fundamentals of Power Electronics*. Springer Science, 2001.

[16] G. F. Franklin, *Digital Control of Dynamic Systems*, 3rd ed. Addison Welsey, 1998.

[17] R. Schreier, "Delta-Sigma Toolbox – High-level design and simulation of delta-sigma modulators." [Online]. Available: www.mathworks.com

[18] L. Dorrer, F. Kuttner, A. Santner, C. Kropf, T. Hartig, P. Torta, , and P. Greco, "A 2.2-mW, continuous-time sigma-delta ADC for voice coding with 95 dB dynamic range in a 65-nm CMOS process," in *Proceedings of European Solid-State Circuit Conference (ESSCIRC)*. Montreux, Switzerland, Sep. 2006, pp. 195–198.

[19] S. Pavan, N. Krishnapura, R. Pandarinathan, and P. Sankar, "A power-optimized continuous-time sigma-delta ADC for audio applications," *IEEE Journal of Solid-State Circuits*, vol. 43, no. 2, pp. 351–360, Feb. 2008.

[20] M. Ortmanns, F. Gerfers, and Y. Manoli, "A continuous-time sigma-delta modulator with reduced sensitivity to clock jitter through SCR feedback," *IEEE Transactions on Circuits and Systems—Part I: Regular Papers*, vol. 52, no. 5, pp. 875–884, May 2005.

[21] F. Cannillo, E. Prefasi, L. Hernandez, E. Pun, F. Yazicioglu, and C. V. Hoof, "1.4-V 13-μW 83-dB DR CT sigma-delta modulator with dual-slope quantizer and PWMDAC for biopotential signal acquisition," in *Proceedings of European Solid-State Circuit Conference (ESSCIRC)*. Helsinki, Finland, Sep. 2011, pp. 267–270.

[22] R. T. Baird and T. S. Fiez, "Linearity enhancement of multibit ΣΔ A/D and D/A converters using data weighted averaging," *IEEE Transactions on Circuits and Systems—Part II: Analog and Digital Signal Processing*, vol. 42, no. 12, pp. 753–762, Dec. 1995.