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Semi-Automated Analog Placement

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Abstract—Analog design remains a manual task because of the complexity of the interactions among devices. Automation tools dedicated to analog circuits are not as mature as the digital automation ones, but have been improved a lot at a point that they can help at individual steps in the analog design flow. Our approach is to propose a semi-automated analog placement controlled by the designer, following an organization in row similar to a digital circuit structure. The results show the ability of our tool at generating multiple layouts respecting designer's constraints.

I. BACKGROUND OF THE PROBLEM

Today system-on-chip contains both digital and analog circuits. Even though most functions in an integrated circuit are implemented with digital circuitry, some functions rely on analog circuit and are the link with the external world. Despite the fact that the digital design flow has been well-defined over the last years, the analog design flow lacks a common methodology making it difficult to capture a design procedure.

An automatic placement tool should produce analog device-level layouts similar in density and performance to the high-quality manual layouts. To achieve this task, the capability to deal with layout constraints, in order to decrease unwanted parasitics due to the fabrication process, is mandatory. [1] enumerates the most common placement constraints that are respected by modern analog placer where symmetries [2] are the most used constraints.

Although most of the recent works focus on highly automated approaches such as the simulated annealing algorithm [3], we believe that giving more control to designers and using their interventions to set some constraints yield good analog placement results. In this work, we introduce a semi-automatic analog placement approach guided by designers' preferences. This semi-automatic approach also helps designers to debug more efficiently and makes adjustments easier since they will control the overall relative placement of the circuit but at the same time, some tiresome and error-prone tasks are automated.

II. ORIGINAL KEY IDEA OF THE STUDY

A. Design Flow

The Cairo Hurricane AMS (CHAMS) project [4], developed by the LIP6 Laboratory, proposes a complete flow to create a library of highly reconfigurable analog circuits, and specially

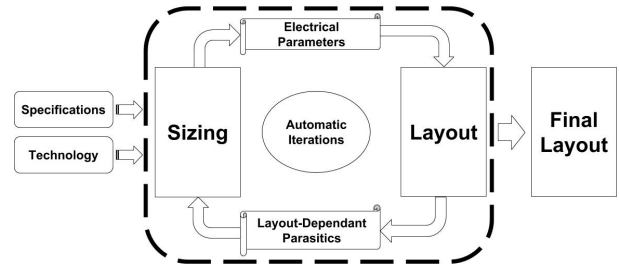


Fig. 1. Cairo Hurricane AMS Design Flow

to automatically generate and optimize the layout with little intervention from designers. The flow provides a reliable and efficient solution taking into account parasitic effect-aware layout generation with enough flexibility to adapt to different designers needs and concerns. Our layout generation tool supports any technology with the new nanometric layout dependent parasitic parameters.

The proposed CHAMS analog design (fig. 1) is a two way communication between the sizing and layout generation. The idea is that the sizing tool provides the electrical parameters of the transistor such as the width, length, number of fingers, etc... to the layout generation tool. The tool automatically generates the layout from a library of parameterized cells and sends back to the sizing engine the layout-dependent parasitic parameters such as the drain and source areas and perimeters, the stress effect parameters, etc... to re-evaluate the performance. This internal loop is repeated several times, with minimal designers intervention, until the target specifications are met.

B. Placement in row

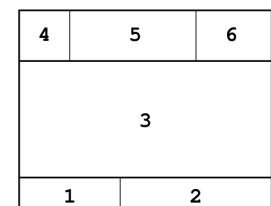
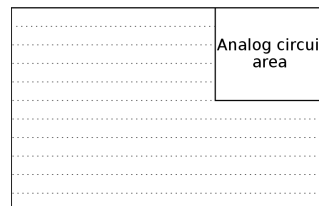


Fig. 2. Mixed-signal circuit floorplanning

Fig. 3. Analog placement in three rows

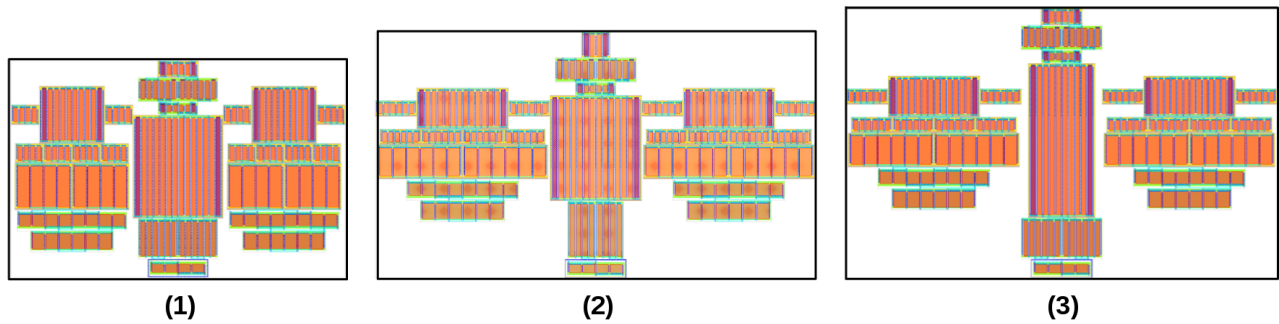


Fig. 4. Layouts of the fully differential transconductor [5]. All figures have the same scale.

Digital and analog circuits have a dedicated area on a system-on-chip circuit so they can be independently designed within a specific space (fig. 2). Digital circuits are well-known for their regular row structure where standard cells are placed and routed accordingly to their netlist. In a similar way, we plan to organize the analog circuit layout in rows of devices and the analog circuit area should be placed and routed within its dedicated area (fig. 3).

It is common to design analog circuit in rows of devices where the height of each row of devices should be adjustable so it can match its dedicated area. Therefore, we choose the slicing tree representation for several reasons:

- Slicing trees are a natural choice to describe a row structure. Rows are represented by horizontal slices which will be divided into vertical slices determined by the area of each device. Since the devices will rarely have the same height, we introduce a margin parameter, which represents the largest difference between the smallest and the tallest devices' heights in the same row.
- Unlike most of modern analog placement methods, our placement strategy is semi-automatic and will be guided by designers' preferences. Slicing trees are easy to handle and let designers choose the overall topology.

III. RESEARCH THAT HAS BEEN CARRIED OUT SO FAR

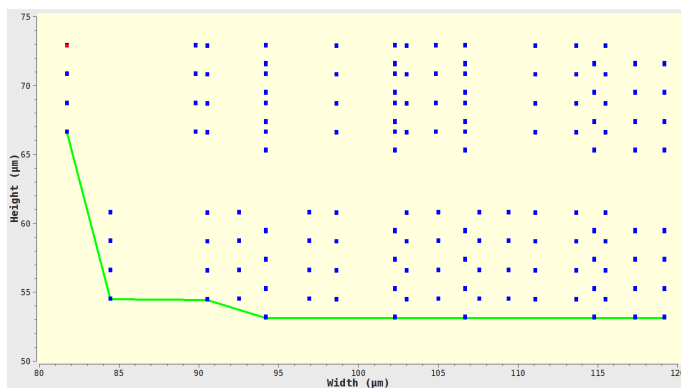


Fig. 5. Circuit's dimensions, showing heights as function of widths

Our tool was implemented in C++ programming language on a Intel(R) Core(TM) i5-4590S CPU @ 3.00 GHz workstation with 6 GB RAM. To illustrate the capability of our tool, we experiment it on a fully differential transconductor [5], designed in a 130 nm CMOS technology. The fully differential transconductor consists of a total of 32 devices and we consider 2 possible variations for each device. The slicing tree takes into account 11 symmetries for this circuit and tolerance margins are set in a way to have reasonable amount of accepted possibilities. Designers can choose their final placement based on their experiences and preferences. Our tool presents the placement results (fig. 4) plotted on a graph (fig. 5) with heights and widths as axis and can be selected interactively to be placed in a few seconds.

IV. DISCUSSION OF THE CONTRIBUTION

Slicing tree structure is a structure that has been studied over the last decades and its drawbacks are well-known. It is in a way restrictive since there are some topologies that cannot be represented with a slicing tree which can be a problem. Moreover, it does not extend to non-rectangular structures and has a bad white space distribution. Nevertheless, we are quite satisfied with the slicing tree structure which is able to handle the organization in row.

For future considerations, even though the white space distribution can be a disadvantage, we plan to exploit it during the routing step that needs to be performed. Our floorplan representation and algorithm have been thought according to the analog routing step that we plan to develop in the future.

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