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Experimental Evaluation of IGBT Junction Temperature Measurement via a Modified- V_{CE} (ΔV_{CE_AVGE}) Method with Series Resistance Removal

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Abstract

Temperature sensitive electrical parameters (TSEPs) allow junction temperature measurements on power semiconductors without modification to module packaging. The on-state collector-emitter voltage (V_{CE}) in IGBTs is an attractive option for junction temperature measurement since it is relatively easy to measure during operation. Nevertheless, the resistive contribution of interconnection and packaging materials has been shown to introduce large errors when using the V_{CE} for junction temperature measurement. This paper uses an IR camera to experimentally evaluate a modified- V_{CE} method designed to remove this series resistance contribution. This method can be described as the difference in V_{CE} at two different gate voltages (15V and 13V). Experimental validation focuses primarily on the accuracy of the temperature measurement and investigates paralleled chip configurations as well as multiple devices with differing geometry and manufacturer. The modified- V_{CE} shows significant improvement over the normal- V_{CE} in terms of correlation to mean junction temperature, with maximum errors typically below 10°C. These results are additionally compared with one traditional and robust TSEP: the voltage drop under low current injection.

1 Introduction

1.1 Background

Knowledge of junction temperature in Insulated-gate Bipolar Transistors (IGBTs) during the operation of power electronic converters can improve condition monitoring systems and enhance power module lifetime [1]

Real time junction temperature measurement is however often difficult. Physical or contact measurement methods such as optical fibres, on-chip sensors, or infra-red cameras are expensive and require substantial modification to standard power module packaging. Electrical methods however can be advantageous. Using a Temperature Sensitive Electrical Parameter (TSEP), such as the on-state voltage drop or threshold voltage, junction temperature measurements can be performed on standard power modules without modification to their structure [2-4].

Electrical methods for junction temperature measurement have been used for many decades on transistors, particularly for offline thermal characterisation of devices. Nevertheless, examples of TSEP-based methods being used online (i.e. during normal transistor operation) are still limited [4].

This paper focuses specifically on the use of the on-state collector-emitter voltage (V_{CE}) at high current for IGBT junction temperature measurement. The V_{CE} is an attractive method for a number of reasons: it is relatively easy to extract during operation [5,6] and it can be used on all IGBT devices. However, junction temperature measurement using the V_{CE} at high current has several problems. The most critical of these is vastly erroneous measure-

ments due to the inherent series resistance contribution of bond wires and packaging [7,8].

Recently, two methods have been tentatively proposed to mathematically remove the series resistance contribution from the V_{CE} . These investigations have thus far only been conducted on one single IGBT [7].

This paper takes one of these methods that is most suited for online use and extends the experimental verification to a variety of chips with differing geometry and manufacturer. Temperature measurements will be made under steady-state current injection and validated with an IR camera. The IGBT chips selected for evaluation are all rated for 1200V and are as follows. Where possible, IGBTs are also assessed in paralleled configuration.

1. **Infineon** – Chip: *IGC189T120T8RL*, Module: *FS200R12PT4*, square chip, 1.2kV-200A.
2. **Infineon** – Chip: *IGC193T120T8RM*, Module: *FF600R12ME4*, rectangular chip, 1.2kV-200A.
3. **Fuji** – Chip: *Unknown*, Module: *6MB1100VA-120-50*, square chip, 1.2kV-100A.

First, the paper will provide a brief description of the modified- V_{CE} method (referred to as ΔV_{CE_AVGE}), the test bench, and some details on the calibration procedure. Results and comparison with IR measurements will then be presented for the three different chips.

1.2 Modified- V_{CE} Method - ΔV_{CE_AVGE}

In a first approximation, the measurement principle investigated in this paper is simple and can be demonstrated mathematically as follows:

$$V_{CE1} = V_{IGBT}(V_{GE1}, I_L) + I_L R \quad \text{Eq.1}$$

$$V_{CE2} = V_{IGBT}(V_{GE2}, I_L) + I_L R \quad \text{Eq.2}$$

$$V_{CE1} - V_{CE2} = V_{IGBT}(V_{GE1}, I_L) - V_{IGBT}(V_{GE2}, I_L) \quad \text{Eq.3}$$

The basic premise of the method is to take two V_{CE} measurements in quick succession at two different levels of V_{GE} (15V and 13V). The measurements should also be performed at the same current level. Providing that the two V_{CE} measurements are taken sufficiently quickly (under 200 μ s), the temperature in the junction and interconnections can be assumed constant. In this case, the voltage drop across the chip will fluctuate while the voltage drop across the resistive materials remains stable. Therefore, one V_{CE} measurement can be subtracted from the other in order to mathematically reduce the resistive contribution to zero.

2 Test Setup

2.1 Test Bench

An experimental setup is developed in order to experimentally evaluate TSEP junction temperature measurement methods. TSEPs are evaluated in a steady state thermal condition under constant current injection. The test bench with IR camera (CEDIP-FLIR SC7500) can be seen in Fig. 1.

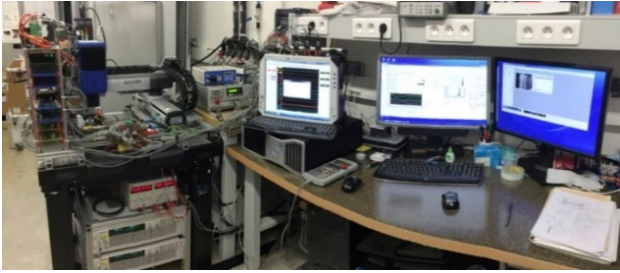


Figure 1 Test Bench with IR Camera

The test bench allows campaigns on a large number of devices in a semi-automatic mode. In particular, IR measurements are made with great care. The positioning of the IR camera is controlled by a 3-axis positioning system in order to attain repeatable image positioning on the chip under test, as well as to perform non-uniformity corrections corresponding to the desired temperature range.

Dielectric gel is removed from commercial power modules via soaking in Ardrex 2312 and cleaning with Acetone and deionised water. Chips are black painted with a thickness between 10-16 μ m with care taken to achieve as consistent emissivity as possible across the surface.

2.2 TSEP Measurements

In order to perform a thorough evaluation of the ΔV_{CE_AVGE} method, four methods of junction temperature measurement are used in total:

1. **IR Camera:** an IR camera is used to extract the mean temperature of the chip surface (IR_{Mean}).
2. **ΔV_{CE_AVGE} :** V_{GE} is briefly lowered from 15V to 13V during high current injection.

3. **Normal V_{CE} :** the V_{CE} value at high current with V_{GE} at a stable 15V (V_{CE}).
4. **$V_{CE(low)}$:** the V_{CE} at a low current injection of between 100-200mA ($V_{CE(low)}$). This is chosen due to its traditional use and repeated evidence of correlation with mean junction temperature [7,9,10] – at low currents, ohmic contribution is negligible.

2.3 Measurement Synchronisation

A constant current is fed into the device for several minutes until a thermal steady state is reached. At this point, junction temperature measurement using the above methods is performed.

Fig. 2 presents the sequencing of the electrical temperature measurements. In this case, $I_{DUT}=250A$ for two IGBTs connected in parallel, and has been constant for several minutes. Between -2000 μ s and -1750 μ s, several measurements of V_{CE} and I_{DUT} are recorded. Immediately after, V_{GE} is reduced from 15V to 13V for a period of 200 μ s. In this period, several measurements of V_{CE} and I_{DUT} are again recorded. This data is then used for the TSEPs ΔV_{CE_AVGE} and normal- V_{CE} .

At 0 μ s, I_{DUT} is removed and a low sensing current of 100mA/chip (200mA in total for two paralleled chips) is injected. The $V_{CE(low)}$ is then recorded from 150 μ s to 400 μ s and an extrapolation vs. the square root of time is used to estimate the junction temperature at 0 μ s [3]. The full I_{DUT} of 250A is then returned to the IGBT. IR measurements are performed one second before the commencement of the electrical measurements.

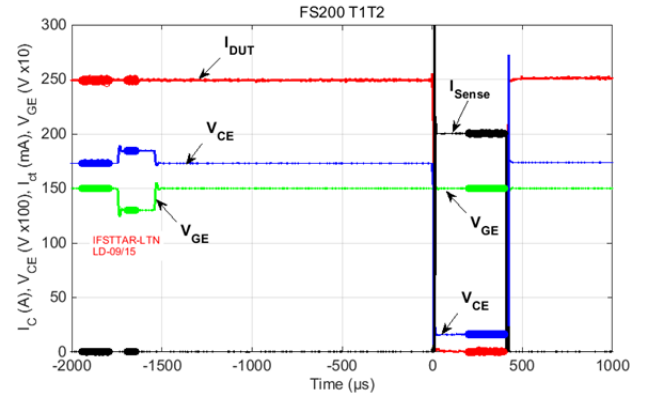


Figure 2 Sequencing of electrical measurements for TSEP junction temperature estimation

2.4 TSEP Calibration

All TSEP measurements are calibrated by varying the baseplate temperature from 40-180C and taking the appropriate electrical measurements. Calibration temperature is recorded using an open thermocouple (Type K, Class 2, $\pm 2.5^\circ C$) placed on the copper layer of the DCB substrate. The thermocouple temperature has been verified using the IR camera, with a maximum difference always lower than 2.2 $^\circ C$ in the range of 40 $^\circ C$ to 180 $^\circ C$.

The $V_{CE(low)}$ is the only TSEP that can be calibrated without inducing self-heating, since the sense current is negligible. For the V_{CE} and ΔV_{CE_AVGE} high current calibrations, the $V_{CE(low)}$ is used to compensate for self-heating.

2.5 Self-heating Calibration Compensation

Although current pulses are kept short (300 μ s) during calibration of V_{CE} and ΔV_{CE_AVGE} , self-heating cannot be assumed negligible at high current levels. Therefore, an estimation of the chip(s) temperature is performed using the TSEP $V_{CE(low)}$ both before and after the calibration current pulse. Fig. 3 shows the sequencing of this procedure. The 100mA sensing current is run continuously. Between -100 μ s and 0 μ s, the $V_{CE(low)}$ can be used directly to estimate chip temperature. After 300 μ s, the calibration pulse ends and there is a short delay of around 10 μ s before the sense current is again stable. After which, the $V_{CE(low)}$ is recorded over time and extrapolated to estimate the chip temperature at the end of the pulse.

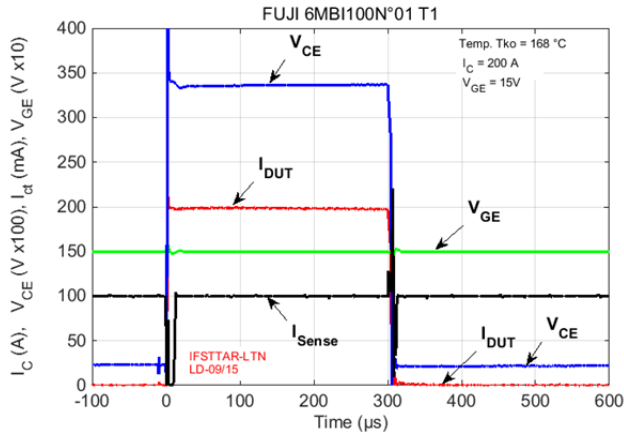


Figure 3 Sample high current calibration pulse

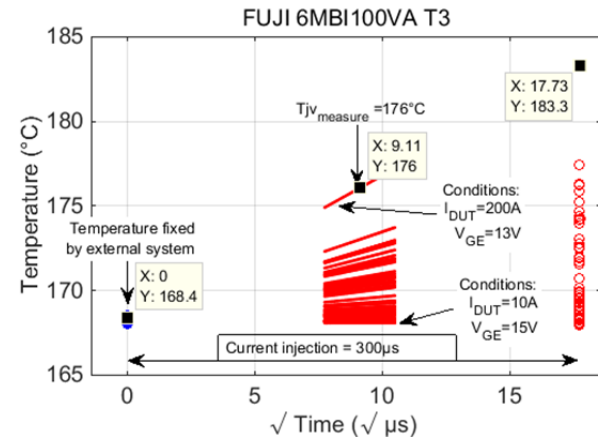


Figure 4 Increase of device temperature due to self-heating during calibration. Measured via $V_{CE(low)}$.

The electrical measurements required for calibration of V_{CE} and ΔV_{CE_AVGE} are taken towards the end of the pulse. Fig. 4 displays an evaluation of the self-heating that occurs during these pulses on the Fuji 6MBI100VA-120-50. It can be seen that, in a worst case scenario (high starting baseplate temperature, very high current and 13V gate voltage) we estimate that the self-heating can be more than 15 $^{\circ}$ C. These results are subsequently taken into account when processing calibration data.

3 Calibration Results

3.1 Calibration Results

The temperature sensitivities for the three TSEPs on single IGBT chips at low and high current levels are displayed in Table 1. Two IGBTs are calibrated from each module. It can be seen that the sensitivity of ΔV_{CE_AVGE} appears reasonably consistent for devices from the same manufacturer. Fuji IGBTs displayed a sensitivity of +0.85mV/ $^{\circ}$ C and +0.87mV/ $^{\circ}$ C at 120A, while Infineon IGBTs were around +0.36mV/ $^{\circ}$ C.

We believe that the sensitivity discrepancies of T1 in the Infineon FF600 module is a result of a measurement error or device degradation, since $V_{CE(low)}$ on this chip was calibrated in a previous study and showed a sensitivity of -2.41mV/ $^{\circ}$ C [10], which is consistent with other Infineon IGBTs here.

Table 1 TSEP sensitivity for single IGBT configuration

Module	TSEP	IGBT	Lower Sensitivity @40A	Higher Sensitivity @120A
INFINEON FS200	V_{CE}	T1	-0.42mV/ $^{\circ}$ C	+1.51mV/ $^{\circ}$ C
		T2	-0.42mV/ $^{\circ}$ C	+1.55mV/ $^{\circ}$ C
	ΔV_{CE_AVGE}	T1	+0.10mV/ $^{\circ}$ C	+0.35mV/ $^{\circ}$ C
		T2	+0.11mV/ $^{\circ}$ C	+0.37mV/ $^{\circ}$ C
	$V_{CE(low)}$	T1	-2.41mV/ $^{\circ}$ C @100mA	
		T2	-2.42mV/ $^{\circ}$ C @100mA	
INFINEON FF600	V_{CE}	T1	-0.58mV/ $^{\circ}$ C	+2.05mV/ $^{\circ}$ C
		T2	-0.45mV/ $^{\circ}$ C	+1.50mV/ $^{\circ}$ C
	ΔV_{CE_AVGE}	T1	+0.14mV/ $^{\circ}$ C	+0.49mV/ $^{\circ}$ C
		T2	+0.10mV/ $^{\circ}$ C	+0.36mV/ $^{\circ}$ C
	$V_{CE(low)}$	T1	-2.32mV/ $^{\circ}$ C @100mA	
		T2	-2.43mV/ $^{\circ}$ C @100mA	
FUJI 6MBI100	V_{CE}	T1	+0.83mV/ $^{\circ}$ C	+3.85mV/ $^{\circ}$ C
		T3	+0.76mV/ $^{\circ}$ C	+3.73mV/ $^{\circ}$ C
	ΔV_{CE_AVGE}	T1	+0.18mV/ $^{\circ}$ C	+0.85mV/ $^{\circ}$ C
		T3	+0.18mV/ $^{\circ}$ C	+0.87mV/ $^{\circ}$ C
	$V_{CE(low)}$	T1	-2.25mV/ $^{\circ}$ C @100mA	
		T3	-2.24mV/ $^{\circ}$ C @100mA	

Figure 5 displays a graphical representation of the calibration results for ΔV_{CE_AVGE} on both T1 and T2 from the Infineon FS200. There appears to be a very good correlation between the two chips in both temperature sensitivity and absolute value for ΔV_{CE_AVGE} . This introduces the possibility that just one calibration procedure can be performed and the results transferred to all chips within a batch or module. Nevertheless, more research will be required to ascertain this possibility.

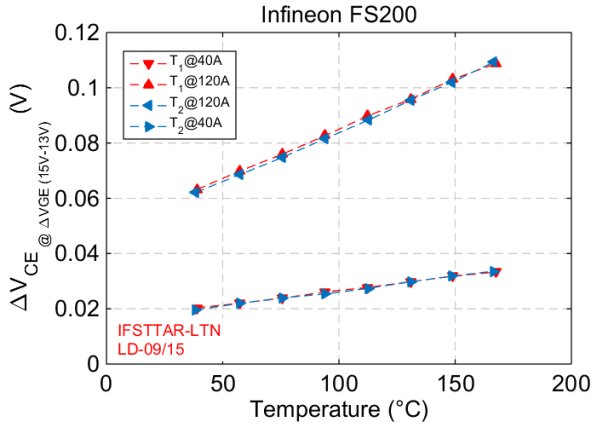


Figure 5 FS200 ΔV_{CE_AVGE} Calibration: Comparison of T1 and T2

3.2 Calibration Results: Paralleled IGBTs

In the case two chips in parallel, the calibration follows the same procedure as for single IGBTs. However, the $V_{CE(low)}$ sensing current used is two times higher (200mA). Results of the calibration of paralleled chips in the FS200 and 6MBI100 modules are displayed in Table 2. The layout of the Infineon FF600 did not provide scope to configure two chips in parallel.

Table 2 TSEP sensitivity for two IGBTs in parallel

Module	TSEP	IGBT	Lower sensitivity @80A	Higher sensitivity @240A
INFINEON FS200	V_{CE_Ip}	T1//T2	-0.40mV/°C	+1.55mV/°C
	ΔV_{CE_AVGE}	T1//T2	+0.11mV/°C	+0.36mV/°C
	V_{CE_Ict}	T1//T2	-2.41mV/°C @200mA	
FUJII 6MBI100	V_{CE_Ip}	T1//T3	+0.77mV/°C	+3.75mV/°C
	ΔV_{CE_AVGE}	T1//T3	+0.18mV/°C	+0.87mV/°C
	V_{CE_Ict}	T1//T3	-2.24mV/°C @200mA	

The sensitivity of each TSEP appears to remain largely unchanged when compared to single IGBTs. This is in contrast to some TSEPs which have a varying sensitivity depending on the number of chips in parallel [11].

4 Dissipation Results

4.1 Single IGBTs

Temperature measurements during dissipation are conducted at a range of current values from 40-160A. The input fluid to the heatsink is maintained at 40°C during all tests.

Dissipation results for T1 in all examined modules are displayed graphically in Figs. 6-8. The figures include temperature measurements made via all investigated TSEPs, along with the mean chip surface temperature as measured via the IR camera (IR_{Mean}). Meanwhile, Table 3 provides the minimum and maximum deviations from IR_{Mean} for each set of TSEP measurements on both T1 and T2.

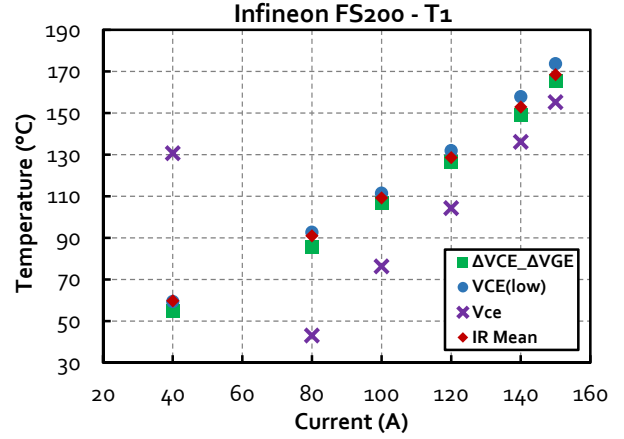


Figure 6 IGBT 1, Infineon FF200; temperature measurement via TSEPs and IR camera during current injection

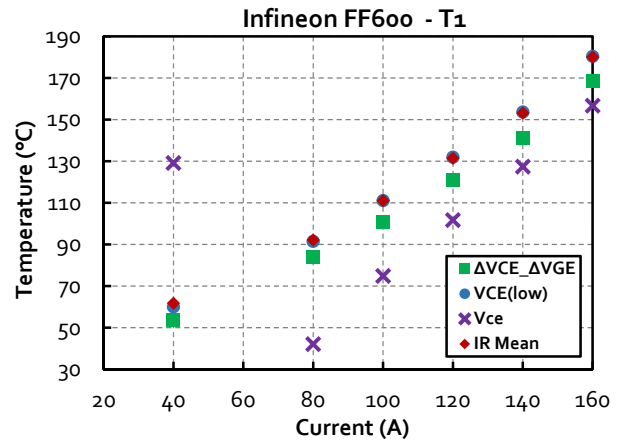


Figure 7 IGBT 1, Infineon FF600; temperature measurement via TSEPs and IR camera during current injection

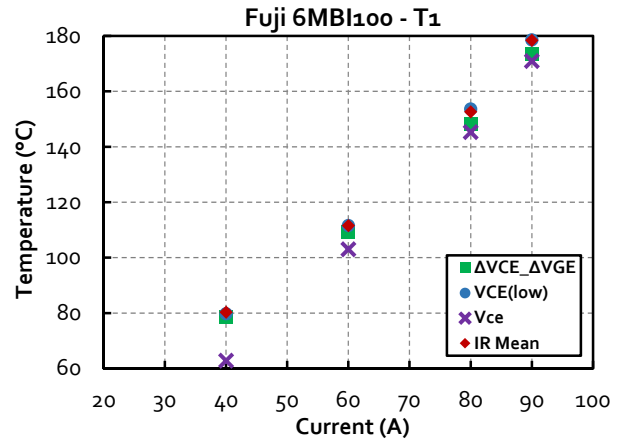


Figure 8 IGBT 1, Fuji 6MBI100; temperature measurement via TSEPs and IR camera during current injection

In the case of the traditional $V_{CE(low)}$ measurement, results are in accordance with previous research and closely match IR_{Mean} , sometimes with a slight overestimation [9]. Clearly, temperature measurement via the normal- V_{CE} led to vastly inaccurate results. These errors can swing from +50°C to -50°C across the current range for chips inside Infineon modules. For the Fuji 6MBI100, the results are markedly better: errors are generally within -20°C, and at

higher current levels this decreases to just a 5°C underestimation of IR_{Mean} .

Nevertheless, the ΔV_{CE_AVGE} temperature measurement method demonstrates significant improvement over the normal- V_{CE} for all chips tested. In the FS200 module, errors of over 50°C with respect to IR_{Mean} are reduced to between -3°C to -7°C. A sizeable error in the region -10°C is observed on IGBTs in the FF600 module, however the error appears to be reasonably consistent throughout all current levels. Once again, the Fuji 6MBI100 module displayed better results in comparison to the Infineon modules, with temperature measurement via ΔV_{CE_AVGE} within -1°C to -6°C of IR_{Mean} .

Table 3 Synthesis of the TSEP deviations from IR_{Mean} for IGBT junction temperature measurement on single chips

Module	TSEP	IGBT	Min_Diff (°C)	Max_Diff (°C)
INFINEON FS200	V_{CE}	T1	-48	+71
		T2	-52	+76
	ΔV_{CE_AVGE}	T1	-3	-7
		T2	-4	-7
	$V_{CE(low)}$	T1	0	+5
		T2	0	+3
INFINEON FF600	V_{CE}	T1	-50	+67
		T2	-50	+78
	ΔV_{CE_AVGE}	T1	-9	-12
		T2	-9	-13
	$V_{CE(low)}$	T1	+1	-2
		T2	+1	-2
FUJI 6MBI100	V_{CE_Ip}	T1	-7	-18
		T3	-5	-11
	ΔV_{CE_AVGE}	T1	-3	-6
		T3	-1	-6
	$V_{CE(low)}$	T1	-1	+1
		T3	-0	+2

4.2 Paralleled IGBTs

Evaluation of two paralleled IGBTs was feasible in the FF200 and 6MBI100 modules. Graphical depiction of these results can be found in Figures 9 and 10. Here, IR_{Mean} is calculated as a single mean temperature comprising of the surface of both IGBTs. Table 4 provides minimum and maximum deviations from IR_{Mean} for each TSEP.

The results follow the largely the same trend as seen with single IGBTs, with ΔV_{CE_AVGE} presenting a large improvement in accuracy over the normal- V_{CE} method. Temperature estimation on the Fuji 6MBI100 is within -5°C of IR_{Mean} , while in the Infineon FS200 the discrepancy was between -5°C and -9°C.

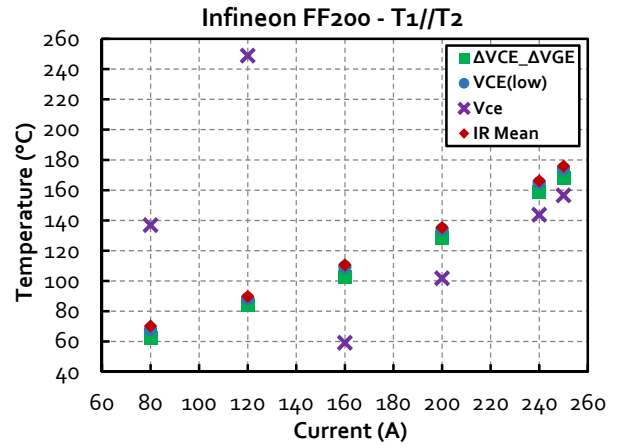


Figure 9 Paralleled IGBTs, Infineon FF200; temperature measurement via TSEPs and IR camera

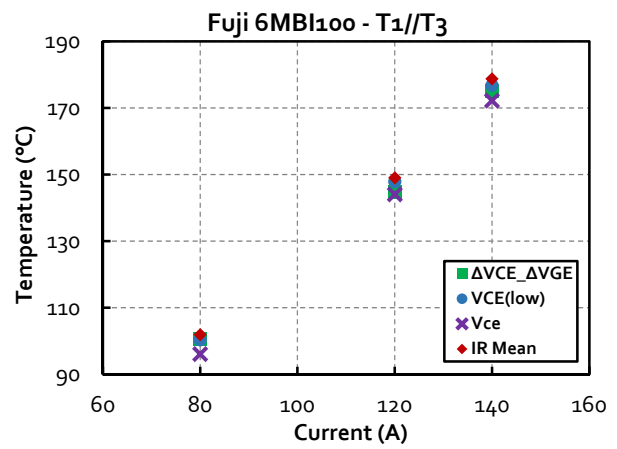


Figure 10 Paralleled IGBTs, Fuji 6MBI100; temperature measurement via TSEPs and IR camera

Table 4 Synthesis of the TSEP deviations from IR_{Mean} for IGBT junction temperature measurement on two paralleled devices

Module	TSEP	IGBT	Min_Diff (°C)	Max_Diff (°C)
INFINEON FS200	V_{CE}	T1//T2	-52	+160
	ΔV_{CE_AVGE}	T1//T2	-5	-9
	$V_{CE(low)}$	T1//T2	-1	-3
FUJI 6MBI100	V_{CE}	T1//T3	-5	-7
	ΔV_{CE_AVGE}	T1//T3	-2	-5
	$V_{CE(low)}$	T1//T3	-1	-2

4.3 Paralleled IGBTs with Temperature Disequilibrium

The Infineon FS200R12PT4 structure allowed a test with a temperature gradient between two paralleled IGBTs. Loosening one side of the module, one chip was left with a worse thermal contact to the heatsink. Fig. 11 displays the results of TSEP temperature measurements in this condition. In these figures, an IR_{Mean} is displayed for each separate chip. The temperature difference between the two IGBTs is more than 20°C at the highest current level.

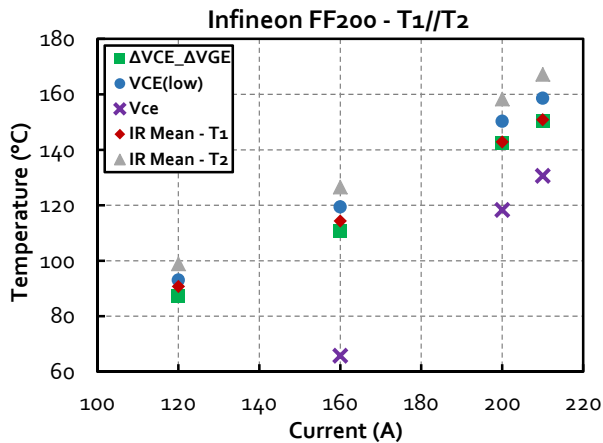


Figure 11 Paralleled IGBTs, Infineon FS200; temperature measurement via TSEPs and IR camera with temperature disequilibrium between chips

While the normal- V_{CE} once again delivers wildly inaccurate results, the ΔV_{CE_AVGE} measurement provided a temperature always IGBT to the chip with the coolest mean temperature (IGBT 1). This is within -4°C of the coolest chip at all current levels.

5 Discussion

The more favourable results experienced on the Fuji 6MBI100 may be explained by viewing the module layout. Fig. 12 displays images of the internal layout of both the Infineon FS200 and Fuji 6MBI100 modules and a schematic of the measurement points used. It can be seen that in the Fuji 6MBI100, a kelvin connection is possible for the measurement of the V_{CE} by using the gate-emitter terminal: the gate-emitter path is separate from the load current carrying path for the power-emitter (P2). On the other hand, both the power-emitter and the gate-emitter share the same load current carrying path in the Infineon FS200, and a kelvin connection for V_{CE} measurement is not possible.

6 Conclusion

This paper uses an IR camera to experimentally evaluate TSEP methods for IGBT junction temperature measurement based on the collector-emitter voltage. Experimental validation is performed on a variety of IGBT modules with differing geometry and manufacturer, and includes verification on paralleled chips. The normal- V_{CE} at high current is shown to give vastly inaccurate results. A modified- V_{CE} method is thus proposed, which is based on the difference in V_{CE} at two different gate voltages (15V and 13V). This method is designed to remove the resistive contribution of interconnection materials at high current levels. The modified- V_{CE} method, referred to as ΔV_{CE_AVGE} , shows significant improvement in accuracy, with maximum errors typically within -10°C of the mean junction temperature as measured with an IR camera. Some modules appear to be more suited to temperature measurement using V_{CE} -based techniques than others.

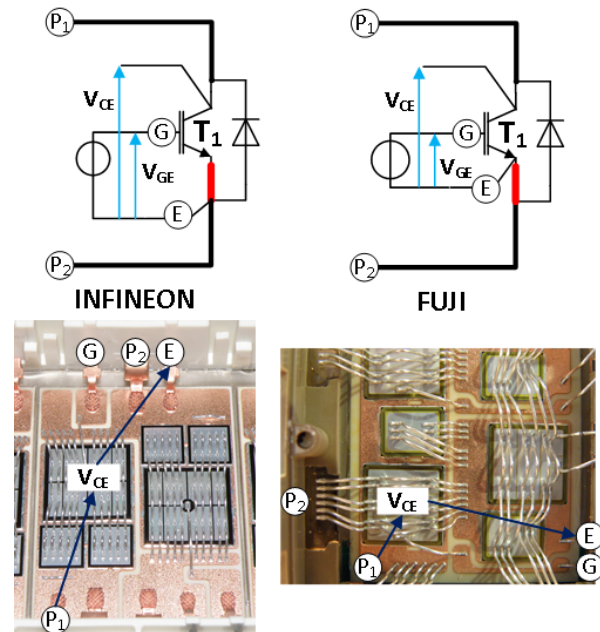


Figure 12 Power module layouts of F200 and 6MBI100, and schematic for electrical measurements

7 Acknowledgement

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