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A Fully-Digital BIST Wrapper Based on Ternary Test Stimuli for the Dynamic Test of a 40nm CMOS 18-bit Stereo Audio $\Sigma\Delta$ ADC

Manuel J. Barragan, *Member, IEEE*, Rshdee Alhakim, *Member, IEEE*,
Haralampos-G. Stratigopoulos, *Member, IEEE*, Matthieu Dubois, Salvador Mir, *Member, IEEE*, Hervé Le Gall,
Neha Bhargava, and Ankur Bal

Abstract—This paper proposes a fully-digital BIST architecture for the dynamic test of $\Sigma\Delta$ ADCs. The proposed BIST relies on generating a ternary stream that encodes a high-linearity analog sinusoidal and injecting it directly at the input of the $\Sigma\Delta$ modulator. Compared to the well-known bitstream, the use of three logic levels in the ternary stream reduces the quantization noise and, thereby, results in a test with a higher dynamic range that covers the full scale of the ADC. The output response is analyzed on-chip using a simplified version of the sine-wave fitting algorithm to compute the SNDR. A standard SPI bus provides digital external access to the embedded test instruments. The proposed BIST wrapper has been integrated into a 40 nm CMOS 18-bit stereo audio $\Sigma\Delta$ ADC IP core provided by ST Microelectronics. It incurs an overall area overhead of 7.1% and the total test time is 28ms per channel. Experimental results on fabricated chips demonstrate an excellent correlation between the BIST and the standard functional specification test.

I. INTRODUCTION

CURRENT market trends in the IC industry towards the design of highly integrated mixed-signal Systems-on-Chip (SoCs) and heterogeneous Systems-in-Package (SiPs) are supported by the reuse of parametrized Intellectual Property cores (IPs) –either in-house developed or provided by different IP vendors– that implement different analog, mixed-signal, and digital functions within the system. Testing the digital IP cores in these systems is a relatively straightforward task. A wide variety of broadly proven Design-for-Test (DfT) strategies for accessing these cores and evaluating their correct functionality are routinely embedded in every digital IP. These DfT strategies are built on the concepts of standardized scan chain buses and structural tests. On the other hand, testing mixed-signal IP cores in these systems still relies on functional specification testing. Functional specification testing uses specialized automated test equipment (ATE) for applying appropriate test stimuli, retrieving the output responses, and

processing the test results. However, in a complex SoC/SiP –where the external access to the internal IPs is difficult, or directly impossible– these operations may turn challenging to perform at a reasonable cost [1]. Indeed, it has been estimated that the cost of testing mixed-signal IP cores has already become the dominant contribution to the overall manufacturing cost [2].

A promising solution to the aforementioned issues is the development of mixed-signal Built-In Self-Test (BIST) techniques. BIST techniques aim at moving some of the ATE functionality into each IP, in such a way that generation and manipulation of test signals become internal to the IP, thus eliminating the need of external analog test access and relaxing the ATE requirements. In an ideal scenario, each analog and mixed-signal IP core should have its own dedicated embedded test instruments adapted to its custom-made test programs and interfaced via a system-level bus to a low-cost digital ATE for controlling test execution and retrieving test results. This way, BIST may significantly reduce the overall production cost of these systems by taking into consideration the test approach right at the IP design stage. Moreover, the benefits of deploying mixed-signal BIST solutions are not limited to production test. BIST opens the door to further developments for performance and reliability enhancements along the complete life-cycle of an integrated circuit, including calibration, self-healing, on-line test, adaptive operation, fault diagnosis and failure analysis, etc.

In this paper, we present the design and experimental validation of a fully-digital BIST wrapper for the dynamic test of a 40nm CMOS 18-bit stereo audio $\Sigma\Delta$ ADC IP core designed by ST Microelectronics. Testing the dynamic performance of an ADC in terms of Signal-to-Noise-and-Distortion ratio (SNDR) requires exciting the ADC Under Test (ADCUT) with a high-resolution sinusoidal stimulus –at least two effective bits higher than the resolution of the ADCUT. Moreover, the demand for high-quality audio devices is driving the improvement in the performance of $\Sigma\Delta$ ADCs toward higher resolutions and dynamic ranges. Therefore, generating the required test stimulus efficiently on-chip towards a fully integrated BIST implementation is a very challenging task. The proposed BIST wrapper achieves this objective by relying on the generation of a digital ternary test stimulus that encodes a high-resolution sine-wave. The ternary test stimulus is directly injected into the input of the modulator of the $\Sigma\Delta$ ADC

M. J. Barragan, R. Alhakim, and S. Mir are with CNRS, Université Grenoble–Alpes, TIMA, F-38000, Grenoble, France (e-mail: manuel.barragan@imag.fr).

H. Stratigopoulos is with Sorbonne Universités, UPMC Univ. Paris 06, CNRS, LIP6, 4 place Jussieu, 75005, Paris, France.

M. Dubois is with Pyxalis, CentrOAlp, 170 rue de chatagnon, 38346 Moirans, France.

H. Le Gall is with ST Microelectronics, 12 Rue Jules Horowitz, 38000, Grenoble, France.

N. Bhargava and A. Bal are with ST Microelectronics, Plot No. 1, Knowledge Park III, 201308, Greater Noida, India.

requiring minimal design modifications. The BIST wrapper also includes a test response analyzer for computing the SNDR on-chip and providing a 1-bit go/no-go test response, as well as a control unit for managing the test execution. The proposed BIST wrapper incurs an overall area overhead of 7.1% and the total test time is 28 ms per channel. We discuss in detail the co-design of the BIST wrapper and the $\Sigma\Delta$ ADC and we present experimental results based on fabricated chips.

The rest of the paper is organized as follows. In Section II, we give an overview of the state-of-the-art for $\Sigma\Delta$ ADC BIST. In Section III, we present the architecture of the proposed BIST wrapper. In Section IV, we present the experimental validation of the proposed BIST approach. Finally, Section V concludes the paper summarizing the main contributions.

II. PREVIOUS WORK

In recent years there has been an intense research effort towards developing BIST strategies for $\Sigma\Delta$ ADCs. In [3], an Oscillation-Based BIST (OBIST) strategy for $\Sigma\Delta$ modulators is proposed that consists of reconfiguring the modulator under test into an oscillator. Both the frequency and amplitude of the oscillation are monitored and processed to distinguish faulty from fault-free circuits. This test strategy provides a structural verification of the modulator under test targeting defects. However, the sensitivity to process variations and the need of extensive circuit reconfiguration can deteriorate the quality of this approach.

In [4], [5], it is proposed to estimate the magnitude of the leakage in the integrators of the modulator which is directly related to the in-band quantization noise power at the modulator's output, thus allowing to estimate the dynamic performance of the modulator. However, as demonstrated in [6], additional tests targeting different modulator parameters (i.e. settling time, amplifier non-linearity, etc.) are required for a complete validation of the modulator's performance.

Another idea that has been thoroughly explored in the literature is the use of digital $\Sigma\Delta$ bitstreams. The starting point is to use an ideal $\Sigma\Delta$ modulator in software to convert a high-resolution analog sine-wave to a digital bitstream. The bitstream is truncated to get an optimized sequence that is periodically reproduced using a circular shift-register [7]. Bitstreams can also be generated using on-chip digital oscillators, but their design is not straightforward [8]. The bitstream can be converted to a high-resolution analog sine-wave by passing it through a 1-bit digital-to-analog converter (DAC) followed by a low-pass filter to remove quantization noise. Although this solution is applicable for a built-off test where the 1-bit DAC and the low-pass filter are placed on the load board, it is not applicable for BIST since for high-resolution applications the low-pass filter may be far more complex than the modulator under test [9], [10].

Interestingly, in the case of Switched-Capacitor (SC) $\Sigma\Delta$ ADCs, the bitstream can be fed directly into the modulator by adding simple circuitry at its input [11]–[13]. A 1-bit DAC – typically a replica of the feedback DAC in the modulator input stage – is used to convert the bitstream to the analog reference voltages of the modulator. However, the direct injection of

the bitstream to the input of the ADC will overload the modulator, unless the reference voltages of the 1-bit DAC are adequately attenuated [12]. This attenuation also scales down the amplitude of the encoded sine-wave, which, in effect, will be far below the Full Scale (FS) of the ADC. This is a key limitation of this test technique, since for an accurate dynamic test the amplitude of the test stimulus has to be as close as possible to the FS such that the harmonic distortion introduced by the ADC is amply manifested [14].

A solution to this problem has been proposed in [15], [16], where the input switched-capacitor network of the $\Sigma\Delta$ modulator is reconfigured in test mode such that it accepts multiple bitstreams delayed from each other. This technique has been proved to attenuate the noise power of the test stimulus, allowing this way to test the modulator at amplitudes closer to the FS. However, this comes at the cost of significantly increasing the design complexity of the input stage of the modulator.

An elegant approach to overcome this issue was proposed in [17]. A sinusoidal test stimulus is encoded in a ternary stream that is composed of three logic levels $\{-1, 0, +1\}$ and injected directly at the input of the modulator of the $\Sigma\Delta$ ADC under test. The ternary stimulus is generated in the digital domain by adding a $\Sigma\Delta$ encoded binary bitstream with a delayed version of itself. From a spectral point of view, the Discrete Fourier Transform (DFT) of a length- N bitstream $\{b_0, \dots, b_{N-1}\}$ is given by

$$B(k) = \sum_{n=0}^{N-1} b_n \cdot e^{-j\frac{2\pi}{N}nk}, \quad k = 0, \dots, N-1. \quad (1)$$

The N periodic extension leads to a spectrum made by N lines located at $f_k = kf_s/N$, where f_s is the sampling frequency. The DFT of the circular-shifted bitstream delayed by one sample $\{b_1, \dots, b_{N-1}, b_0\}$ is obtained by applying the time shift theorem to (1)

$$B_\delta(k) = B(k) \cdot e^{-j\frac{2\pi}{N}k}, \quad k = 0, \dots, N-1. \quad (2)$$

The DFT of the ternary stream is then obtained by averaging the DFT of the original bitstream and the DFT of the circular-shifted version of it and by using the linearity property of the DFT

$$T(k) = \frac{B(k)}{2} \left(1 + e^{-j\frac{2\pi}{N}k}\right), \quad k = 0, \dots, N-1. \quad (3)$$

The Power Spectral Density (PSD) of the bitstream and the ternary stream are given by

$$\begin{aligned} S_B(k) &= \|B(k)\|^2 \\ S_T(k) &= S_B(k) \cdot \cos^2\left(\frac{\pi k}{N}\right) \\ & \quad k = 0, \dots, N-1, \end{aligned} \quad (4)$$

respectively. Therefore the spectra of the ternary stream presents a lowpass filter behavior that attenuates the shaped quantization noise at high frequencies. In other words, the ternary stream overloads less the modulator compared to the bitstream and, thereby, offers the possibility of testing the $\Sigma\Delta$ ADC closer to full scale. In fact, the proposed ternary

TABLE I
SUMMARY OF PERFORMANCE AND DESIGN PARAMETERS OF THE ADCUT

Input range	1.4 V
Input bandwidth	24 kHz
Sampling frequency (MASH input)	6.144 MHz
Sampling frequency (ADC output)	48 kHz
Nominal resolution	18 bits
SNDR (typical)	94 dB
Analog power supply	3.3 V
Digital power supply	1.1 V
Power consumption	41.8 mW

encoder is equivalent to a first-order lowpass FIR filtering of the binary stream to attenuate the shaped quantization noise. In principle, higher-order FIR filtering could be used to reduce the quantization noise of the test stimulus even further, but doing so would also require a complex high-linearity multi-bit DAC to inject the digitally filtered test stimulus at the input of the modulator.

On the other hand, the injection of the ternary stimulus at the input of the modulator does not require a significant reconfiguration of the input stage. In particular, the ternary stream is converted to a three-level analog signal and injected directly at the input stage of the modulator. In fact, the implementation is, in essence, equivalent to the case of applying a binary bitstream. The proposed approach presents a minimal overhead and allows measuring SNDR for amplitudes close to FS.

The theoretical principles behind the concepts of ternary test stimulus generation and injection were described in [17] and were validated using behavioral model simulations. The feasibility and suitability of the ternary test stimulus for high-volume production test was further validated in [18], [19] by means of parametric test metrics estimation techniques based also on behavioral model simulations.

In this paper, we present for the first time a hardware implementation of the BIST approach based on ternary test stimuli.

III. SELF-TESTABLE $\Sigma\Delta$ ADC ARCHITECTURE

A. System overview

Fig. 1 shows a conceptual block diagram of the complete $\Sigma\Delta$ ADC IP core incorporating the BIST wrapper for measuring on-chip the SNDR. In normal operation mode, the analog input signals for Left and Right channels are first filtered by an active-RC second-order low-pass anti-aliasing filter that also provides a single-ended-to-fully-differential signal conversion. A 2:1 MASH SC modulator converts these differential signals to a digital bitstream and a fourth-order digital decimation filter eliminates the shaped high-frequency noise to provide the 18-bit digital output. The IP features a single output port with 18 bits in parallel, where the Left and Right channel outputs are time-interleaved according to the rising and falling edges of a control signal (labelled FSYNC_IN in Fig. 1). Relevant performance and design parameters of the ADC IP are summarized in Table I.

In BIST mode, an optimized digital bitstream stored in a circular shift-register is periodically repeated and combined

with a delayed version of itself to generate a digital ternary test stimulus encoding a high-resolution sinusoidal test stimulus within the bandwidth and input dynamic range of the ADCUT. The ternary test stimulus is injected directly at the input of the 2:1 MASH modulator of one of the ADC channels, which has been previously selected and disconnected from the input signal path. The resulting output bitstream is routed to the Left channel of the decimation filter to produce an 18-bit test response signal, labelled S_{out} in Fig. 1. At the same time, the original optimized digital bitstream is fed to a fully-digital implementation of the 2:1 MASH modulator. The resulting output bitstream is fed to the Right channel of the decimation filter to produce a high-precision 21-bit digital sine-wave, labelled S_{ref} in Fig. 1, that serves as the reference signal. The digital 2:1 MASH assures the synchronization between Right and Left channel output signals, since both the modulator in the channel under test and the digital 2:1 MASH introduce a z^{-3} signal delay. Then, the test output response from the Left channel and the reference signal from the Right channel are extracted from the time-interleaved output of the ADCUT using the synchronization signal FSYNC_IN and fed to the test response analyzer block. This block computes the SNDR of the channel under test from the response and reference signals using a simplified version of the sine-wave fitting algorithm. The obtained SNDR is finally compared to a pre-loaded specification limit and a go/no-go digital signal is generated. The complete test is managed by a BIST control block which also includes a standard Serial-Peripheral Interface (SPI) digital bus for external programming and communication.

The following subsections detail the design and functionality of the main building blocks of the proposed BIST wrapper.

B. Ternary stimulus generator

Fig. 2 shows a schematic view of the on-chip digital ternary test stimulus generator and its interface signals with the ADCUT, the BIST control, and the digital 2:1 MASH modulator. The core of the ternary test stimulus generator circuitry is a circular shift-register composed of $n = 1126$ flip-flops. During test mode, this circular shift-register stores and reproduces a bitstream that encodes one period of a high-precision sinusoidal test stimulus. The circular shift-register is clocked at the modulator sampling frequency of $f_s = 6.144$ MHz and produces a bitstream with a fundamental tone at $f_{test} = f_s/n = 5.46$ kHz. This frequency is fixed by design and it has been chosen such that the main tone of the test stimulus and the first three harmonic components (i.e. up to the fourth harmonic component) lie within the audio bandwidth of the ADCUT. The bitstream is obtained by simulating in software an ideal $\Sigma\Delta$ modulator excited by a pure sine-wave.

The ternary test stimulus is obtained by adding the bitstream stored in the circular shift-register with a version of the same bitstream delayed by one clock cycle. As demonstrated in [17] and discussed in Section II, this operation has a lowpass filtering effect on the shaped quantization noise at high frequencies and achieves a significant reduction of the total quantization noise power with respect to the original

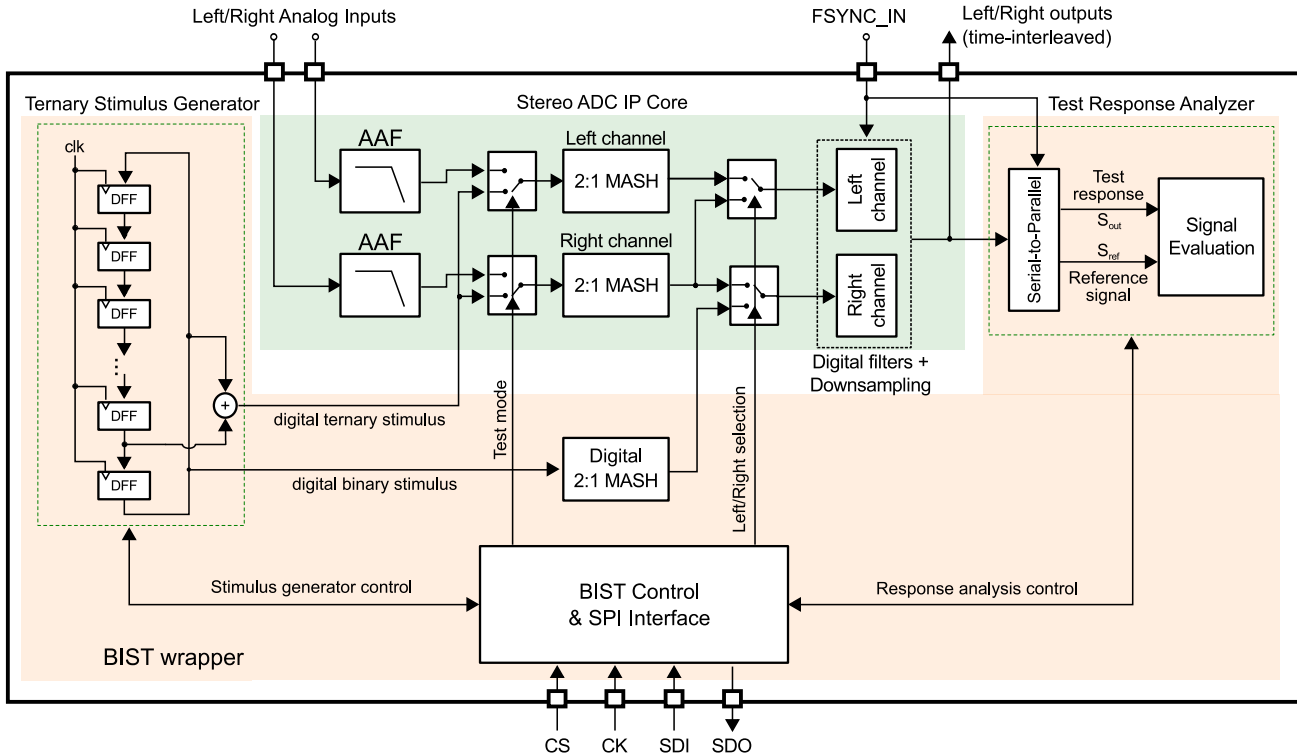


Fig. 1. Architecture of the self-testable $\Sigma\Delta$ ADC.

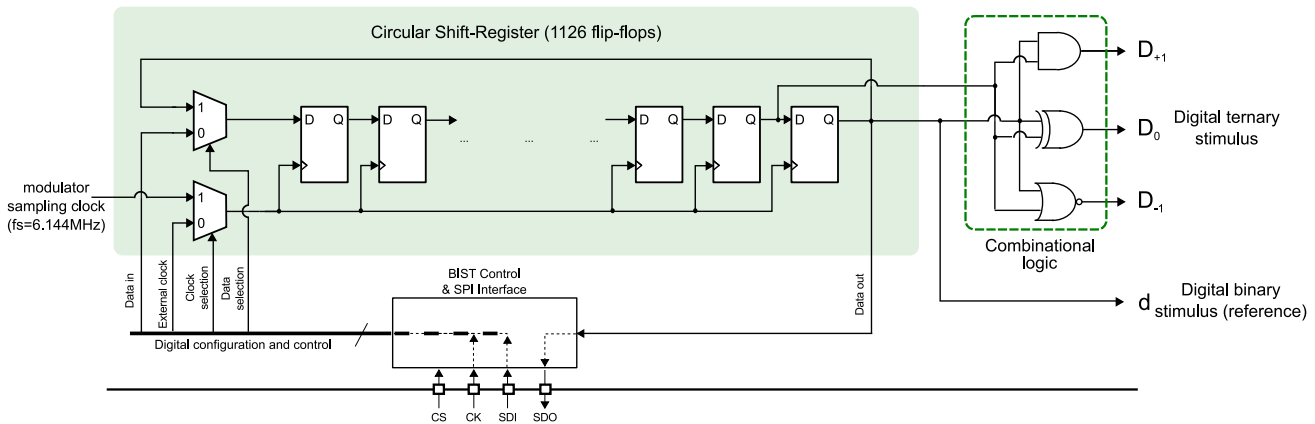


Fig. 2. Micro-architecture of the ternary test stimulus generator block.

bitstream. The combination of the two bitstreams only requires the addition of three logic gates to generate the three digital signals D_{-1} , D_0 , and D_{+1} encoding the three levels of the ternary test stimulus.

It is widely accepted in the industry that the test stimulus has to be at least 2 effective bits more linear than the specification of the ADCUT for accurate and reliable results. Otherwise, the non-linearity of the ADCUT is masked by the non-linearity of the test stimulus [20]. For this purpose, an optimization is performed with the aim to select the bitstream that maximizes the SNDR of the ternary test stimulus and renders the ternary test stimulus appropriate for an accurate dynamic testing of the ADCUT. The interested reader is referred to [17] for a detailed description of the optimization strategy.

Fig. 3 plots together the nominal SNDR of the 2:1 MASH

modulator in the ADCUT as a function of its input amplitude and the SNDR of the optimized ternary test stimulus as a function of the amplitude of the encoded sine-wave, both measured at $f_{test} = 5.46$ kHz. The amplitude is varied across the complete FS of the modulator. As it can be seen, the optimization loop manages to find ternary test stimuli that have a SNDR at least 2.5 equivalent bits higher than the SNDR of the modulator, thus respecting the requirement that the test stimulus must have a resolution at least two effective bits higher than the resolution of the ADCUT.

It is important to note that the proposed BIST wrapper has been designed for production testing, where a single fixed-frequency in-band test stimulus is applied according to the standard [20]. Therefore, the proposed BIST is not meant for

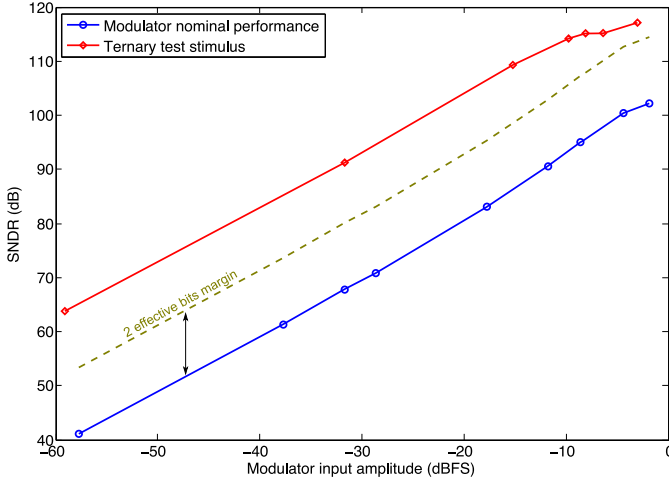


Fig. 3. SNDR of the modulator and the optimized ternary test stimulus as a function of the input amplitude.

full electrical characterization across the complete bandwidth of the ADCUT. Furthermore, pushing the frequency of the test stimulus towards the bandwidth limit is not a straightforward task. From a hardware point of view, the frequency of the stimulus can be easily increased by reducing the number of flip-flops, n , in the circular shift-register or, equivalently, by encoding multiple signal periods into the register. The optimization algorithm can also be easily redesigned, in order to get appropriate test stimuli with a high enough SNDR at high frequencies. However, obtaining high-linearity stimuli close to the bandwidth limit may require employing a high-order $\Sigma\Delta$ modulation scheme within the optimization loop. The challenge in this scenario is that the decimation filter in the ADCUT itself may need to be modified so as to cope with the shaped quantization noise.

The ternary stimulus generator is managed by the BIST control block and is interfaced to the external pins (or to other IPs in a SoC/SiP) through the SPI bus. The optimized bitstream is loaded into the circular shift-register through the Serial Data Input (SDI) port. Serial data are synchronized to an external clock fed to the BIST control through the CK port. The content of the circular shift-register can also be read out for additional verification and diagnosis. Output data are sent out through the Serial Data Output (SDO) port and are synchronized to the external clock. During test execution, the BIST control unit enables the test mode, closes the feedback loop of the circular shift-register, and clocks the circular shift-register at the sampling clock frequency of the modulator (i. e. clock phase ϕ_1 in Fig. 4).

C. Ternary test stimulus injection

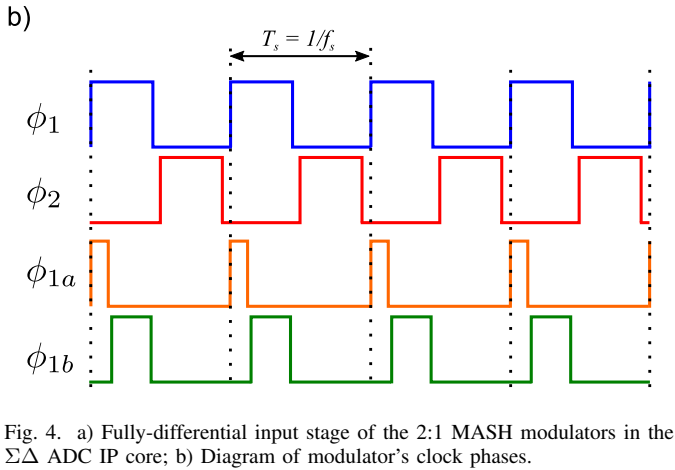
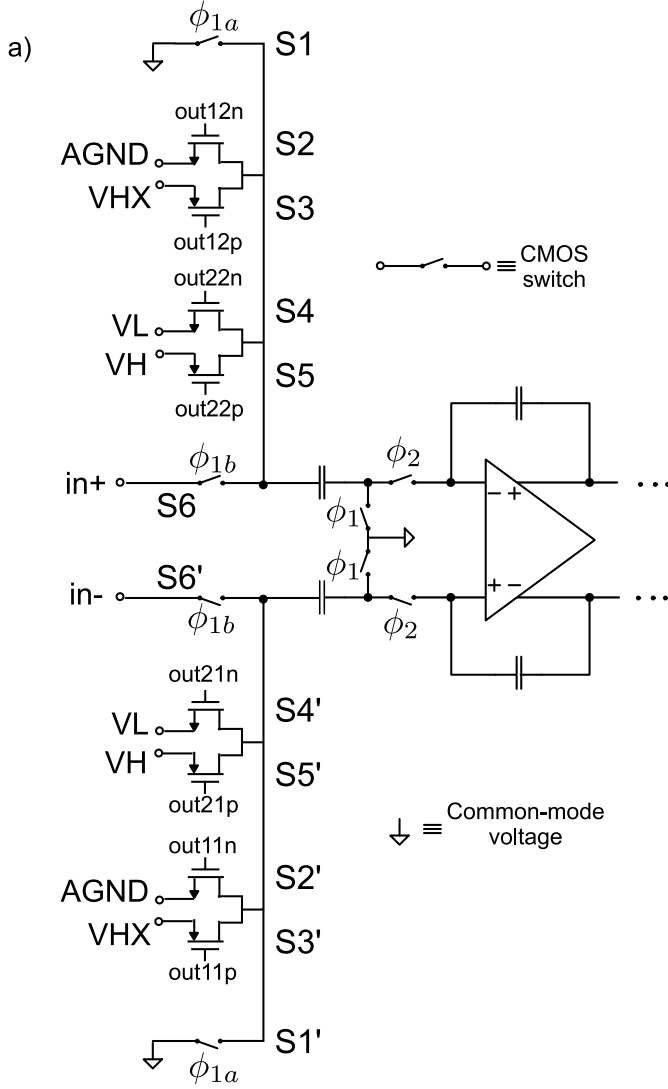
The ternary test stimulus is directly injected into the input of the modulator using a three-level DAC controlled by signals D_{-1} , D_0 , and D_{+1} . Fig. 4 shows the original schematic of the input switching stage of the 2:1 MASH modulator and the diagram of its clock phases. The 2:1 MASH modulators in the ADC IP core work with two non-overlapped clock phases, denoted by ϕ_1 and ϕ_2 in Fig. 4. The input sampling

operation is divided into two sub-phases within clock phase ϕ_1 . During clock sub-phase ϕ_{1a} , the input capacitors are reset by shorting their nodes to the common-mode voltage. During clock sub-phase ϕ_{1b} , the input capacitors are charged to the input voltages. The digital output bitstreams at the output of the modulator, denoted by $outXYZ$, are fed back to the input of the modulator in clock phase ϕ_2 , which is also divided into two steps. In a first step, the feedback signals $out1YZ$ are activated, connecting the input node to reference voltages $AGND$ or VHX . Note that index Y makes reference to the signal path—positive or negative—to which the switch is connected, while index Z makes reference to the type of transistor. Reference voltages $AGND$ and VHX offer a fast signal settling at the cost of a low precision. They are used to pre-load the input capacitor to a value close to the $\Sigma\Delta$ ADC references. In a second step, feedback signals $out2YZ$ are activated, connecting the input node to the ADC reference voltages VL or VH . These reference voltages offer a high precision reference value, but signal settling is slower. The division of the modulator feedback operation in these two steps allows relaxing the design of the integrated bandgap reference generator.

Fig. 5 shows the modification of the input switching stage for the purpose of injecting the ternary test stimulus. During test mode, control signal T is set to “1” by the BIST control block, turning off the input sampling switches, denoted by $S6$ and $S6'$ in Fig. 5, and, thereby, isolating the modulator under test from the input signal path. At the same time, extra switches STX are connected to the input node of the sampling capacitors. This set of switches implements a simple and robust three-level differential DAC that reconstructs the analog sine-wave encoded in the ternary test stimulus $\{D_{-1}, D_0, D_{+1}\}$ and injects it directly into the input sampling capacitors of the modulator under test. As opposed to [12], it is not required to scale down the reference voltages VH and VL , thus no modifications of the bandgap reference generator and no extra external analog references are needed. States “+1” and “-1” in the ternary test stimulus are directly converted to the differential analog levels $VH - VL$ and $VL - VH$, respectively, while the “0” state is implemented by generating a null differential voltage at the input nodes of the sampling capacitors. This is achieved by connecting the input capacitors to the common-mode voltage V_{cm} through switches $ST1$ and $ST1'$ to discharge them. Alternatively, this null differential voltage could have been produced by activating switches $S1$ and $S1'$ during clock phase ϕ_{1b} , but this would have required an extensive modification of the internal clock phase generator to avoid overlapping between clock phases ϕ_{1a} and ϕ_{1b} during normal operation. We opted for adding independent switches $ST1$ and $ST1'$ since it is a simpler option.

The overall overhead for injecting the ternary test stimulus is only the six switches $ST1$, $ST1'$, $ST2$, $ST2'$, $ST3$, and $ST3'$ which is equivalent to only four CMOS switches. From a design point of view, switches $ST1$ and $ST1'$ are an exact replica of switches $S1$ and $S1'$, whereas switches $ST2$, $ST3$, $ST2'$, and $ST3'$ are an exact replica of switches $S4$, $S5$, $S4'$, and $S5'$, respectively.

An aspect that should be carefully considered in the design of the three-level DAC is the impact of the DAC non-linearity



on the spectral purity of the ternary test stimulus. An ideal three-level DAC should have the linear input-output characteristic depicted in Fig. 6(a). However, second-order non-idealities, such as mismatch and unbalanced charge injection between positive and negative signal paths, may lead to DAC non-linearity. In order to analyze the impact of these non-idealities on the proposed three-level DAC, we consider a

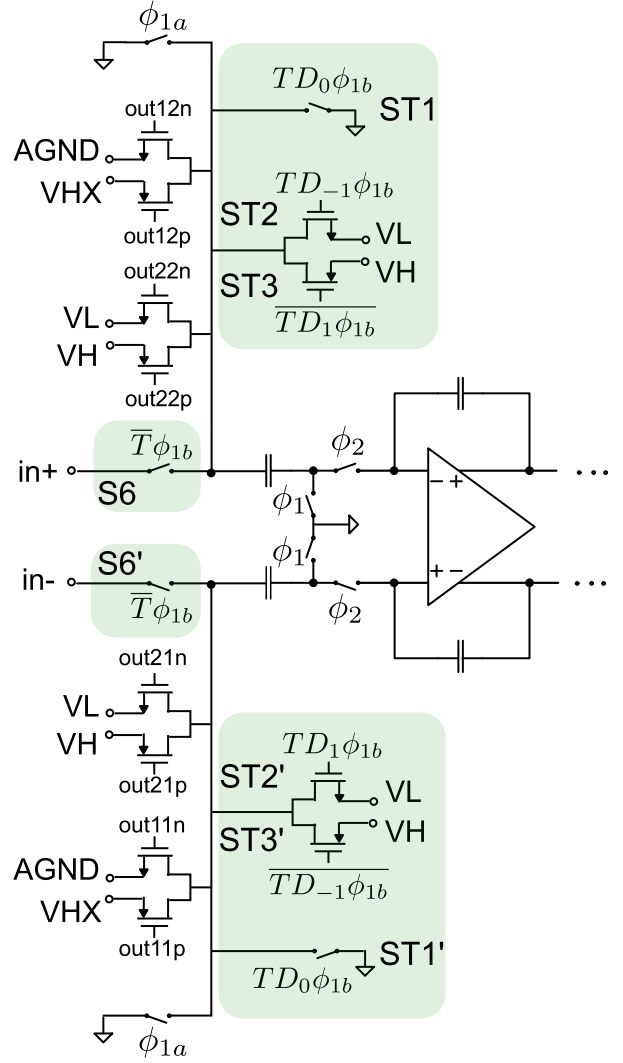


Fig. 5. Modification of the fully-differential input stage of the 2:1 MASH for the purpose of injecting the ternary test stimulus. The modifications have been highlighted.

simple model, as shown in Fig. 6(b). The effect of the non-idealities on the DAC levels has been modeled as an equivalent deviation on the middle-point output voltage, labelled as V_{off} in Fig. 6(b). In general, V_{off} may also depend on the input digital sequence of the DAC. However, the fully-differential DAC implementation, together with the reset of the sampling capacitor during phase ϕ_{1a} before injecting each sample of the test stimulus, result in V_{off} that is approximately constant. Using this simple model for the proposed three-level DAC design, Fig. 7 shows the SNDR at the output of the DAC when the magnitude of V_{off} is swept from 1 nV to 1 mV. In this analysis, the DAC is excited by a digital ternary test stimulus encoding a sinusoid with an amplitude $A = -3$ dBFS. The SNDR of this test stimulus is SNDR = 117 dB and is indicated in Fig. 7 for visual reference. As it can be observed, the linearity in terms of SNDR of the signal at the DAC output drops quickly for $V_{off} > 10 \mu\text{V}$.

To this end, we performed a transistor-level Monte Carlo simulation of the actual three-level DAC that is employed in

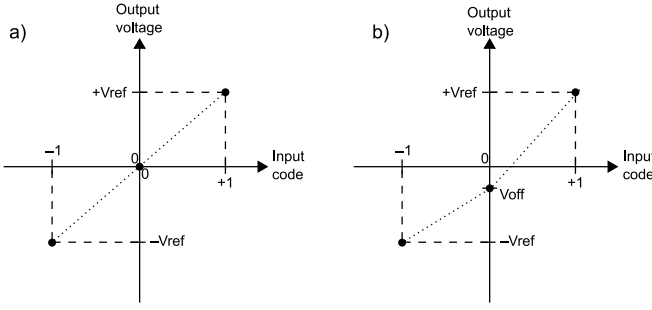


Fig. 6. a) Input-output characteristic of an ideal three-level DAC; b) Non-linear model for a three-level DAC. Non-linear effects are combined into an equivalent offset in the middle-point level of the DAC.

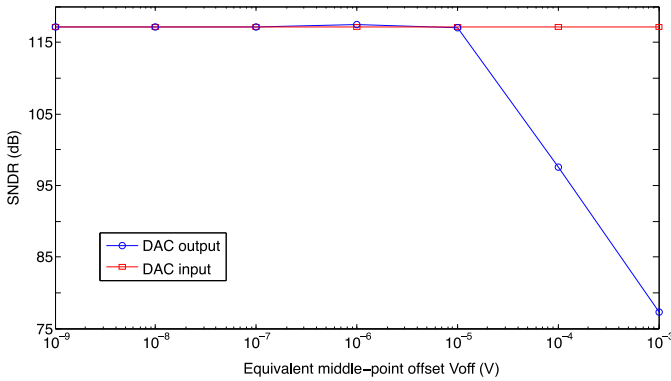


Fig. 7. SNDR at the output of the three-level DAC as a function of the equivalent middle-point offset. The DAC is excited by a digital ternary stimulus encoding a sinusoidal signal with $A = -3$ dBFS and SNDR = 117 dB

the BIST wrapper considering both global process variations and mismatch. The Monte Carlo analysis shows a worst equivalent deviation of the middle-point voltage of the DAC $V_{off} < 10$ nV. Referring back to the results in Fig. 7, we conclude that the non-linearity of the proposed DAC has no effect on the BIST technique.

D. Test response analyzer

The test response evaluation is performed by a version of the sine-wave fitting algorithm [20], [21]. Many efficient implementations of the sine-wave fitting algorithm have been proposed in the literature [12], [22], [23]. In this work, we implement a simplified version of the sine-wave fitting algorithm that was first introduced in [12]. The classical sine-wave fitting algorithm aims at fitting in a least-square sense a pure sinusoidal reference signal to the output response of the ADCUT. The goal is to determine the DC level, amplitude, frequency, and phase of the fundamental tone in the test response signal. Noise and distortion components can then be easily computed as the residues of the fitted curve. The interested reader is referred to [20], [21] for a detailed analysis of the sine-wave fitting technique. The proposed simplification of the sine-wave fitting algorithm is based on the fact that the test response and reference signals have the same frequency and they are completely synchronized, which saves us from having to compute the phase and frequency of the test response

signal. Next, we describe the algorithm for computing the SNDR and making a direct go/no-go test decision on-chip. The algorithm is conceptually depicted in Fig. 8.

The algorithm first computes the DC component of the test response signal as

$$DC = \frac{1}{N} \sum_{i=1}^N S_{out}(i), \quad (5)$$

where $S_{out}(i)$ are the samples of the test response signal at the output channel under test and N is the total number of samples considered in the evaluation. In our implementation, the number of samples is fixed to $N = 563$ which corresponds to 64 signal periods coherently sampled. Coherent sampling is not required by the classical sine-wave fitting algorithm, but it further simplifies the computations and, thereby, it reduces significantly the resources required for the hardware implementation. It should be stressed that coherent sampling is easily achieved by construction, since, as explained in Section III-B, the period of the test stimulus is an integer multiple of the modulator sampling clock period.

In the next step, the algorithm computes the point-to-point correlation of test response and reference signals as

$$Correl = \sum_{i=1}^N S_{out}(i) S_{ref}(i), \quad (6)$$

where $S_{ref}(i)$ are the samples of the reference signal. The amplitude of the test response signal is related to the computed correlation as

$$A = \frac{2}{NA_{ref}} Correl, \quad (7)$$

where A_{ref} is the amplitude of the reference signal encoded in the ternary test stimulus, which is known *a priori*.

Once the amplitude has been computed, the algorithm adjusts the reference signal to the amplitude A and DC values as

$$S_{ref,adj}(i) = \frac{A}{A_{ref}} S_{ref}(i) + DC. \quad (8)$$

Finally, the algorithm computes the noise and distortion power in the test response signal, denoted by P_{error} , as

$$P_{error} = \frac{1}{N} \sum_{i=1}^N (S_{out}(i) - S_{ref,adj}(i))^2. \quad (9)$$

The SNDR of the test response signal can be computed as

$$SNDR = 10 \log \frac{A^2/2}{P_{error}}. \quad (10)$$

However, to avoid an excessive overhead, the test response analyzer does not compute directly the SNDR value. Instead, it performs a comparison with a preloaded threshold to provide a go/no-go test decision. From (10)

$$\text{go/no-go} = \begin{cases} 1, & \text{if } \frac{A^2}{2} \geq P_{error} 10^{SNDR_{spec}/10} \\ 0, & \text{if } \frac{A^2}{2} < P_{error} 10^{SNDR_{spec}/10} \end{cases} \quad (11)$$

where $SNDR_{spec}$ is the SNDR specification of the ADCUT. The threshold value $Threshold = 10^{SNDR_{spec}/10}$ is a known

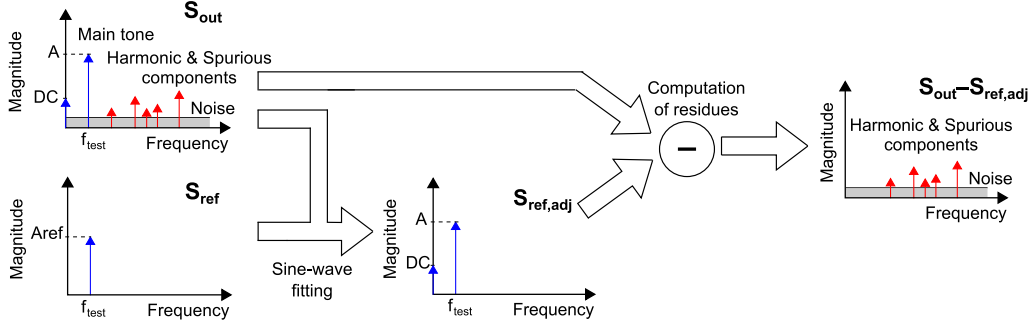


Fig. 8. Graphical representation of the proposed algorithm for test response analysis.

constant that is loaded into the test response analyzer prior to the evaluation.

The proposed test response analyzer has been implemented with an embedded Arithmetic Logic Unit (ALU) and a Finite-State Machine (FSM) controller, schematically depicted in Fig. 9. The ALU has three main blocks—addition, multiplication, and division— together with two blocks for complement operations and one block for comparison operations. The blocks for the complement operations are required to enable subtractions, while the block for comparison is required to compare P_{error} with the preloaded threshold value. The proposed implementation uses Booth’s multiplication algorithm to build the multiplier, while the division is actually performed by multiplying by the inverse of the denominator. The FSM controller is programmed to evaluate equations (5)-(11) sequentially, using only one adder, one multiplier, and one divider. In order to further reduce the area overhead of the test response analyzer, S_{out} and S_{ref} samples are not stored into a memory, but sequentially read from the outputs of the ADCUT and fed to the evaluation algorithm. As a consequence, the evaluation algorithm is executed in two sequential steps: in the first step the algorithm evaluate equations (5)-(7) over N ADCUT output samples, while in the second step N additional samples are read to evaluate equations (8)-(11).

The functionality of the test response analyzer is also controlled by the BIST control block through the SPI bus. The reference values A_{ref} and $Threshold$ are externally loaded through the SDI port, synchronized to the external clock fed by the CK port. The BIST control block manages the execution of the evaluation algorithm and outputs the go/no-go test decision through the SDO port at the end of the evaluation.

E. BIST control and SPI interface

The BIST control block manages the test program by supervising the execution of the test and, as it has been described previously, it also interfaces the BIST wrapper with the external ATE through a standard SPI bus. The BIST control block consists of four main units, as shown in Fig. 10, namely a SPI Slave port Unit, a Fetch and Execute Unit, a Configuration Unit, and a Reset Unit.

The SPI Slave port Unit has been designed to provide a robust and simple serial interface between the BIST wrapper and the ATE. This standard serial connection allows the ATE to configure the test parameters (i.e. load input stimulus,

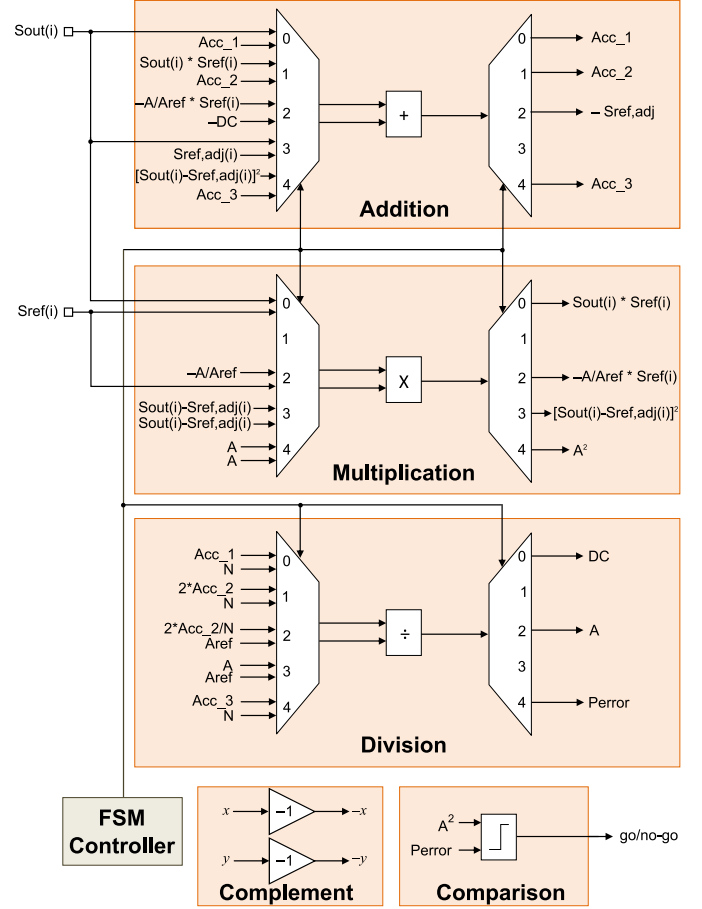


Fig. 9. Micro-architecture of the test response analyzer.

write configuration registers, etc.) and read out the test results through the SPI standard ports CS, CK, SDO, and SDI. The SPI Slave port Unit is connected to the Fetch and Execute Unit using a parallel interface which is clocked at the master system clock of the IP, which is denoted by SYS_CK in Fig. 10. The SPI Slave port Unit works on two asynchronous clock domains, namely the external clock CK and the master system clock SYS_CK. It has been designed to guarantee a correct data transfer over these two asynchronous clock domains without any data loss or undesired meta-stability behavior.

The Reset Unit initializes all registers in the BIST wrapper. This global reset instruction can be activated directly via

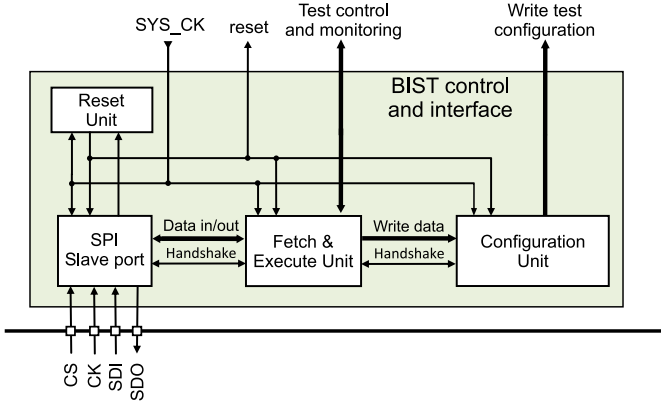


Fig. 10. Micro-architecture of the BIST control and SPI interface block.

the SPI Slave port Unit sending the appropriate command sequence.

The Fetch and Execute Unit has been designed to receive 8-bit command messages from the SPI Slave port Unit, decode them, and execute the corresponding action. It transmits all external configuration data coming from the SPI Slave port Unit to the Configuration Unit. Then, the Configuration Unit loads these data to the appropriate register in the BIST wrapper. The Fetch and Execute Unit also receives the test result data and sends them to the SPI Slave port Unit to be read out through the SPI interface. In addition, it acts as the global test processor of the BIST wrapper and controls the execution of the self-test procedure.

A complete test sequence starts by loading a test configuration through the SPI bus (e.g. bitstream in the circular shift-register and reference values A_{ref} and $Threshold$) and defining the channel under test (i. e. Left or Right). Then, upon receiving the “execute test” command, the BIST control block interrupts the normal operation of the ADCUT by enabling the test mode and the ternary test stimulus is injected into the input of the selected channel. The first 20 periods of the test response are discarded to avoid capturing transient effects, then the following 128 periods are processed by the test response analyzer which compares the SNDR of the test response signal to the preloaded specification value, as detailed previously. Once the self-test has been completed, the BIST control restores normal operation and stores the test results, which can be thereafter read out via the SPI bus upon receiving the appropriate commands. The whole self-test procedure takes 28 ms per ADC channel.

IV. EXPERIMENTAL RESULTS

We have redesigned a 40nm CMOS 18-bit stereo audio $\Sigma\Delta$ ADC IP provided by ST Microelectronics to include the complete BIST wrapper. In total, 56 prototype chips were fabricated. Fig. 11 shows a microphotograph of one of the fabricated chips. The BIST wrapper incurs an area overhead that is only 7.1% of the area of the $\Sigma\Delta$ ADC. This area overhead is dominated by the test stimulus generator, test response analyzer, and BIST control blocks, which are fully digital blocks. The area of the modulators has not been

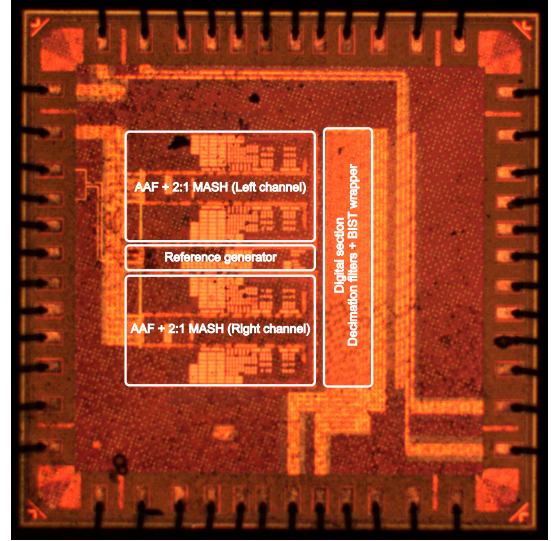


Fig. 11. Microphotograph and floorplanning of the fabricated $\Sigma\Delta$ ADC IP with BIST.

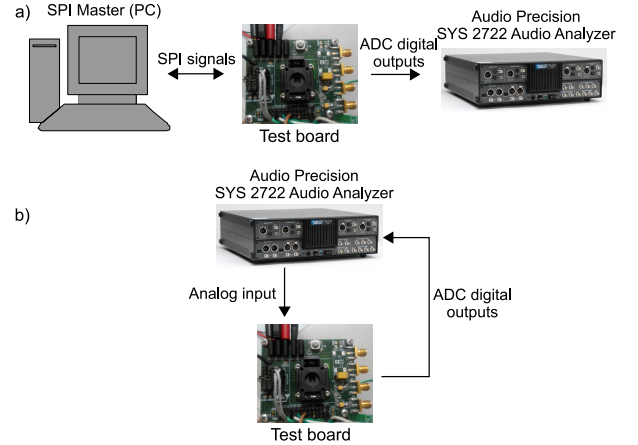


Fig. 12. a) Test setup for injection of digital ternary test stimulus in BIST mode; b) Functional specification test setup.

modified since the extra switches for injecting the ternary test stimulus have been inserted within the existing layout of the modulators. Furthermore, no power consumption overhead is observed during test mode since power consumption is dominated by the analog section of the $\Sigma\Delta$ ADC which is not modified.

In order to validate the feasibility of the proposed BIST strategy and the functionality of the test instruments within the BIST wrapper, we set up a batch of experiments to compare the BIST to the standard functional specification test approach. The BIST is based on a digital ternary test stimulus that encodes a high-resolution analog sine-wave, whereas the standard functional specification test approach is based on applying directly a high-resolution analog sine-wave at the input of the ADCUT.

Our first test setup, conceptually depicted in Fig. 12, aims at showing the equivalence between the proposed digital ternary test stimulus and the standard functional specification test. Firstly, we use the configuration of Fig. 12(a) where

we employ a conventional workstation as SPI master device for configuring and executing the BIST program and an Audio Precision Audio Analyzer for computing the SNDR. The functional specification test uses the test configuration of Fig. 12(b) where an Audio Precision Audio Analyzer is employed both for generating the high-resolution analog sine-wave test stimulus and for computing the SNDR. The procedure is repeated considering seven different input amplitudes, i.e. -59.1 dBFS, -31.7 dBFS, -14.6 dBFS, -10.6 dBFS, -8.6 dBFS, -6.4 dBFS, and -3.0 dBFS, and for the 2 channels of all 56 fabricated chips (i.e. 112 ADCUTs in total).

The SNDR values obtained using the digital ternary test stimulus and the standard functional specification test, as well as their comparison, are shown in Fig. 13. In the x-axis, we show the amplitude of the signal at the input of the modulator, while in the y-axis we show the measured SNDR values obtained by processing directly the ADCUT output, i.e. without employing the test response analyzer block. Fig. 13(a) shows the SNDR measured using the functional specification test, Fig. 13(b) shows the SNDR measured using the digital ternary test stimulus, and Fig. 13(c) shows a superposition of both sets of curves in Fig. 13(a) and Fig. 13(b) for a direct visual comparison.

By comparing Fig. 13(a) and Fig. 13(b), for the standard functional specification test set up, we observe that the amplitude of the signal at the input of the modulator is consistently attenuated. This attenuation is clearly visible by looking at the position of the data points on the x-axis. As it can be observed, the circle markers in Fig. 13(a) are consistently 2.3 dBFS below the diamond markers in Fig. 13(b) when the markers are projected to the x-axis (i.e. modulator input amplitude) for all seven test stimuli considered in our experiment. This constant attenuation of the input amplitude is due to the anti-aliasing filter that is placed before the modulator. It is not apparent when using the digital ternary test stimulus generator because the anti-aliasing filter is disconnected from the signal path and the ternary test stimulus is fed directly into the modulator. In Fig. 13(b), the higher spread of the SNDR measurements that appears for input amplitudes close to the FS can be easily explained by the fact that these input amplitudes are in the vicinity of the stability limit of the modulator. In contrast, in Fig. 13(a), the SNDR measurements obtained by the functional specification test do not show a similar spread because the input amplitude is attenuated by the anti-aliasing filter and the signal amplitude at the input of the modulator is less than the stability limit. The knee that is apparent in the SNDR measurements in Fig. 13(a) is due to the additional distortion introduced by the anti-aliasing filter that essentially limits the SNDR of the ADC in normal operation. From Fig. 13(c) it can be seen that the SNDR measurements obtained using the digital ternary test stimulus track very well, along the complete input amplitude range, the SNDR measurements obtained with the standard functional specification test.

Fig. 14 shows the histogram of the SNDR estimation error, defined as the difference between the SNDR obtained by the standard functional specification test and by using the digital ternary test stimulus. The histogram is produced by considering all fabricated chips and by measuring the SNDR

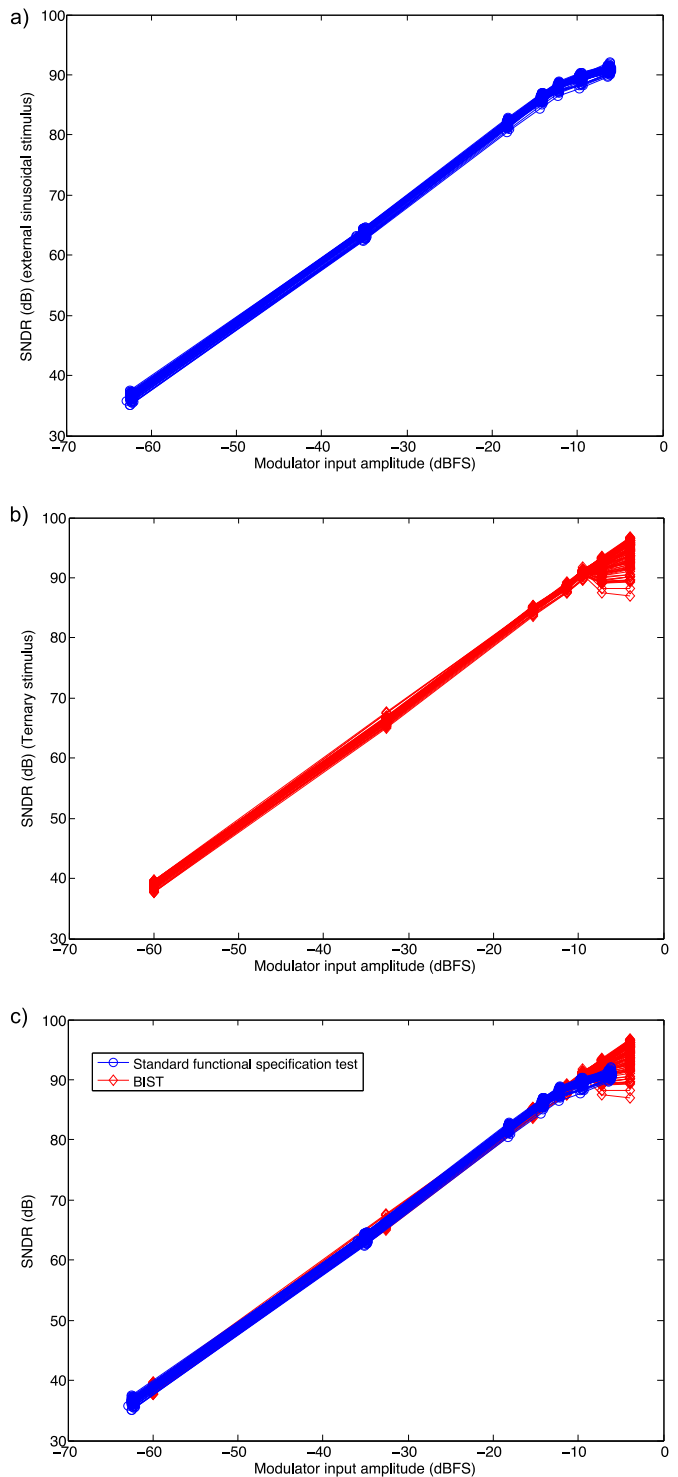


Fig. 13. SNDR measured by processing directly the ADCUT output versus the signal amplitude at the input of the modulator: (a) standard functional specification test and (b) digital ternary test stimulus. Each curve corresponds to the SNDR of one channel of a fabricated chip (i. e. in total $2 \times 56 = 112$ curves). The curves in (a) and (b) are superimposed in (c) for the purpose of comparison.

in both ways at different input amplitudes, i.e. -59.1 dBFS, -31.7 dBFS, -14.6 dBFS, -10.6 dBFS, and -8.6 dBFS. Higher amplitudes close to the FS are excluded since, as explained above, they give rise to other phenomena (e.g.

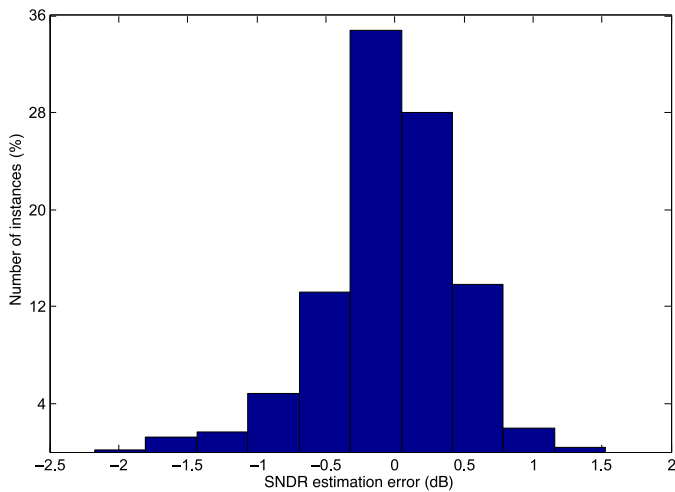


Fig. 14. Histogram of SNDR estimation error.

instability of modulators, distortion introduced by the anti-aliasing filter) which are not related to the BIST precision. A good indicator of the average precision of the SNDR measurement using the digital ternary test stimulus is the standard deviation σ of the SNDR error distribution. From Fig. 14, we calculate $3\sigma = 1.4$ dB, which is essentially equivalent to the precision of the standard functional specification test performed on dedicated ATE. Therefore, the results demonstrate the equivalence between the proposed digital ternary test stimulus and the functional specification test that employs a high-precision analog sine-wave test stimulus.

Regarding the test response analyzer, upon first silicon inspection, we found a routing error of the digital input signal FSYNC_IN that had passed undetected during the pre-silicon verification process. This error affects only the functionality of the test response analyzer block. Nevertheless, since this is a fully-digital block and the output signals of the ADCUT are accessible from primary pins, we were able to replicate the functionality of this block in software to validate the proposed signal processing algorithm. We used the test setup in Fig. 12(a) with the exception that the digital output of the ADC is now routed back to the workstation and fed to a software implementation of the test response analyzer block. The SNDR computed by the test response analyzer block is compared to the SNDR measurement obtained by the functional specification test across different input amplitudes for one random chip, as shown in Fig. 15. As it can be seen, the two measurements track each other very well across the complete input amplitude range. As before, for input amplitudes close to FS, the differences are explained by the anti-aliasing filter that is disconnected during the BIST execution.

V. CONCLUSIONS

We have presented a 40nm CMOS 18-bit stereo audio $\Sigma\Delta$ ADC that features a fully-digital BIST wrapper for measuring the SNDR on-chip. The proposed BIST is based on injecting a digital ternary test stimulus that encodes a high-precision analog sine-wave directly into the input of the modulator. The

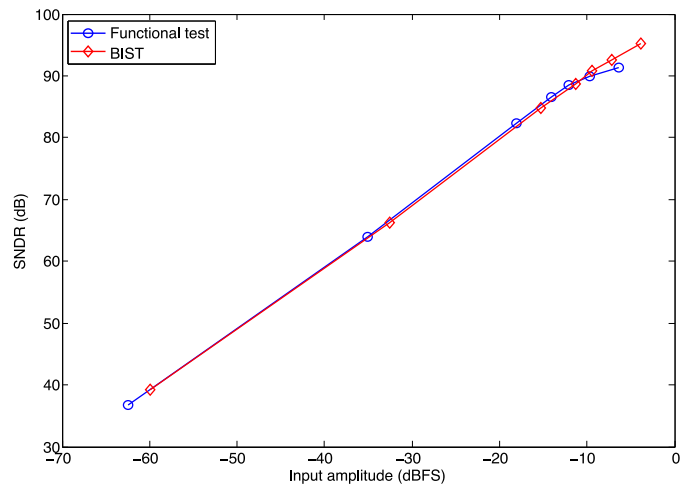


Fig. 15. SNDR measurement using the BIST (the test response analyzer is implemented in software) and the standard functional specification test as a function of the signal amplitude at the input of the modulator.

test response analysis is also carried out on-chip based on a simplified sine-wave fitting algorithm. The BIST includes a dedicated control block based on a standard SPI bus for switching to test mode, monitoring the test execution, and reading out the test results. The estimated total area overhead of the BIST is 7.1% and the total test time per channel is 28 ms. Experimental results on 56 fabricated chips prove the feasibility and effectiveness of the proposed BIST approach. Results show an excellent match across the complete dynamic range between SNDR measurements obtained using BIST and SNDR measurements obtained using standard functional specification test on precision equipment.

Future work will be aimed at extending the functionality of the BIST circuitry for enhancing the performance and reliability of the $\Sigma\Delta$ ADC. One clear research path in this line is the calibration of the $\Sigma\Delta$ ADC by taking advantage of the reference digital channel in the BIST wrapper to provide a “golden reference” signal.

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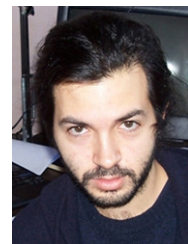
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Manuel J. Barragan (M'14) received a M.Sc. degree in Physics in 2003 and a PhD in Microelectronics in 2009, both from the University of Seville, Spain. He is currently a researcher with the French National Research Council (CNRS) at TIMA Laboratory, France. His research is focused on the topics of test and design for testability of analog, mixed-signal, and RF systems. He served as the General Chair of the 2014 Statistical Test Methods Workshop, as the Program Chair of the 2015 IEEE International Workshop on Test and Validation of High Speed Analog Circuits, as the Program Chair of the 2016 IEEE International Mixed-Signal Testing Workshop, and as Track Chair of the Test and Reliability track of the 2014 IEEE International Conference on Electronics Circuits and Systems. He currently serves in the Technical Program Committee of the Design, Automation, and Test in Europe (DATE) Conference and as a Review Editor for Wiley International Journal of Circuit Theory and Applications. His PhD research won a Silver Leaf Award at the IEEE PRIME conference in 2009 and in 2011 his work was selected for inclusion in the 20th Anniversary Compendium of Most Influential Papers from the IEEE Asian Test Symposium. He received the Best Special Session Award in the 2015 IEEE VLSI Test Symposium.



Rshdee Alhakim received the Diploma in electronic engineering from the University of Damascus, Syria, in 2004, the M.Sc. degree in communications engineering technology from the University of Brest, France, in 2008, and the Ph.D. degree in telecommunications engineering and signal processing from the University of Grenoble, France, in 2013. Currently he holds a post-doc position at TIMA Laboratory (France). His research interests are digital signal processing and image processing.



Haralampos-G. Stratigopoulos (S'02-M'07) received the Diploma in electrical and computer engineering from the National Technical University of Athens, Greece, in 2001 and the Ph.D. in electrical engineering from Yale University, USA, in 2006. He is currently a Researcher with the French National Center for Scientific Research (CNRS) at Laboratoire d'Informatique de Paris 6 (LIP6), Paris, France. His research interests are in the areas of design, test, and computer-aided design tools for analog, mixed-signal, and RF circuits and systems.

He served as the Program Chair of the 2010 IEEE International Workshop on Test and Validation of High Speed Analog Circuits and the 2011 IEEE International Mixed-Signals, Sensors, and Systems Test Workshop and as the General Chair of the 2015 IEEE International Mixed-Signals Test Workshop. He has served on the Technical Program Committees of Design, Automation, and Test in Europe Conference (DATE), IEEE International Conference on Computer-Aided Design (ICCAD), IEEE VLSI Test Symposium (VTS), IEEE European Test Symposium (ETS), IEEE International Test Conference (ITC) and several others international conferences. He is an Associate Editor of Springer Journal of Electronic Testing: Theory & Applications, IEEE Design & Test Magazine, and IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems. He received the Best Paper Award in the 2009, 2012, and 2015 IEEE European Test Symposium.



Matthieu Dubois Matthieu Dubois received the Ph.D. degree in microelectronics from the University of Grenoble Alpes, Grenoble, France, in 2011. From 2006 to 2010 he was a PhD student at TIMA laboratory, Grenoble, France, working in the Reliable Mixed-signal Systems (RMS) group. His research field concerned mainly built-in test techniques for ADCs. He is currently working on the development of ADC architectures for imaging applications in Pyxalis, Grenoble, France.



Salvador Mir (M'99) has an Industrial Engineering (Electrical, 1987) degree from the Polytechnic University of Catalonia, Barcelona, Spain, and M.Sc. (1989) and Ph.D. (1993) degrees in Computer Science from the University of Manchester, UK. He is a Research Director of CNRS (Centre National de la Recherche Scientifique) at TIMA Laboratory in Grenoble, France. He is currently director of TIMA and member of the RMS (Reliable Mixed-signal Systems) Group. His research interests are in the field of mixed-signal/RF/MEMS test.



Hervé Le-Gall started his career on silicon test working with space products in 1982. For many years he has been in charge of managing field experiments in test rooms worldwide. Today he uses this knowledge to develop novel DfT solutions and test methodologies. He managed the High-Speed Interface Test and Engineering teams in ST's Digital Group. Hervé participated in TOETS and ELESIS European projects. His research interests include advanced testing methodologies for ADCs, jitter measurement, and high-speed links. He has

published several patents on these topics.



Neha Bhargava received Bachelor in Electronics and Telecommunication Engineering from National Institute of Technology Bhopal, India, in 2002 and M.E. in Microelectronics from Indian Institute of Science, Bangalore, India, in 2004. She has since been working with STMicroelectronics, Greater Noida, India on data converters and signal processing solutions.



Ankur Bal received the B.E. degree in electrical engineering from Delhi College of Engineering, University of Delhi, Delhi, India, in 1999. He joined STMicroelectronics in 1999 as a Design Engineer. Since December 1999, he has been working at ST Microelectronics on various aspects of VLSI design and Digital Signal Processing. His current interests include high precision sigma delta data converters, high speed Nyquist data converters and Clock generators.