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Corresponding Author: Dr Magali Brunet, PhD

Corresponding Author's Institution: CNRS ; LAAS

First Author: Magali Brunet, PhD

Order of Authors: Magali Brunet, PhD; Hicham Mafhoz Kotb; Laurent Bouscayrol; Emmanuel Scheid; Michel Andrieux; Corinne Legros; Sylvie Schamm-Chardon

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*Reply to Editor and Referees

CENTRE NATIONAL DE LA RECHERCHE SCIENTIFIQUE

Magali Brunet
Research Scientist,
LAAS-CNRS, 7 avenue du Colonel Roche,
31077 Toulouse Cedex 4, France

To Associate Editor, Patrick Desjardins
University of Illinois at Urbana-Champaign, USA

Toulouse, 25th February 2011,

Dear Pr. Desjardins,

Please find enclosed the revised paper entitled **'Nano-crystallized tetragonal metastable ZrO_2 thin films deposited by MOCVD for 3D capacitors'** by M. Brunet et al. for publication in Thin Solid Films.

We have corrected our manuscript according to the final recommendation of the reviewers. The manuscript has been corrected by a native English speaker as requested.

We hope that the manuscript is now up to the standards of Thin Solid films and can be published.

With my best regards,

Magali Brunet, on behalf of all co-authors

7, Av. du Colonel Roche – 31077 Toulouse Cedex 4 – France
Tél : National : 05.61.33.62.00 – international : +33.5.61.33.62.00
Télécopie : National : 05.61.55.35.77 – international : +33.5.61.55.35.77
Email : mbrunet@laas.fr – Web : http://www.laas.fr

Nanocrystallized tetragonal metastable ZrO_2 thin films deposited by metal-organic chemical vapor deposition for 3D capacitors

M. Brunet[1*], H. Mafhoz Kotb[2], L. Bouscayrol[1], E. Scheid[1], M. Andrieux[3], C. Legros[3], S. Schamm-Chardon[4].

[1] *CNRS ; LAAS ; Université de Toulouse ; 7 avenue du Colonel Roche, F-31077 Toulouse, France.*

[2] *Physics Department ; Faculty of Science ; University of Assiut ; Assiut 71516, Egypt.*

[3] *Université Paris Sud 11 ; LEMHE-ICMMO ; CNRS UMR 8182 ; Bât. 410, F-91405 Orsay, France.*

[4] *CEMES-CNRS ; Université de Toulouse ; nMat group ; BP94345, F-31055 Toulouse, France.*

** Corresponding author: Magali Brunet, LAAS-CNRS, 7 avenue du Colonel Roche, 31077 Toulouse Cedex 4, France ; email: mbrunet@laas.fr ;*

Tel: 00 33 5 61 33 61 21; fax: 00 33 5 61 33 62 08

Abstract: ZrO_2 is a potential candidate for the realization of 3D capacitors on silicon for future Systems-on-Chip. This paper reports on the deposition of ZrO_2 thin films by metal-organic chemical vapor deposition on planar and 3D structures. Physico-chemical as well as electrical properties of the films are investigated. It is shown that the change of phase and microstructure of the film due to annealing at 900°C under O_2 impacts directly on the electrical performance of the capacitors. Capacitance densities are 2 nF/mm² for planar capacitors and reach 8 nF/mm² for capacitors with pores etched in silicon with a 4:1 aspect ratio.

Keywords: MOCVD, ZrO_2, cubic/tetragonal, high-k dielectric, 3D capacitors, FTIR, TEM.

1. Introduction

Today, portable electronic equipment is required to be lighter, more compact, multifunctional, rapid and highly reliable. High performance Systems-on-Chip (SoC) appear to be a logical answer to these challenges. Integrated passive devices (IPD) are particularly interesting for industry as far as the numerous passive components (capacitors, inductors and resistors) required in electronic systems are concerned. Integrated capacitors with a metal-insulator-metal (MIM) structure showing high capacitance per surface area are expected to find many applications such as decoupling, filtering output signals in DC-DC converters, energy storage or A/D conversion [1]. To reach high capacitance densities, two complementary ways must be explored: 3D architectures and integration of high-k dielectrics. In 3D architectures, very high capacitance densities can be reached through the increase of the surface to volume ratio of the electrodes. The technique of high-aspect ratio pores network etched in silicon by deep reactive ion etching (DRIE) has previously been developed [2]. An alternative technique of n-type silicon electrochemical etching with backside illumination in HF-based electrolytes has also been reported [3]. A capacitance density of up to 650 nF/mm² could be reached with the latter technique and conventional dielectrics (SiO_2 and Si_3N_4) [4]. Introducing high-k dielectrics such as HfO_2 or ZrO_2 or very high-k dielectrics such as (Pb,Zr)TiO_3 or (Ba,Sr)TiO_3 perovskites instead of SiO_2 in these high-aspect ratio structures should allow for capacitance densities higher than 1 µF/mm². For instance, atomic layer deposition (ALD) has been used to deposit Al_2O_3 dielectric layers into 30 µm deep pores in silicon [5] leading to capacitance densities of 440 nF/mm² or inside anodic aluminium oxide nanopores leading to capacitance densities of 1 µF/mm² [6]. However, the ALD rate is quite low: 0.1-1 Å/cycle with a cycle time

ranging from 1 to 10 sec. This limits its use for very thin dielectric layers. For applications such as output filters of DC-DC converters, relatively high breakdown voltages are required (10-15 V) driving the need for thicker layers than for metal-oxide-semiconductor (MOS) type applications. Metal-organic chemical vapor deposition (MOCVD) allows deposition of quite thick layers of binary and ternary oxides with a high deposition rate (0.1–1000 Å/s).

As a high-k dielectric, ZrO_2 is a promising candidate for high density capacitors as it combines a high dielectric constant and relatively high breakdown voltages: 3-6 MV/cm [1, 7, 8, 9]. The dielectric static response of ZrO_2 was calculated by Zhao et al. [10, 11]. It is much higher for the cubic and tetragonal phase (($\varepsilon_{r(c)}$ = 37 and $\varepsilon_{r(t)}$ = 38, respectively) than for the monoclinic phase ($\varepsilon_{r(m)}$ = 20). Therefore, tetragonal/cubic phases must be present if high capacitance densities are to be reached. We have already deposited ZrO_2 thin films with a tetragonal phase by direct liquid injection MOCVD (DLI-MOCVD) on planar and tridimensional surfaces (high-aspect ratio pores etched in silicon) [12, 13]. The influence of the deposition parameters on the physico-chemical properties of the films was investigated. The purpose of this paper is to address, for one set of deposition parameters, the effect of annealing on the morphology, the crystalline structure and the corresponding capacitance of the films for 2D and 3D MIM structures.

2. Fabrication and experimental methods

Planar and 3D capacitors were fabricated as follows: on n-type two inch silicon wafers, arrays of pores were etched by DRIE with the Bosch process using a photoresist as an etch mask [14]. The pores are 4 µm wide with an aspect ratio of 4:1. The wafers were dipped for 1 min in HF to remove the native oxide then in a bath containing tetramethyl

ammonium hydroxide (22 wt%) and isopropyl alcohol (17%) heated up at 75°C to smooth the scalloping in the pores produced with the Bosch process. The silicon substrate was highly doped with a phosphorus diffusion step ($POCl_3$ in N_2 at 1050°C for 35 min) in order to obtain a MIM structure (without depletion in the semiconductor) and to reduce the series resistance of the capacitor. After a RCA cleaning of the substrates, a thin silicon dioxide layer (12 nm) was then grown thermally through dry oxidation at 900°C for 35 min in total (5 min under O_2/N_2). This oxide layer was introduced in the stack for electrical characterization purposes. Indeed, it is known that leakage current through as-deposited high-k films is mainly due to as-grown defect states at the interface with silicon [15, 16]. The inclusion of a thin SiO_2 layer, grown on purpose, is a solution to reduce these defect states and act as a barrier for electronic transport [17].

ZrO_2 thin films with a thickness between 50 and 60 nm were deposited by DLI-MOCVD using the following precursor: $Zr_2(O^iPr)_6(thd)_2$ dissolved in cyclohexane and evaporated at 240°C. Several deposition parameters such as substrate temperature (400-900°C), injection frequency (0.5–2 Hz), total pressure in the reactive chamber (10–1000 Pa) and evaporation temperature of the precursor (200-230°C) were investigated in a previous study in order to determine the optimal conditions for the growth of a tetragonal zirconia film [12]. All these parameters were investigated and their effects analyzed. It was found that peculiar deposition conditions provided a uniform film with no cracks and a good crystallization in the expected tetragonal structure [12, 13]. The substrate temperature has especially a strong influence on the crystal structure: a substrate temperature of 525°C was selected as it is a good compromise between amorphous deposition (below 450°C) and very poor conformal deposition on 3D structures (above 550°C). Compared to the samples prepared in reference [12], the injection frequency was lowered from 2 Hz to 1 Hz in order to favor the $(111)_t$

phase which was proven in the previous study to be more stable during further annealing. Finally, the oxygen and nitrogen gas flow were set at 0.05 L/min. Several batches were deposited in such optimized conditions; each of them containing up to ten substrates (2" wafer and several 10*10 mm^2 samples) to check them using various characterization techniques. A post-annealing step was carried out on some of the substrates under oxygen gas flow at reduced pressure (100 Pa) to check its chemical stability.

Capacitors were finalized with a boron-doped polysilicon layer as the top electrode etched in a square shape (100 µm x 100 µm and 250 µm x 250 µm). The final step was the deposition of a metallic contact (Ti/Au) on the polysilicon layer as well as on top of the films for planar capacitors. As for the bottom electrode of the capacitors, an AuSb layer was deposited on the back side of the silicon substrate.

Concerning the material characterization, the crystal structure of ZrO_2 in the thin films was checked by grazing incidence (2°) X-ray diffraction (XRD) performed on a PANALYTICAL X'pert pro MRD diffractometer using $Cu_{K\alpha}$ radiation. All the patterns were realized with a detector angle (2θ) varying from 27 to 37°, a step of 0.05° and 144 s counting rate. Nanocrystallized tetragonal zirconia $ZrO_{2(t)}$, cubic zirconia $ZrO_{2(c)}$ and monoclinic zirconia $ZrO_{2(m)}$ were identified using JCPDS files #17-923, #27-997 and #37-1484 respectively. Fourier transform infra-red (FT-IR) spectroscopy was performed on samples using a Perkin Elmer 2000 FT-IR spectrophotometer in the range 4000-220 cm^{-1} as it is a sensitive technique to identify the polymorphs of zirconia, even if films are nanocrystallized. Each spectrum was obtained by averaging nine or more scans in order to obtain a good S/N ratio. Selected area electron diffraction pattern (SAED) was also performed on the planar films.

The thin film coverage in 3D structures was controlled on cross-sections with a Hitachi S-4800 scanning electron microscope (SEM). The local structural and chemical properties around the film/substrate interface and in the film were analyzed by transmission electron microscope (TEM)/high resolution (HRTEM) and electron energy loss spectroscopy with a field emission TEM (FEI Tecnai™ F20) operated at 200 kV and equipped with a spherical aberration corrector. TEM samples were prepared by classical procedures cutting the samples either perpendicular to the film/substrate interface (cross-section) or parallel to the film/substrate interface (plan-view). Electrical characterizations were conducted on the fabricated capacitors by performing impedance versus frequency measurements under point probes with an impedance analyser (Agilent 4294A) and current versus voltage measurements on a Keithley 4200 Semiconductor Characterization System.

3. Results.

3.1. Thin film characterization

Figure 1a shows the XRD results for a $ZrO_2/SiO_2/Si$ planar stack before and after annealing under O_2 at 900°C. The as-deposited film crystallized in the tetragonal/cubic phase, and after annealing the $(111)_m$ line of the monoclinic phase appeared. It is difficult to clearly distinguish the difference between the $ZrO_{2(c)}$ and $ZrO_{2(t)}$ phases due to the similarity of their patterns. It was shown by Tsoutsou et al. [18] in their study on Ge-doped zirconia films grown by atomic oxygen beam deposition that it was possible to identify the tetragonal crystalline state through the splitting of both lines at 50° or 60°. In our patterns, the large broadening of the diffraction lines due to a very small crystallite size (lower than 10 nm) hinders the discrimination of both (c) and (t) phases.

Therefore, in order to identify without any doubt the presence of (c) or (t) phases in the films, FT-IR experiments were conducted. The FT-IR spectra presented in figure 1b were compared with reported stabilized cubic, tetragonal and monoclinic zirconia spectra [19, 20]. Group theory predicts only one IR active mode for cubic zirconia that signs in figure 1b as a weak broad band between 600 and 350 cm^{-1} and an extra band at 589 cm^{-1} due to a secondary oscillator of the cubic phase. The three active modes reported for tetragonal ZrO_2 correspond to the weak bands that emerged from the broad band between 350 and 600 cm^{-1}. The monoclinic phase can be recognized when sharpen bands are added to the spectra. They correspond to the fifteen vibrational modes of the monoclinic phase of zirconia. The position of these bands is red shifted compared to those obtained theoretically on bulk zirconia. Moreover, they are broadened and flattened. These differences in the broadening and position of the absorption band could be attributed to various parameters such as the reduction of the particle size (nanostructuration), the shape of particles and a possible disordering of the oxygen sublattice [21-23]. However, despite the differences in the position of the bands, the presence of well-defined modes in the spectra supports the identification of the tetragonal and monoclinic phases rather than the cubic phase either in the as-deposited and annealed films. In the annealed films, the monoclinic character is emphasized.

From TEM analyses carried out on the $ZrO_2/SiO_2/Si$ planar stack before and after annealing at 900°C under O_2, the layer thickness was measured to be 64 and 53 nm on the as-deposited and the annealed samples, respectively (figure 2 a and b). It is worthy to note that the thickness difference between the as-deposited and the annealed sample is probably due to the annealing process that is able to densify and/or to eliminate the carboxylates impurities adsorbed during the CVD process. As a consequence, it is possible to observe a

modification of the microstructure of the film after the heat treatment. Indeed, as shown in figure 2, the as-deposited ZrO_2 layer is polycrystalline, with crystallite sizes between 5 and 10 nm. The SAED patterns of the as-deposited ZrO_2 layer provide evidence of mainly the cubic and or tetragonal ZrO_2 structure (figure 2c, insert). As for XRD patterns, the two structures are difficult to separate. However, the ring corresponding to the 0.213 nm distance can only be attributed to the low level diffracting (102) plane of the $ZrO_{2(t)}$ phase supporting the FT-IR conclusions of a major contribution of the tetragonal phase with respect to the cubic one. After annealing, a columnar organization is revealed with an increase in crystallite size due to the grain growth mechanism. The monoclinic structure appears there in addition to the cubic/tetragonal one (figure 2d, insert). In addition, the thermal SiO_2 layer, which was 12 nm, did not change after annealing (figure 2a et b).

In tridimensional structures, the coverage of the deposit was observed by SEM (figure 3). The deposition is not fully conformal: there is a loss of about 54% between the top thickness and the bottom thickness. However, it was verified with TEM analysis (figure 4-a to d), thanks to a cross-section inside a pore, perpendicular to its long axis, that the ZrO_2 layer is deposited homogeneously on the vertical pore walls. The same conclusions for the stack in planar configuration can be drawn concerning the structure of the deposit: the as-deposited ZrO_2 layer is constituted of very small crystallites of cubic/tetragonal phase with a major contribution of the tetragonal phase (SAED not shown) that grow after annealing and transform to the monoclinic phase (SAED not shown) (figure 4-e and f).

3.2. Electrical characterization

Figure 5 shows the capacitance density versus frequency of planar and 3D capacitors. The capacitance was 8 nF/mm² for 3D capacitors with as-deposited ZrO_2, which is about three times better than planar capacitors. In addition, annealed samples always have lower capacitance than as deposited ones (5.4 nF/mm² for 3D capacitors, 1.9 nF/mm² for planar capacitors).

The measured capacitance is an equivalent one, which contains the capacitance of the SiO_2/ZrO_2 stack with parasitic incorporated due to electrodes and interfaces. Models were thus developed on planar capacitors to extract the pure capacitance of the ZrO_2 layer and therefore, the permittivity. The model curves are superposed on the measured curves in figure 5 for planar capacitors with as-deposited ZrO_2 and annealed ZrO_2. The equivalent circuits used for modeling are shown in figure 6. In these models, identified contributions are: C_{ox} (the capacitance of the SiO_2 layer), Rp_{ox} and Rp_{ZrO2} (the parallel resistance of each layer representative of the leakage current), and Rs (the series resistance due to electrodes). In the model for the as-deposited film, the branches C1 R1, C2 R2, C3 R3 and C4 R4 are representative of interface states distributed in energy [24]. Only one C1 R1 interface branch was necessary for modeling the annealed film. With these models, the capacitance of the ZrO_2 layer (C_{ZrO2}) was extracted as 190 pF for both the as-deposited film and the annealed film. Using a thickness of 64 nm and 53 nm for the as-deposited and annealed ZrO_2 films, respectively, the permittivities of theZrO_2 layers are calculated to be 27 and 22.7.

In figure 7, for as-deposited and annealed samples (planar capacitors), the current density is plotted versus the electrical field of the stack capacitor where $E = V/t_{stack}$;

$t_{stack} = t_{SiO2} + (\varepsilon_{SiO2}/\varepsilon_{ZrO2})*t_{ZrO2}$ [25]

In both case, the current at low bias (below 1-2 MV/cm) followed the same behavior and was of the order of 1 nA/cm². At higher bias, i.e. above 2.5 MV/cm for the as-deposited layer and above 1.5 MV/cm for the annealed layer, the current mechanism changed: a sharp increase of the leakage current was observed. The breakdown took place at a lower bias (around 2 MV/cm) for the annealed sample than for the as-deposited sample.

4. Discussion

4.1. On the material structure.

It is well known that preparation methods (physical or chemical processes), preparation parameters (temperature of growth and O_2 partial pressure) [7, 26, 27] and film thicknesses [27-30] greatly influence the crystalline structure of the deposited material. In particular, for the zirconia system, general trends can be drawn for ZrO_2 polymorph. The monoclinic phase is favoured by high growth temperature and thick films. Furthermore, the crystallographic structure is dependent on the size of the crystallites [31]. This point is well discussed in the works of Bernard, Filipovitch and Garvie [27, 32, 33]. The general principle discussed is that the tetragonal phase is stabilized in thin films because of the small size of the crystallites having a lower surface energy compared to the crystallites of the monoclinic phase.

It was shown in figure 1b that the FT-IR spectra of as-deposited and annealed films are clearly structured with an increase in the number of modes going from as-deposited to annealed films. This supports the results observed by XRD (figure 1a) showing the growing of the monoclinic phase with annealing. In the as-deposited films, the monoclinic phase is also present, though with a minor contribution, together with the cubic phase (secondary oscillator band at 589 cm^{-1}). However, two observations, clearly visible in the

as-deposited films, support the presence of the tetragonal phase in the films. First, if we consider that the cubic or tetragonal phase of ZrO_2 is mainly present in the as-deposited films as revealed in the XRD patterns, the presence of structured modes in the corresponding FT-IR spectra can only support the presence of mainly the tetragonal phase. Second, we showed in a previous work [13] that the cubic zirconia phase transforms more easily into the monoclinic phase than the tetragonal phase during annealing under oxygen flow. As a consequence, in the present study, if the cubic phase amount was very large in the as-deposited films, they should easily transform during annealing into the monoclinic phase and a large number of monoclinic absorption bands should be observed on the spectrum. As shown in figure 1b, the monoclinic absorption bands do not evolve strongly during annealing. This confirms that the as-deposited films crystallize mainly in the tetragonal structure.

In this work, for a film thickness of around 60 nm, it has been verified with three different methods (XRD, FT-IR and SAED) that the deposited ZrO_2 crystallizes mainly in its tetragonal structure with crystallite sizes of the order of 5 nm. In addition, the monoclinic phase appears in the corresponding annealed film with crystallite sizes of around 15 nm. This work confirms our previous results that for thicknesses in the range of 50-100 nm, it is possible through particular deposition conditions to stabilize the tetragonal zirconia phase [12]. As a consequence, initial crystallite size associated with grain growth during deposition and/or annealing may be the key parameter to control the existence of the tetragonal metastable phase.

4.2. On the electrical performance.

The measured permittivities are 27 and 22.7 for the as-deposited layer and the annealed layer, respectively. This difference is attributed to the crystalline phase of the ZrO_2 layer: the contribution of the monoclinic phase appearing after annealing presents a lower permittivity, which decreases the overall permittivity. The measured ε_r for (c)/(t) phase is lower than the theoretical value (ε_r = 38) calculated by Zhao et. al [10, 11], but higher than permittivities usually reported in the literature: between 16 and 25 [7, 9, 29, 34, 35]. It was also observed that the electrical model for the annealed sample is much simpler than for the as-deposited one. This verifies the common knowledge that annealing reduces the defect states at the interfaces [15, 16, 17]. For 3D capacitors, the same decrease in capacitance was observed: it is 8 nF/mm² for as-deposited films and 5.4 nF/mm² after annealing. The gain in capacitance density from planar to 3D capacitors is about 3 for as-deposited layer or annealed layer. A simple geometry calculation based on relation (1) indicates that the enhancement factor (3D electrode surface (S_{3D})/ Planar electrode surface (S_{plan})) should be 4.7 for the realized pores.

$C = \frac{\varepsilon_0 \varepsilon_r}{t_{stack}} \frac{S_{3D}}{S_{plan}}$ with $S_{3D} = S_{plan} + 4nwh$ with t_{stack} the dielectric thickness, n the number of pores etched in the substrate, w the pore width and h the pore depth.

The difference between the measured enhancement and the calculated one is due to the ZrO_2 layer which is not conformal on the 3D structure: the layer at the bottom is thinner (25 nm) than at the top (55 nm) reducing the equivalent permittivity of the SiO_2/ZrO_2 stack. The lack of conformity in high-aspect ratio structures can be explained by the fact that the deposition is diffusion limited because of a high surface reaction rate. Although low temperature and low pressure should reduce surface reaction and promote diffusion of reactive species in 3D structures against a surface reaction, the MOCVD equipment was

not designed to operate below 100 Pa. Furthermore, lower temperature would lead to a non stoechiometric zirconium oxide, which would enhance leakage current.

The measured leakage currents are representative of the silicon oxide layer because in dielectrics stack, the oxide of best quality, SiO_2 in this case, drives the current mechanism. It can be noted first that the leakage current density is much lower than for ZrO_2 layers deposited by MOCVD in the same conditions directly on silicon [36]. For bias above 1 MV/cm, the current density is increasing drastically: this behavior was already reported in the literature [37]. It is believed that in this configuration (bi-layer SiO_2/ZrO_2), electrons first tunnel through the SiO_2 layer (direct tunneling) and then tunnel through traps located in the high-k layer [38], which is representative of Poole-Frenkel emission.

Similarly to the leakage current, the breakdown voltage plotted in figure 7, is representative of the SiO_2 layer. The breakdown voltage is about 6 MV/cm for the as-deposited layer and 2 MV/cm after annealing. These values are much lower than what is the usually reported breakdown voltage for thermal SiO_2, i.e. around 13 MV/cm. The phosphorus diffusion step before the thermal oxidation is probably one cause of a lower breakdown voltage as doping impurities may diffuse in the oxide during its growth. On the other hand, the annealing step under O_2 is another cause of the degraded breakdown voltage, since the microstructure of the film is changing. Indeed, after annealing the grain size is increasing and a preferred orientation is favored in the layer: the $(200)_t$ peak is slightly increased in the XRD pattern (fig. 1a) and in the TEM analysis is associated with a columnar microstructure that is clearly visible (fig. 2b). This columnar structure leads to more conduction paths through grain boundaries, eventually causing premature breakdown of the stack.

5. Conclusions

Planar and 3D MIM-like capacitors with ZrO_2 as the high-k dielectric were prepared and characterized. The tetragonal phase of ZrO_2, in films with a thickness ranging from 50 to 60 nm, was stabilized through peculiar MOCVD conditions. It was demonstrated that the change of phase and microstructure of the film due to annealing at 900°C under O_2 impacts directly on the electrical performance of the capacitors. Intrinsically, the permittivity of ZrO_2 is lowered with the annealing step due to the partial tetragonal/monoclinic phase transformation. Extrinsically, although the quality of the interfaces of the overall stack is improved, the change in microstructure (larger grains and columnar structure) is responsible for the higher leakage current and lower breakdown voltage.

3D capacitors showed four times larger capacitance density (8 nF/mm²) compared to planar ones (2 nF/mm²). Although the deposition parameters giving conformal deposition were not found for this precursor in this particular MOCVD equipment, it is believed that conformal deposition of ZrO_2 in very high-aspect ratio structures should lead to very high capacitance densities.

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Figure captures:

Figure 1. Chemical and structural characterization of a ZrO_2 film deposited at 525°C and annealed for 1h at 900°C under O_2 at P_{tot}=100 Pa : a) XRD patterns and b) FT-IR spectra.

Figure 2. TEM images of $ZrO_2/SiO_2/Si$ stack a) and c) as-deposited, b) and d) after an annealing step at 900°C under O_2. Top: bright field images on cross-sections where all the stacks can be seen. Bottom: dark-field images on plan-view where crystals appear with a white contrast. Selected area electron diffraction patterns are inserted. The arrows sign the position of the (102) plane of $ZrO_{2(t)}$. In c) radial intensity profile from the rotational average is inserted.

Figure 3. SEM images of $ZrO_2/SiO_2/Si$ coverage inside pores (4.9 µm*4.9 µm*11.9 µm). Thickness of 55 nm and 25 nm at the top and at the bottom of the pore respectively.

Figure 4. TEM images of $ZrO_2/SiO_2/Si$ inside pores (4.9 µm*4.9 µm*11.9 µm) in cross-section configuration (perpendicular to the principal axis of the pore) (a to d) and in plan-view configuration (e, f). On the left, the as-deposited sample and on the right, the annealed ones at 900°C under O_2.

Figure 5. Measured specific capacitance versus frequency for planar and 3D capacitors, as-deposited and after annealing under O_2 at 900°C.

Figure 6. Equivalent circuits for planar capacitors with SiO_2/ZrO_2 layer a) as-deposited, b) annealed.

Figure 7. Characteristics J(E) of as-deposited and annealed planar capacitors.

Figure 1

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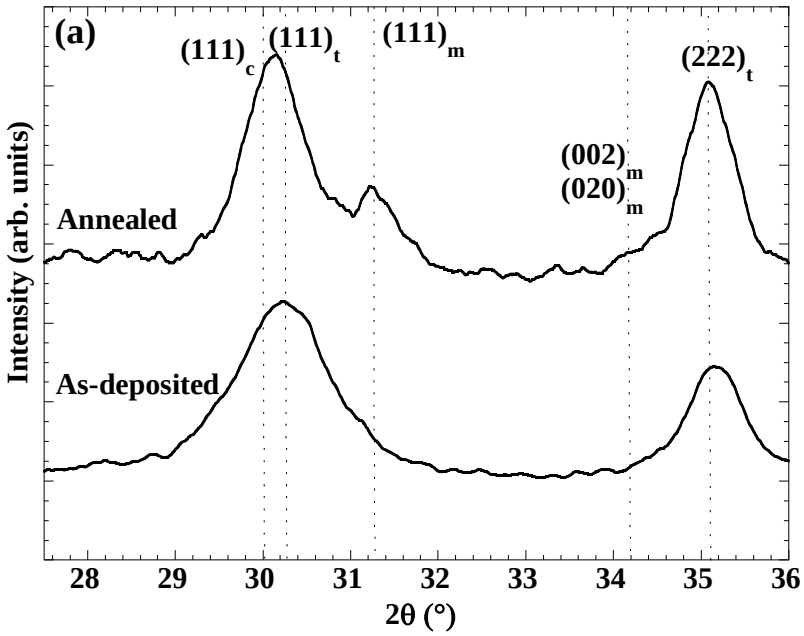

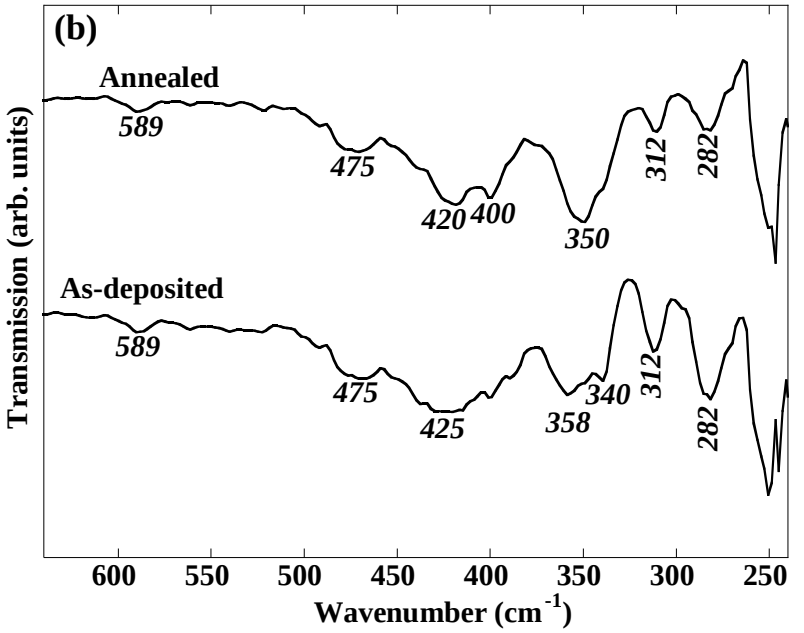

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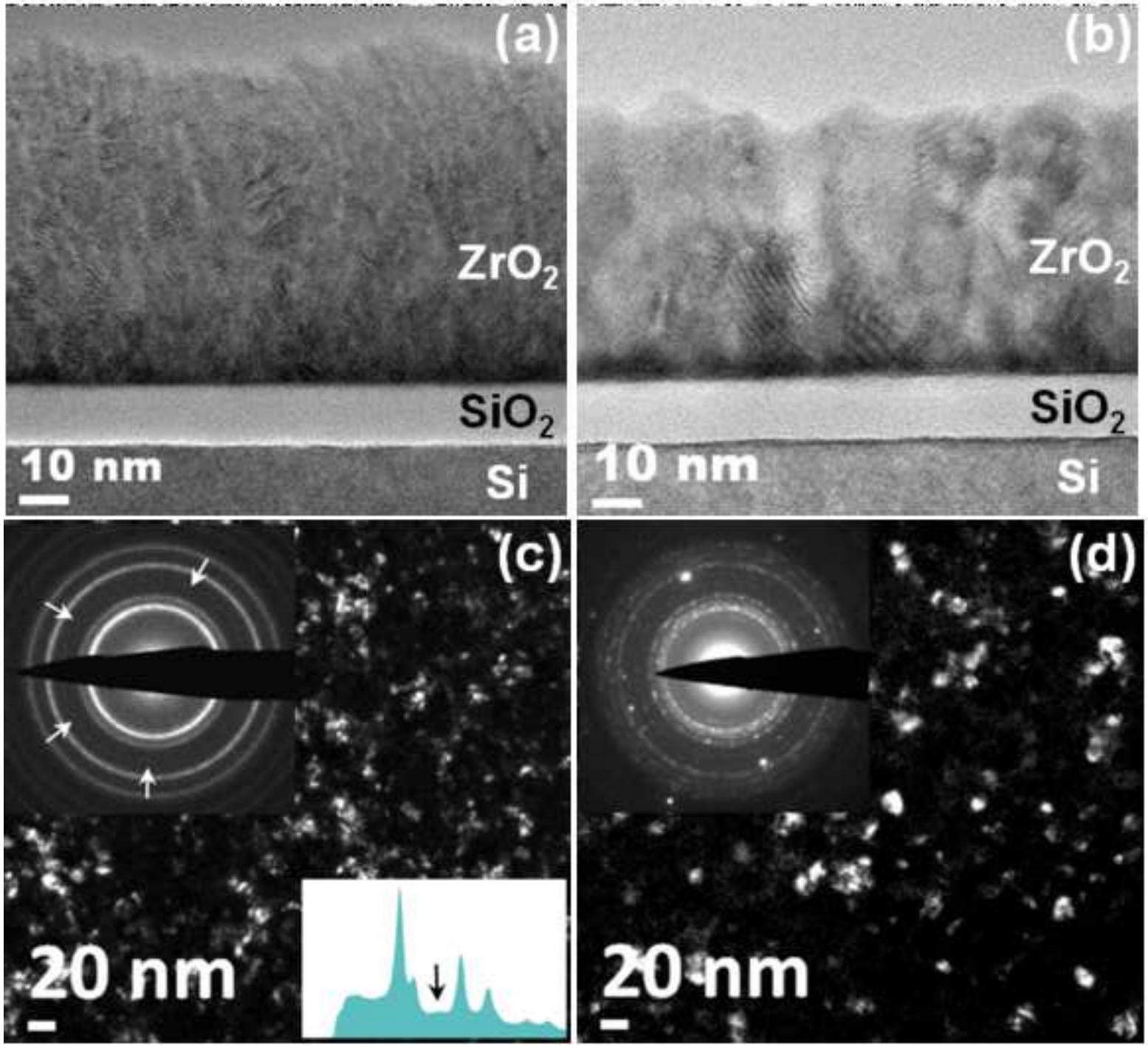

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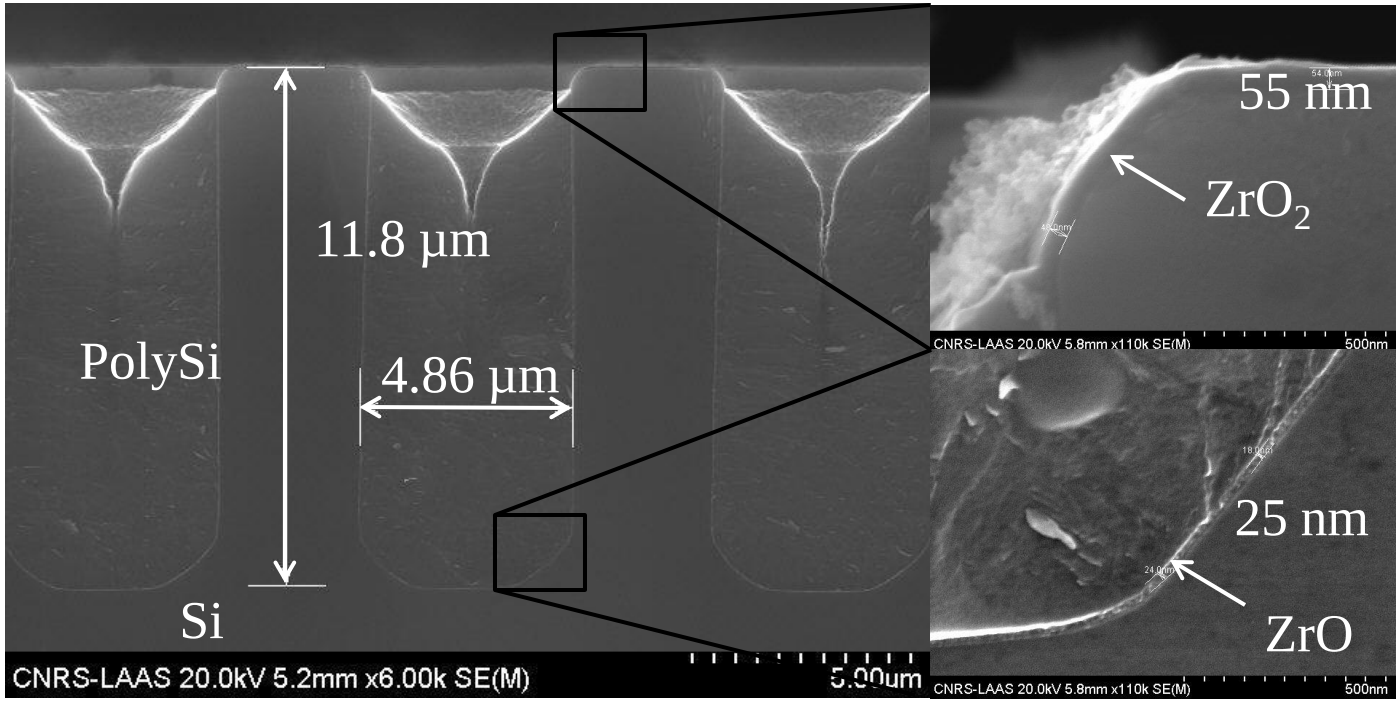

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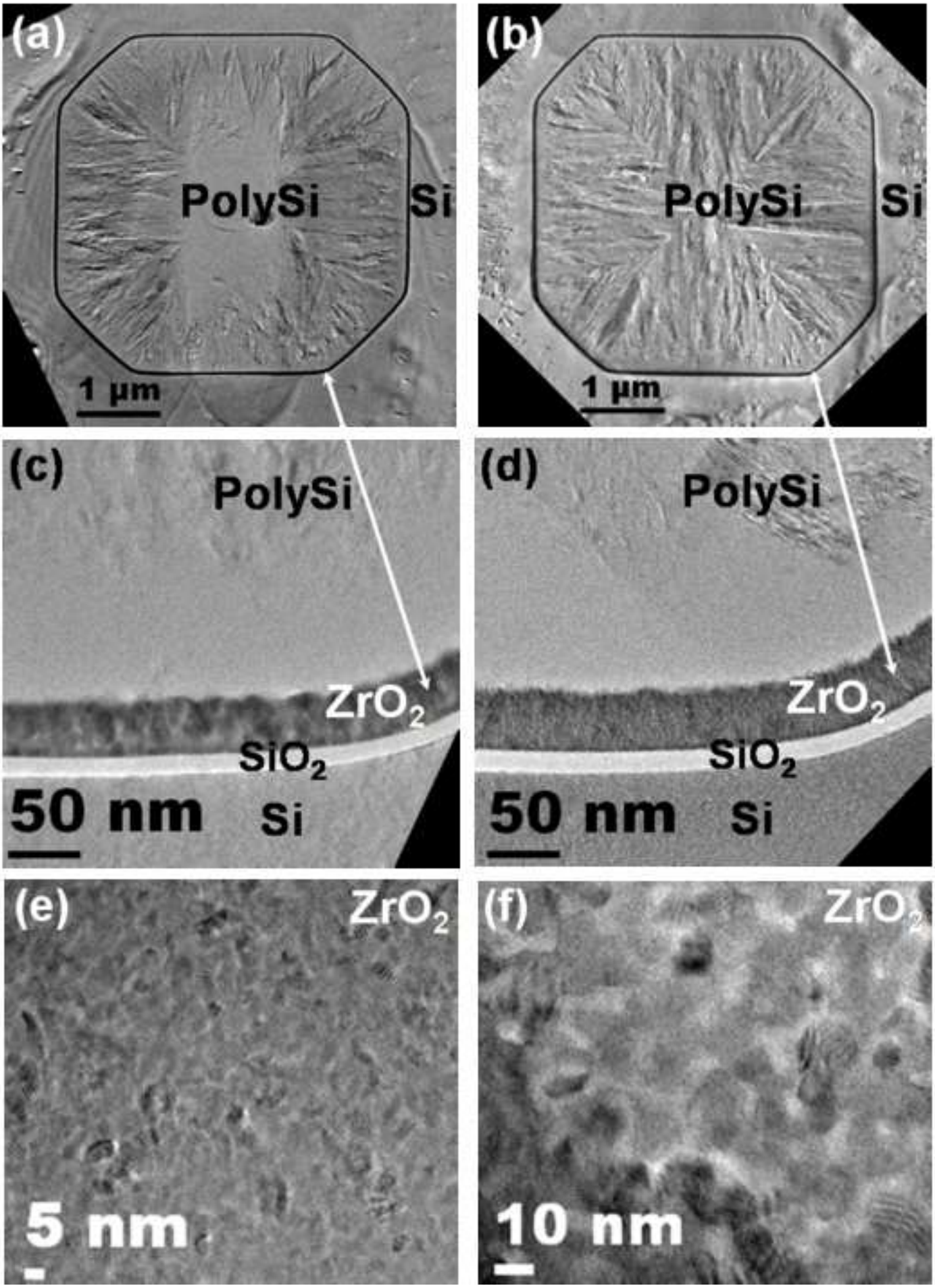

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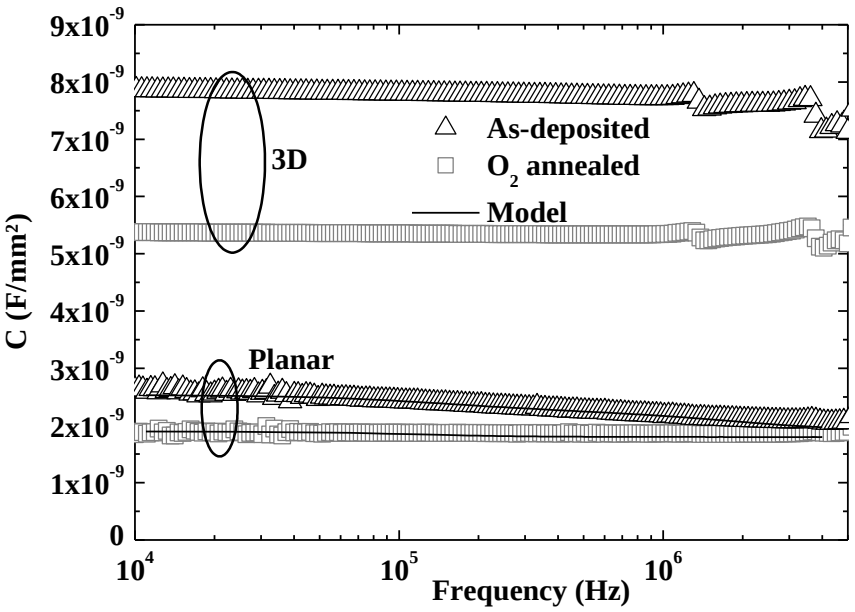

Figure 6

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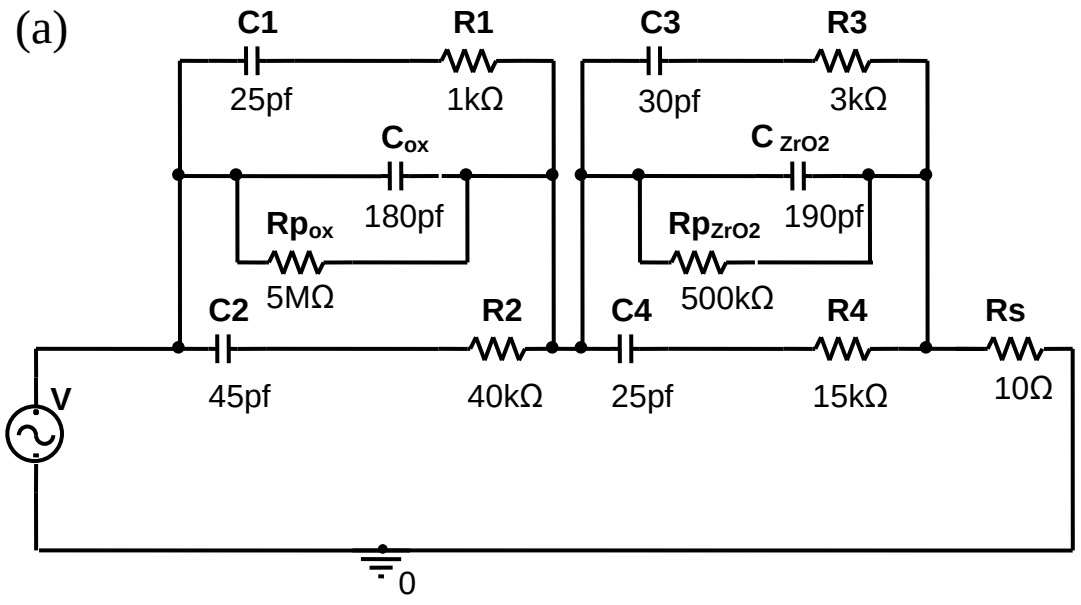

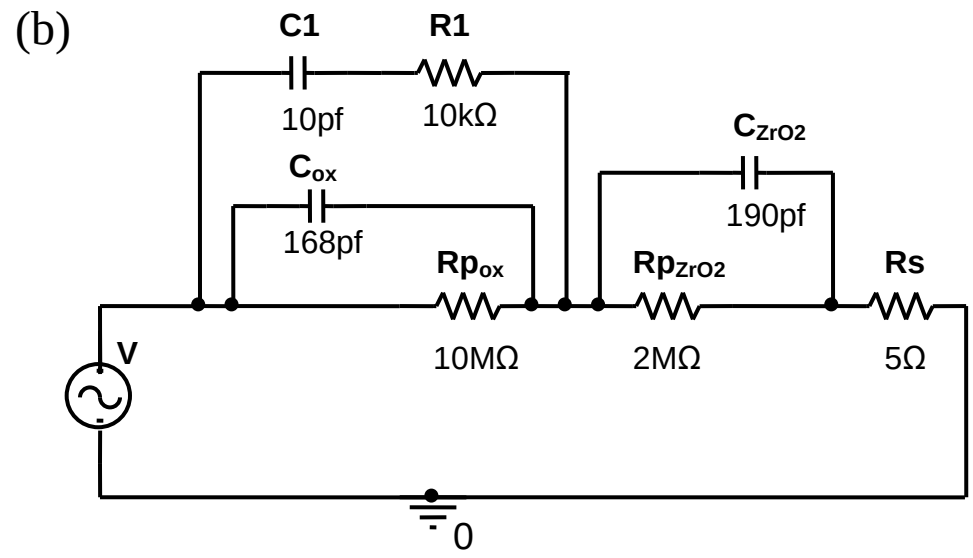

Figure 7

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