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► **To cite this version:**

Philippe Artillan, Magali Brunet, David Bourrier, Jean-Pierre Laur, Nicolas Mauran, et al.. Integrated LC filter on silicon for DC-DC converter applications. IEEE Transactions on Power Electronics, 2011, 26 (8), pp.2319-2325. 10.1109/TPEL.2010.2102776 . hal-01443073

HAL Id: hal-01443073

<https://hal.science/hal-01443073>

Submitted on 22 Jan 2017

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Integrated LC filter on silicon for DC-DC converter applications

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Abstract—The integration of passive components on silicon for future DC-DC converters applications is still a challenging area of research. This paper reports the microfabrication of a fully integrated filter containing a spiral inductor on top of a 3D capacitor. A thin magnetic shielding layer is introduced between the two components demonstrating that losses caused by the inductor in the capacitor area are reduced, thus increasing the maximum working frequency of the whole component. The fabricated filter was characterized in a test circuit (buck-type converter).

Index Terms—Integrated circuit fabrication, Electromagnetic induction, Inductors, Capacitors, Energy conversion, Magnetic shielding.

I. INTRODUCTION

The ever reducing size of electronic hand-held equipments combined with the increase in the number of functionalities, reveals a blocking point relative to the power management of systems. In embedded systems, switched-mode DC-DC converters can be used for supplying devices which do not require an extremely low noise supply voltage but are the most power consuming (e.g. memory chips, base-band cores, power amplifiers). Typical application ranges are input and output voltages less than 5 V. For those high consumption devices, the converter has to provide an important output current: at least 100 mA and up to 1 A, higher values being provided by several parallel converters. DC-DC converters will have to adapt to these new power requirements while being reduced in size and improved in terms of efficiency, cost and reliability.

The choice of the switching frequency depends on the size allocated to the DC-DC converter, the switching time limitation due to switch drivers and finally the global efficiency of the converter. The global efficiency is in turn affected by active losses (conduction and

switching losses, required energy in drivers) and passive losses (conductors and magnetic core in inductors, equivalent series resistance in capacitors). Although it is difficult to propose a closed rule, today converters (discrete [1] and integrated [2], [3]) tend to work at switching frequencies less than 100 MHz for about 100 mA output current, and less than 10 MHz for about 1 A output current.

Passive components assuring storage and filtering (i.e. capacitors and inductors) are the bulkiest components of converters. Increasing the operating frequencies allows size reduction of these components. Studies have been carried out for embedding passive components on standard power devices substrates for applications from a few hundreds of milliwatts to a few watts: Printed Circuit Boards (PCB), Low Temperature Co-fired Ceramics (LTCC), on flexible substrates or directly “On-chip” [4]-[8]. For such low power applications, integrating passive components on silicon using microfabrication techniques thus becomes possible. The challenge for integrated passive components on silicon is therefore to allow high power density while keeping low losses at the operating frequency. Integrating inductors on silicon for DC-DC converter applications has focused research efforts for more than 10 years now [9]-[12]. The difficulty remains in producing thick conductors to reduce conductive losses and in integrating in the component a thin-film magnetic material with high resistivity, high saturation magnetization, and high in-plane anisotropy field [13], [14]. Similarly, high density integrated capacitors have been developed with either an optimization of the geometry of the structure: reduced dielectric thickness, enhanced electrodes area [15], [16] or the use of thin-film dielectrics with a high permittivity such as Ta₂O₅ [17], [18], Al₂O₃ [17], HfO₂ [19], ZrO₂ [20], STO [21, 22], BST [23], PZT [24].

Integrating both passive components on the same substrate and thus creating an integrated filter is a way to push the integration a step further while reducing losses through connections and increasing reliability. Considering the range of frequencies mentioned above

and, simultaneously, relatively low power, the task is feasible. For instance, a 45 MHz converter with fully integrated output filter was reported in [6]: the required values for the passive components (6 nF and 11 nH) were reduced by two compared to state-of-the-art converters. More recently, Bergveld and al. [3] have shown the characteristics of an inductive step-down converter operating at 80 MHz with integrated passive components (output LC filter and decoupling capacitor). The capacitors were realized by etching deep pores in the silicon to enhance the electrodes specific area [15], achieving 80 nF/mm² capacitance density and the air-core inductors were realized in the 8 μ m thick copper top metal layer [25].

In this paper, we present the realization of an integrated output LC filter dedicated to future DC-DC micro-converters with the following characteristics: 560 nF 3D capacitor based on a process developed in [26] on top of which is realized a 110 nH spiral micro-inductor based on processes developed in [27] and [28]. The total footprint of the filter is 9 mm². The impedances of the capacitor and inductor of the fabricated filter were measured on a wide range of frequencies. In particular, the interest of a magnetic shield layer is investigated to reduce eddy current losses induced in the capacitor by the micro-inductor. Finally, the full LC filter was tested under real conditions, i.e. with square waveforms typically found in buck DC-DC converter architecture and its losses were analyzed.

II. FABRICATION PROCESS

The LC filter schematic top view and cross-section view are shown in fig. 1. The device area is 3 mm x 3 mm.

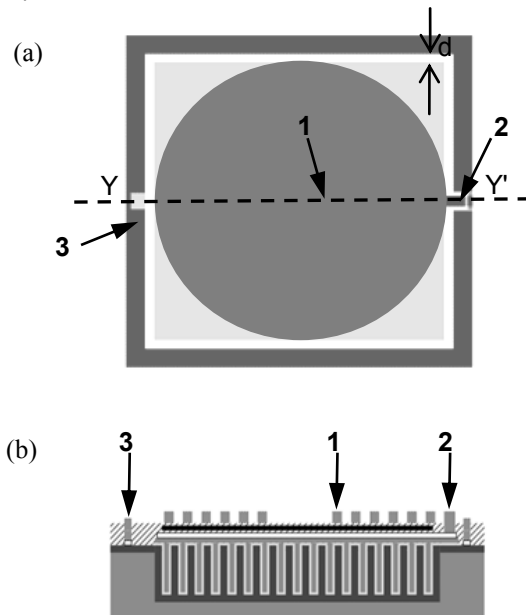


Fig. 1. Schematic (a) top view and (b) cross-section view along (YY') of the integrated LC filter.

The technological steps are reported in fig. 2. From (a) to (e), the 3D capacitor steps are detailed. In step (a), the bottom electrode of the capacitor is formed: high aspect ratio pores are etched by DRIE (Deep Reactive Ion Etching) in the silicon substrate and a phosphorus diffusion step (by POCl_3) is applied. Then, in step (b), a dielectric ($\text{SiO}_2\text{-Si}_3\text{N}_4$ bilayer) is formed by a dry oxidation step and by LPCVD (Low Pressure Chemical Vapor Deposition) of silicon nitride. In step (c), the top electrode of the capacitor is realized: a boron-doped polysilicon ($2 \cdot 10^{20}$ at/cm³) is deposited by LPCVD, with a resistivity of 1.5 m Ω .cm² and patterned.

The dielectric layer is also patterned (step d) and a Ti/Au layer is deposited by sputtering to form ohmic contacts (step e). Steps (f) and (g) are the intermediate steps between the capacitor and the inductor. In step (f), an insulation layer made of SU-8 photoresist is spin coated and openings are provided to connect the inductor to the capacitor. In step (g), a thin layer of CoNiFe [28] is electrodeposited followed by copper electrodeposition to bring contacts to level. Finally, steps (h) to (i) are the steps concerning the spiral inductor. In step (h), an insulation layer made of SU-8 photoresist is spin coated and openings are provided. The spiral shape windings are then electrodeposited with copper through 50 μ m thick photoresist molds (step i). A gold flash (50 nm) is finally realized after copper deposition.

The fabrication steps of the capacitor (from step a to step d) are CMOS compatible and can be accommodated in the process flow of power components, as demonstrated with MOSFETs in [29] for self power supply application. The magnetic shield and the micro-inductor are typical back-end processing steps. Additional steps, required and not shown here, are the deposition of a passivation layer and of an additional metal layer for electrical feed through, and eventually the finishing with solder bumps for flip-chip. In this work, the components are directly cut after step i, i.e. without passivation layer and wire-bonds connect points (1), (2) and (3) to external pads.

III. RESULTS

In this section, the technological developments and the electrical performance of the capacitors and the inductors are analyzed separately before discussing the performance of the LC filter.

A. 3D capacitors

Studies on creating high aspect ratio pores in silicon by DRIE were done on a STS equipment with an ICP (Inductively Coupled Plasma) source for high density plasma [30]. The Bosch process was optimized to obtain

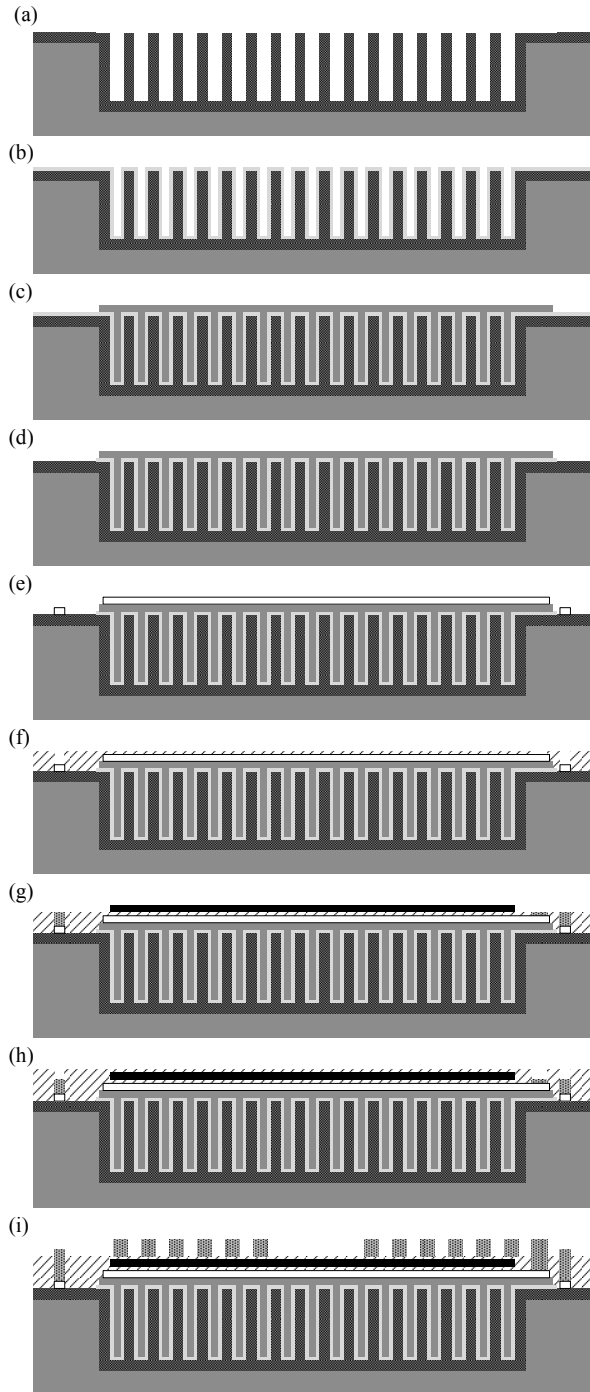


Fig. 2. Schematic (a) DRIE in Si substrate and POCl_3 diffusion; (b) Oxidation (SiO_2) and LPCVD of Si_3N_4 ; (c) LPCVD of boron-doped polysilicon; (d) Dielectric layer patterning; (e) Ti/Au deposition; (f) SU-8 spin coating; (g) CoNiFe electrodeposition and Cu electrodeposition on the contact areas; (h) SU-8 spin coating; (i) Thick Cu electrodeposition.

high density pores network that allows high density capacitance [31]. A photoresist mask was used for the

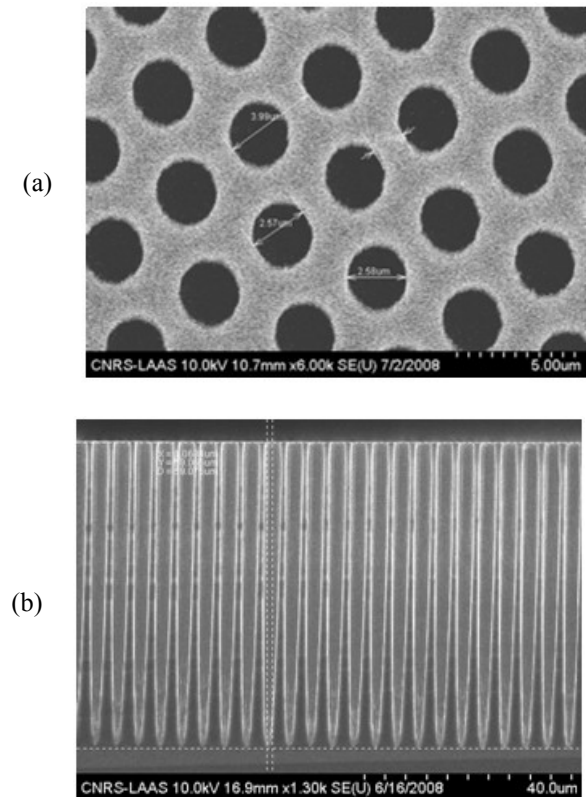


Fig. 3. SEM views of high aspect ratio pore network (a) top view, (b) cross-section: depth is $60 \mu\text{m}$, width is $2.6 \mu\text{m}$.

etching process. Figure 3 shows a SEM (Scanning Electron Microscope) view of a sectioned high aspect ratio pore network. At the end of the process, the width w and the depth h of the pores measured by SEM Hitachi S-4800 were $w=2.6 \mu\text{m}$ and $h=60 \mu\text{m}$ respectively. An additional treatment with TMAH + IPA (Tetramethyl Ammonium Hydroxide + Isopropyl Alcohol) was applied [32] to remove the scalloping and to widen the top of the structures. This treatment is beneficial for subsequently filling the pores with polysilicon without forming void. A phosphorus diffusion step is done at this stage to decrease the access resistance of the capacitor bottom electrode.

N-type silicon substrates with two different initial doping: 10^{12} at/cm^3 and 10^{19} at/cm^3 constituted the bottom electrode of the capacitor. On each of these substrates, the phosphorus diffusion step was applied: POCl_3 at 1500°C for 25 min. As a consequence, a highly doped layer: 10^{21} at/cm^3 is formed at the surface with a depth of $1.5 \mu\text{m}$. This has been checked by Secondary Ion Mass Spectrometry (SIMS).

At the end of step (e) (cf. fig. 2), the fabricated 3D capacitors were measured with impedance analyzer Agilent 4294A connected to RF probe Agilent 42941A. Figure 4 shows the impedance module of 3D capacitors

of different sizes and for different initial substrate doping $N_d = 10^{12}$ at/cm³ and $N_d = 10^{19}$ at/cm³.

The capacitance is 558 nF for 3 mm x 3 mm size capacitor corresponding to 62 nF/mm². The ESR (Equivalent Series Resistance) for an initial doping of 10^{19} at/cm³ is lower than for 10^{12} at/cm³. Therefore, despite the doped region 10^{21} at/cm³ at the surface, the substrate doping underneath still has a large effect over the series resistance. As a result, for instance, the larger capacitor keeps its capacitive behaviour until 3 MHz when the substrate initial doping is 10^{19} at/cm³ as opposed to 800 kHz when the substrate initial doping is 10^{12} at/cm³. To establish with precision the value of the ESR for each case, measurements with Kelvin probes (Microworld PTA-73APT25-50) were conducted. Figure 5 reports the measured ESR for 3 mm x 3mm capacitors. It is 0.17 Ω for the highly doped substrate and 0.37 Ω for the weakly doped substrate corresponding to 0.015 Ω .cm² and 0.03 Ω .cm² respectively. This series resistance is dominated by the access resistance in the doped silicon substrate between the bottom electrode contact (outside ring) and the top electrode contact (polysilicon square), represented in fig. 1 by the distance d . This access resistance could be further reduced by decreasing the corresponding distance or proposing a distributed electrodes configuration as in [33]. Another identified solution could be the use of a metal layer, such as TiN in [22] and [34], for the capacitor electrodes instead of doped silicon.

Other measurements were conducted on the 3D capacitors: C(V) and I(V). C(V) characteristics reveal that there is no capacitance variation when a DC bias is applied. I(V) characteristics measured with a Keithley SC4200 reveal a breakdown voltage of 9 V for these capacitors.

A. Micro-inductor developments

Similarly to 3D capacitors, integrated inductors were first analyzed separately with different configurations. As a 3D capacitor is composed of conductive areas (bottom and top electrodes), it is likely that an inductor directly realized on top of it would develop eddy current losses in the foresaid areas: it was clearly shown in reference [3]. We thus investigated the introduction of a magnetic thin layer acting as a shield to prevent interaction between the inductor and the substrate/capacitor. The influence of the magnetic layer on the inductance and resistance of the micro-inductor was tested on prototypes without capacitor but where the silicon substrate was highly doped (10^{21} at/cm³ at the surface).

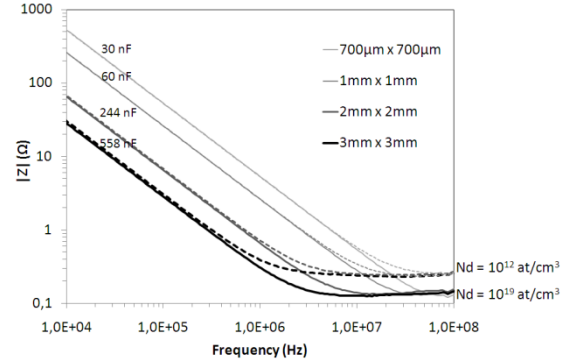


Fig. 4. Measured impedance module versus frequency for different sizes 3D capacitors. Dashed and plain lines correspond to substrate doping of 10^{12} at/cm³ and 10^{19} at/cm³ respectively.

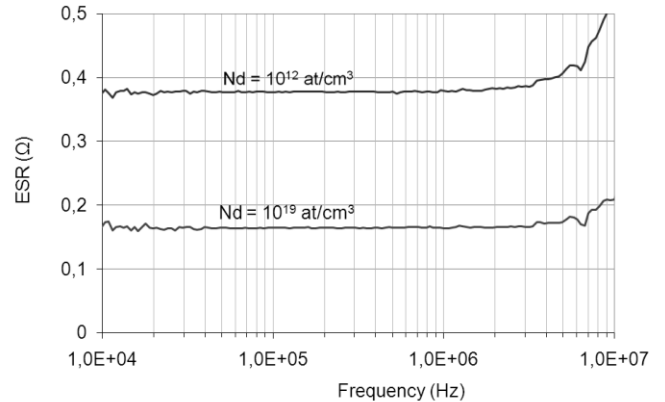


Fig. 5. Equivalent Series Resistance (ESR) of 3D capacitors versus frequency for two types of substrate doping measured with Kelvin probes.

Figure 6 shows pictures of the inductors realized with the magnetic layer (CoNiFe), with and without lamination. The micro-inductors windings were composed of 8 turns, 78 μ m wide, separated by 72 μ m. The electrodeposited copper windings were 51 μ m thick. For comparison purposes, a micro-inductor without magnetic layer was fabricated: in this particular case, the copper windings were 26 μ m thick.

Characterizations of the fabricated integrated inductors were done on an Impedance Analyzer (Agilent 4294A) with an RF probe (Agilent 42941A) from 10 kHz up to 1 MHz and on a network analyzer (Rhode & Schwartz ZVRE.) from 1 MHz up to 4 GHz. Figure 7 shows the equivalent series inductance (ESL) and resistance (ESR) for the following cases: no magnetic layer, a magnetic layer (2 μ m thick), and a laminated magnetic layer.

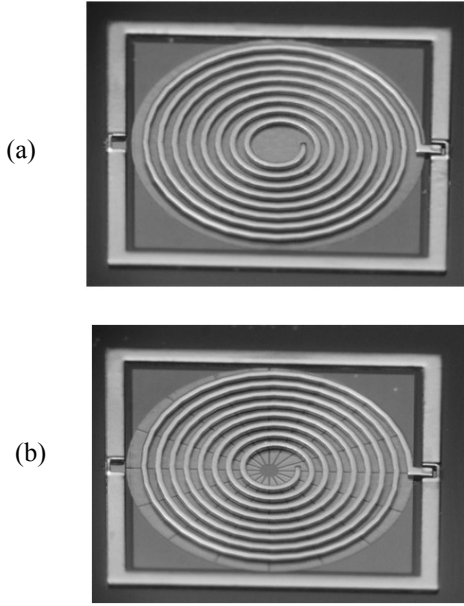


Fig. 6. Optical pictures of micro-inductor with magnetic shield (a) plain; (b) laminated.

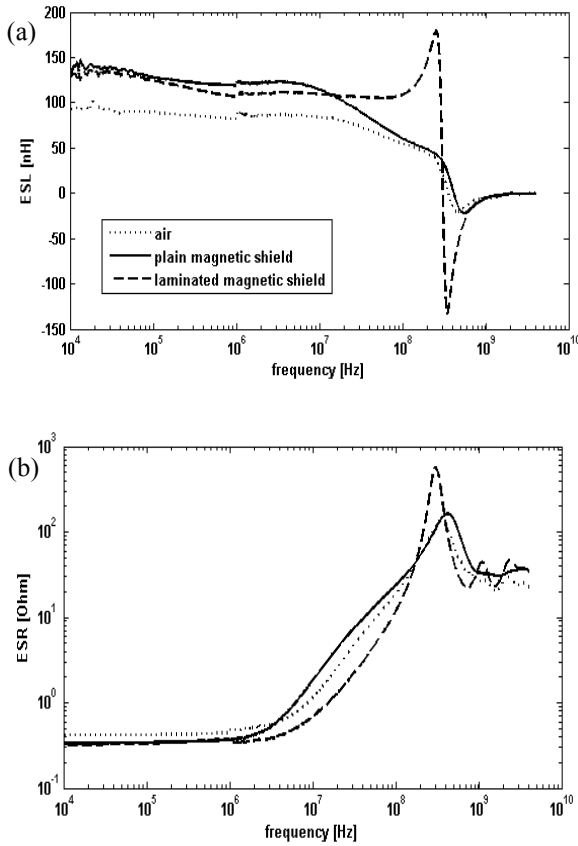


Fig. 7. Equivalent series inductance and resistance measured with impedance analyzer below 1MHz and with network analyzer above 1MHz for three types of inductors: no magnetic layer, a plain magnetic layer, and a laminated magnetic layer.

As expected, the inductance of the air micro-inductor is lower (85 nH) than the inductance of the micro-inductor with magnetic layer underneath (120 nH). On the other hand, the DC resistance for the air micro-inductor is 430 mΩ while for the micro-inductors with magnetic layer, it is 320 mΩ. This is clearly explained by the conductors section which is higher in the latter case.

For AC features, it is clearly shown on the curve corresponding to the air micro-inductor that, above 10 MHz, induced eddy currents in the substrate are responsible for the inductance decrease and the resistance increase. If a magnetic layer is introduced, eddy currents are then occurring in the magnetic layer. As a result, the ESL also decreases and the ESR increases. In the case of laminated magnetic layer, the inductance is not much lower than in the case of non laminated magnetic layer (110 nH versus 120 nH), however, it remains constant up to 110 MHz (just before resonance frequency which occurs at 400 MHz) as opposed to 10 MHz for non laminated layer. The ESR of the inductor with laminated magnetic layer is also lower: 540 mΩ at 10 MHz versus 2.1 Ω at 10 MHz for the plain one.

Saturation characterizations were also conducted on the three types of micro-inductors. The inductance versus DC current at 1 MHz is shown in figure 8. The inductance value is stable for the air-type inductor throughout the whole DC current range. For inductors with magnetic shield, the inductance is reduced by about 10% under 1A. This inductance drop is reasonable and will not impede on the characteristics in a converter. One could not conclude on a difference between the laminated shield and the plain shield. The slightly higher drop in inductance at 1A for the inductor with laminated shield could be attributed to thickness variation in the process as electroplating can be sensitive to geometries.

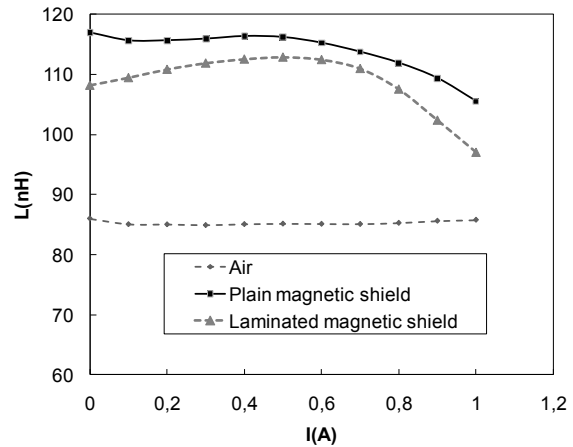


Figure 8. Equivalent series inductance (L) versus DC current measured with impedance analyzer at 1 MHz.

We thus showed that a magnetic layer allows the shielding of eddy currents in the substrate. Moreover, the magnetic shield must be laminated in order to prevent eddy currents from developing in the magnetic layer itself. This solution is efficient and allows reaching high frequencies (up to 110 MHz, self-resonance frequency occurs at 400 MHz) with minimum losses.

B. Integrated LC Filter

Small-signal frequency responses obtained in parts A and B demonstrate that the presented integrated LC filter involves a spiral inductor and a 3D capacitor with high specific values (110 nH and 560 nF for a total surface of 9mm²), and a maximum working frequency beyond 110 MHz in sinusoidal mode.

This new component thus achieves a good trade-off between obtainable electrical features and total footprint. This first prototype was mounted and wire-bonded onto a PCB support and characterized in a test circuit represented in fig. 9 which comprises a switching cell based on the association of discrete components: a low R_{ON} MOSFETs (IRLR3105), a Schottky diode (1N5819). The MOSFET’s gate is controlled by a variable frequency generator followed by a low output impedance driver providing high current peaks. A snubber was added in parallel with the MOSFET to limit the oscillation on V_{DS} due to a parasitic inductance in the switching cell loop. This circuit will allow evaluating the component under real conditions (large signals, non sinusoidal mode).

The circuit operating conditions were chosen to fit as follows: a switching frequency of 5 MHz; a duty cycle of 0.5; an input voltage of 3V and a load resistance of 2.2Ω.

Figure 10 shows measured waveforms: the inductor current I_L, the MOS transistor voltage V_{DS} and the output voltage V_{OUT}. The measured average output voltage is V_{OUT}=0.94 V with a voltage ripple ΔV_{OUT}=460 mV. The current waveform in the inductor I_L shows an average value of about I_{OUT}=445 mA and a ripple ΔI_L=958 mA. One can observe nonlinear tendencies for the current during increasing and decreasing time, both due to the inductor ESR and to the fact that the assumption ΔV_{out} << V_{out} is not satisfied.

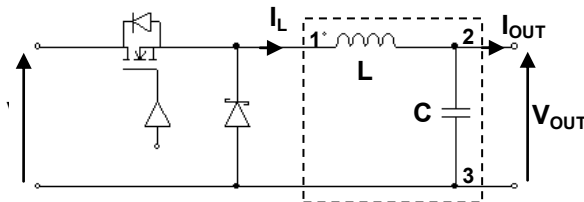


Fig. 9. Test circuit for integrated LC filter characterization. (1), (2) and (3) correspond to the points referenced in Fig. 1a)

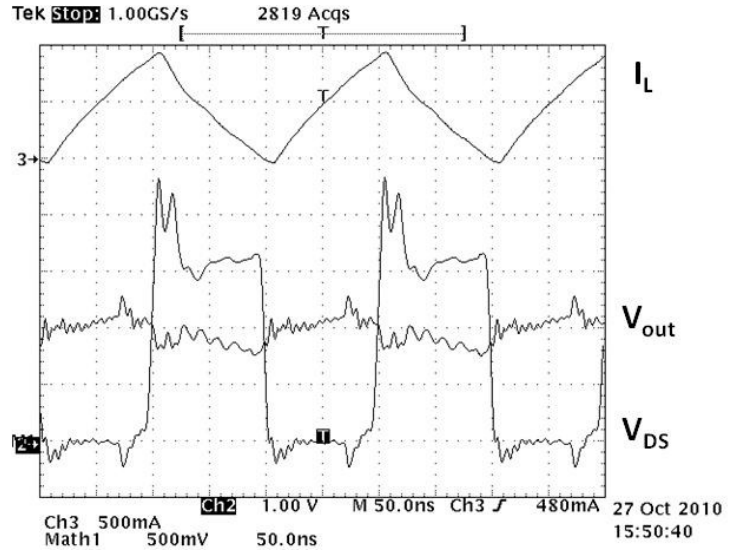


Fig. 10. Inductor current I_L, V_{DS} and output voltage V_{OUT} at 5 MHz .

TABLE I. ELECTRICAL PERFORMANCE OF INTEGRATED FILTER IN THE TEST CIRCUIT AT 5MHZ.

Symbol		Calculated	Measured
Pind	Inductor losses	237 mW	264 mW
Pcapa	Capacitor losses	23 mW	--
Pfilter	Total filter losses	260 mW	--
Pcir	Circuit (other than passives) losses*	243 mW	--
Pin	Input power	891 mW	900 mW
Pout	Output power	388 mW	398 mW
η	Circuit efficiency	43.5 %	45.6%

*Circuit losses take into account the losses in the active component (Diode + MOSFET), the snubber, the input capacitor and the connection wires. The driver consumption was not taken into account.

In order to evaluate the integrated filter performance in a typical power electronics application, circuit simulations (PSIM) were performed using simple components models to validate the measured waveforms. In particular, intrinsic values and disturbances of each component (passive and active) were taken into account as well as all disturbances coming from the connections (wires and bonds). These simulations also allowed calculation of losses that are not directly measurable in the circuit. Table 1 reports the measured and calculated losses corresponding to the different parts of the test circuit.

Circuit efficiency, although quite low (about 45%), shows that despite the use of linear models, there is a good correlation between calculation and measurements. This efficiency is affected by the output filter losses (which represents 52% of total losses) and in particular the losses in the inductor. Despite the technological improvement of the presented solution (thick conductors), the equivalent series resistance of the inductor is still too high for the targeted application and in particular for such current values (I_{OUT} = 445 mA).

Solutions to tackle this problem are to increase further the conductor thickness and to use efficiently a magnetic core that would allow the total conductor length to be reduced (thanks to an inductance increase).

Concerning the capacitor, the estimated losses are lower than the inductor. However, the capacitor ESR has an impact on the voltage output ripple visible in Fig. 9. The measured value $\Delta V_{OUT}=460$ mV is indeed higher than the expected theoretical one that should be 50 mV without parasitic elements of the capacitor branch. The voltage output ripple is both due to ESR of the capacitor (approximately 70% of the total ripple) and the parasitic resistance and inductance of the bondings. Wire-bondings were used in these measurements but this solution should not be adopted for on-chip DC-DC converters where flip-chip BGA packaging is preferred. And as mentioned in section III-A, there are technological solutions to decrease further the intrinsic value of the capacitor ESR.

IV. CONCLUSION

A fully integrated LC output filter for DC-DC application was designed, processed, and characterized. The feasibility of superposing a 3D capacitor and a spiral-type inductor with thick conductors while keeping resistive losses to a minimum at high frequencies was demonstrated. Beyond the challenge of technological steps successions, precise impedance measurement in a wide range of frequencies (10 kHz to 4 GHz) proved the double interest of realizing a thin magnetic material layer between the inductor and the capacitor: the inductor value is modestly increased and the magnetic layer provides an excellent shielding against magnetic coupling with the substrate/capacitor. The component was characterized with waveforms typically found in DC-DC converters and a loss analysis was conducted at 5 MHz. The filter presents absolute values of inductance (110 nH) and capacitance (560 nF) that are well suited for DC-DC converters with switching operation in the range of several MHz. Furthermore, for such values, by stacking the two components, this arrangement offers an advantage in terms of integration.

The equivalent series resistances of both the inductor and the capacitor should be reduced further for achieving high converter efficiency and low output voltage ripple. Various technological solutions were proposed to improve the performance of each passive components but an optimized solution must take into account the specifications of the application where the integrated filter has to be implemented. The choice of the switching frequency, driven by the efficiency target, is then the principal parameter to design the output filter. The passive components optimization should be closely linked to a proper active components design in order to

enable on chip DC-DC converter realization with high performance.

ACKNOWLEDGMENT

Technological developments were conducted in the microfabrication facilities at LAAS-CNRS.

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