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High rate UWB CMOS transceiver chipset for WBAN and biomedical applications

Oswaldo Ramos Sparrow · Rémy Vauché · Nicolas Dehaese · Sylvain Bourdel · Jean Gaubert · Ines Ben amor · Eloi Muhr · Pascal Losco · Olivier Fourquin

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Abstract This work presents a high rate UWB transceiver chipset implemented in a 130 nm CMOS technology for WBAN and biomedical applications in the 3–5 GHz band. The transmitter architecture is based on a double-filter excitation technique that can generate high magnitude pulses and address bipolar modulations such as BPSK. Measurements show that bipolar pulses with a peak-to-peak voltage of 1.9 Vpp for a power consumption of 139 μW @100 kbps can be generated. The receiver is a non-coherent architecture based on LNA followed by an envelope detector. A BER of 10^{-3} is achieved for a 3–5 GHz input peak-to-peak amplitude of 3.4 mVpp which corresponds to a -89.3 dBm sensitivity at 100 kbps. The energy consumption of the receiver and of the transmitter is respectively 0.144 nJ/bit and 196 pJ/bit at 100 Mbps. To improve the budget link of our non-coherent based transceiver a Randomly Alternate OOK signaling is proposed which leads to an estimated communication range of 2.36 m in a free space propagation channel.

Keywords IR-UWB · Ultra wideband CMOS transceiver · WBAN · Non-coherent receiver · Low power

1 Introduction

The interest for biomedical applications and Wireless Body Area Network (WBAN) is growing thanks to the last generation of smart phones which offer a new potentiality for

developing health care monitoring services. The smart phone is a powerful gateway to different networks and can be used to collect data from monitoring devices and to transfer them to health care centers enabling continuous monitoring. In this context, the demand for WBAN systems connecting monitoring devices to a mobile handset is extremely high.

Ultra-Wideband Impulse Radio (IR-UWB) is a promising technology for WBAN and biomedical applications for several reasons. Firstly, the mean radiated power of an IR-UWB signal is low due to the gated nature of the signal. It enables the reduction of the body exposures to the RF energy which is limited by a specific absorption rate (sar) fixed by FCC [1]. The IEEE 802.15.6 standard, which is dedicated to WBAN, recommends the use of IR-UWB, and several biomedical systems have been realized with this technology [2], [3]. Secondly, biomedical applications need moderate data rate communications (around few tens of Mbps) over a short range to ensure services such as video, imaging or high resolution monitoring like electroencephalogram (EEG), or neurological recording. On the receiver side, since only a short communication range is needed (around 1.5 m), the receiver sensitivity requirement is reduced and a non-coherent detection can be used. Non-coherent detectors can support high data rate since they use simplified synchronization schemes and one-bit ADC. Thirdly, since the system should be used with a mobile handset, high energy efficiency is required. IR-UWB is also known for its good energy consumption per bit (few nJ/bit) [4] whereas narrow band systems such as Zigbee exceed 100 nJ/bit [5].

In this paper, we present an IR-UWB transceiver chipset dedicated to WBAN. The system can operate up to a pulse repetition frequency (PRF) of 100 Mpulses per second (Mpps) over a range of 2.36 meters when considering a free space propagation channel. The second part presents some

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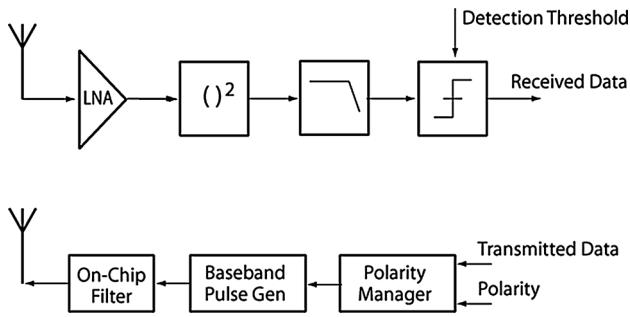


Fig. 1 Transceiver principle

system considerations and especially focuses on the link budget and the system description. The third part presents the design of the transceiver. The transmitter is based on a filter excitation technique and achieves a very high output dynamic. The receiver is a non-coherent envelope detector based on a LNA, a squarer and a filter. The fourth part presents measurement results and compares the performances with previous published works.

2 System consideration

2.1 Architecture

The proposed transceiver is presented in Fig. 1. Since the receiver is based on an envelope detector, several choices have been made to reduce the impact of its low sensitivity and improve the link budget. Firstly, the transmitter is based on a filter excitation technique which is well suited for generating high output dynamic with a low power consumption [6]. Such architectures achieve high energy efficiency and a large output dynamic which benefit the budget link. Secondly, the low band of the FCC spectrum is planned to be used in order to reduce the propagation loss. Six decibels are saved into the budget link by using a center frequency of 4 GHz instead of the 8 GHz of the FCC high frequency band. The targeted -3 dB bandwidth (BW_{-3dB}) is 1.33 GHz, which corresponds to the fourth channel of the IEEE 802.15.4a standard.

The receiver is non-coherent and is based on a LNA followed by an envelope detector (pseudo energy detector). This topology is simple and does not need to be synchronized with the received signal unlike conventional energy detectors based on integrators. The envelope detector is followed by a comparator with a variable threshold.

2.2 Modulation scheme

In the case of non-coherent receivers, OOK signaling is often used since such topology cannot manage the polarity of the received signal. However, OOK modulation produces discrete spectrum due to the mean value of the sequence which is not

null. As shown in (1), where $P^+(f)$ is the unilateral spectrum of the emitted pulse and, μ_d and σ_d , are respectively the mean and the variance of the emitted sequence ($\{d_k\}$), the magnitude of the discrete spectrum grows with the square of the PRF ($D_s = 1/T_s$) which is a major drawback for high rate transmission because the FCC limits the maximum value of the mean power spectral density (noted $PSD_S^+(f_M)$ in the case of an unilateral representation).

$$PSD_S^+(f) = \frac{\sigma_d^2}{T_s} |P^+(f)|^2 + \frac{\mu_d^2}{T_s^2} |P^+(f)|^2 \sum_{i=-\infty}^{\infty} \delta\left(f - \frac{i}{T_s}\right). \quad (1)$$

From (1) and for a given pulse waveform, we can evaluate the maximum pulse energy (E_{P-MAX}) allowed by FCC for different bit rates and different modulation schemes. From (1), $PSD_S^+(f_M)$ can be derived as follows:

$$PSD_S^+(f_M) = \frac{1}{T_s} \frac{|P^+(f_M)|^2}{Z_L} \max\left[RBW\sigma_d^2; \frac{\mu_d^2}{T_s}\right], \quad (2)$$

where $P(f_M)$ is the value of the pulse spectrum evaluated at the frequency for which the PSD is maximum (f_M), Z_L is the antenna impedance and RBW is the resolution bandwidth of the spectrum analyzer used for the PSD measurement which is set to 1 MHz by FCC. If we consider a Gaussian pulse given by (3) which is well suited to represent a wide pulse ($BW_{-3dB} > 1$ GHz), the pulse energy can be expressed by (4).

$$p(t) = A \exp(-at^2) \cos(2\pi f_M t) \\ P^+(f) = A \sqrt{\frac{\pi}{2a}} \exp\left(-\frac{[2\pi(f - f_M)]^2}{4a}\right), \quad (3)$$

$$E_P = \frac{A^2}{2Z_L} \sqrt{\frac{\pi}{2a}} \left[1 + \exp\left(-\frac{|4\pi f_M|^2}{8a}\right)\right], \quad (4)$$

$$\text{with } a = \frac{\pi^2 BW_{-XdB}^2}{2 \ln(10^{XdB/10})}, \quad (5)$$

where BW_{-XdB} is the $-XdB$ bandwidth of the pulse. We can express, as a function of the PRF, the maximal value $A_{MAXmean}$ of the pulse and its energy $E_{P-MAXmean}$ that comply with the mean PSD limitation imposed by FCC (i.e. $PSD_S^+(f_M) < -41.3$ dBm/MHz) as shown in (6) and (7):

$$A_{MAXmean} = \sqrt{\frac{2 \cdot PSD_S^+(f_M) T_s Z_L a}{\pi \max\left[RBW\sigma_d^2; \frac{\mu_d^2}{T_s}\right]}}, \quad (6)$$

$$E_{P-MAXmean} = \frac{2 T_s PSD_S^+(f_M)}{\max\left[RBW\sigma_d^2; \frac{\mu_d^2}{T_s}\right]} \sqrt{\frac{a}{8\pi}} \left[1 + e^{-\frac{|4\pi f_M|^2}{8a}}\right]. \quad (7)$$

Moreover, FCC also limits the peak Power Spectral Density which is defined as the peak power measured in a

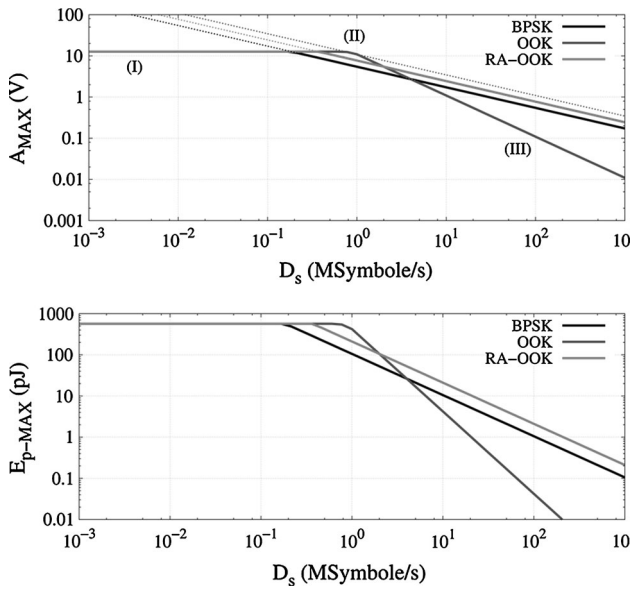


Fig. 2 Maximum pulse magnitude and pulse energy allowed by FCC for a Gaussian pulse ($BW_{-3dB} = 1.33$ GHz)

50 MHz bandwidth (RBW_{50MHz}) at f_M and which can be expressed as follows [6]:

$$P_{pk} = \frac{2}{Z_L} |P^+(f_M)|^2 \cdot RBW_{50MHz}^2 \quad (8)$$

From (3), (4) and (8) we can compute the maximal magnitude ($A_{MAXpeak}$) and the maximal energy ($E_{P-MAXpeak}$) which comply with the peak power limitation ($P_{pk} < 0$ dBm). Then, $A_{MAXpeak}$ and $E_{P-MAXpeak}$ can be respectively expressed by:

$$A_{MAXpeak} = \sqrt{\frac{P_{pk} Z_L a}{\pi \cdot RBW_{50MHz}^2}} \quad (9)$$

$$E_{P-MAXpeak} = \frac{P_{pk}}{RBW_{50MHz}^2} \sqrt{\frac{a}{8\pi}} \left[1 + e^{-\frac{4\pi f_M^2}{8a}} \right] \quad (10)$$

In Fig. 2, A_{MAX} (respectively E_{P_MAX}) which is the minimum between $A_{MAXmean}$ and $A_{MAXpeak}$ (respectively $E_{P-MAXmean}$ and $E_{P-MAXpeak}$) is plotted for several modulations.

Thus, A_{MAX} (respectively E_{P_MAX}) is equal to $A_{MAXpeak}$ (respectively $E_{P-MAXpeak}$) for low rates, where it is constant, and A_{MAX} (respectively E_{P_MAX}) is given by $A_{MAXmean}$ (respectively $E_{P-MAXmean}$) for high rates, where it is dependent on the symbol rate. Then, three areas can be distinguished in Fig. 2. Area (I) is defined by the peak power imposed by FCC and for which A_{MAX} is given by $A_{MAXpeak}$. Area (II) is defined by the continuous part of the mean PSD which grows with D_s and for which A_{MAX} is given by $A_{MAXmean}$. Area (III) is defined by the discrete part of the mean PSD which grows with the square of D_s and for which A_{MAX} is also given by $A_{MAXmean}$. The area (III) exists only for

OOK since it is the only modulation which has a discrete spectrum ($\mu_d \neq 0$). Moreover, the area (II) does not exist for OOK modulation because the peak power limitation occurs for a bit rate equal to 1.2Mbs^{-1} which is higher than the bit rate for which the discrete spectrum is lower than the continuous one. The Fig. 2 can be used to choose the modulation scheme and also to make the link budget.

As said, at low rates the energy is limited by the peak power and does not depend on the bit rate. At high rates, the maximal allowed energy drops with the bit rate. Thus, for rates greater than a few Mpps, a bipolar modulation is needed to avoid the discrete spectrum and to maximize the emitted pulse energy. Since a non-coherent receiver is unable to demodulate a BPSK modulation, the adopted modulation scheme is based on a Randomly Alternate OOK (RA-OOK) signaling which is a conventional OOK modulation scheme for which the polarity of the emitted pulses is randomly alternated. For a RA-OOK, μ_d is null and σ_d^2 is equal to $1/2$ which finally increases the maximum possible bit rate by a factor equal to 2 for the same pulse energy compared to a conventional BPSK. Moreover, RA-OOK receivers do not need to recover the polarity of the pulse to operate unlike BPSK receivers.

2.3 Power consumption

Since the UWB signal is a gated waveform, power gating techniques can be implemented to reduce power consumption especially by turning off the transceiver between two consecutive pulses. On the transmitter side, power gating is easy to implement since no clock recovery is needed. On the receiver side it becomes a difficult issue. To achieve efficient power gating, the time needed to turn on (T_{on}) and to turn off (T_{off}) the receiver must be very short. For rates around a few tens of Mbps, T_{on} and T_{off} must be a few ns and complex topologies are needed to reduce the settling time of the DC operating point [7]. Moreover, the precision of the clock and data recovery (CDR) system, used to manage the power gating, must be very high. To reduce these constraints, bursts can be used. To avoid changes in the PSD, the mean PRF must be constant for 1 ms which is the spectrum analyzer sweep time imposed by FCC to measure the PSD. The maximal burst duration is then given by:

$$T_{BURST} = \frac{PRF_{MEAN}}{PRF_{BURST}} \cdot 10^{-3} = \eta_{BURST} \cdot 10^{-3}, \quad (11)$$

and the receiver can be turned off during:

$$T_{IDLE} = 10^{-3} - T_{BURST}. \quad (12)$$

η_{BURST} gives the ideal power reduction factor which is not very sensitive to T_{on} and T_{off} since the T_{IDLE} is in the order of 1 ms.

Table 1 Preliminary link budget

PRF_{MEAN} (MHz)	30
PSD_{MAX} (dBm/MHz)	-41.27
BW_{-3dB} (GHz)	1.33
E_{p-MAX} (pJ)	3.5
A_{MAX} (V) ^a	1
G_{TX} (dB)	3
G_{RX} (dB)	3
M_{dB} (dB)	6
A_{RX} (mV) ^a	4
E_{RX} (pJ)	56×10^{-6}
$P_{RX@30}$ Mpps (dBm)	-57.8
$P_{RX@100}$ kpps (dBm)	-82.5
d (m)	1.5

^a On a 50 Ω impedance

2.4 Preliminary link budget

The power received at the receiver (P_{RX}) is given by:

$$P_{RX} = P_{TX} + 2G_a - L_{dB} - M_{dB}, \quad (13)$$

where P_{TX} is the emitted power, G_a is the gain of the transmitter and emitter antennas, L_{dB} is the propagation loss and M_{dB} is a fade margin. For a given energy or a given pulse amplitude, the signal power depends on the bit rate. Since the energy detected by a non-coherent receiver does not depend on the bit rate, a voltage link budget gives the communication range for any bit rate as follows:

$$d = \frac{A_{TX} \cdot G_a \cdot \lambda}{A_{RX} \cdot 4 \cdot \pi \cdot \sqrt{M}}. \quad (14)$$

where λ is the signal wavelength and A_{TX} and A_{RX} are respectively the amplitudes at the transmitter output and at the receiver input. To ensure video transmission and high resolution monitoring the targeted mean PRF is 30 Mpps. For such rates, E_{p-MAX} is limited by the mean PSD and is given by (7). For a Gaussian pulse with a 1.33 GHz bandwidth $E_{p-MAX} = 3.5$ pJ and $A_{MAX} = 1$ V if a RA-OOK is used. When considering a simple free-space-propagation model for the propagation loss and if the fade margin is set to 6 dB (taken equal to the cumulative gain of the antennas $2 \cdot G_a$), the communication range is 1.5 meters for a voltage sensitivity of 4 mV which corresponds to a received energy of 56×10^{-18} J. The main values of the preliminary link budget are given in Table 1.

3 Transmitter design

The proposed transmitter, based on the excitation of two identical band-pass filters [6, 8], is presented in Fig. 3. Its

architecture is chosen to achieve two objectives. The first one is the generation of high energy pulses and the second one is the generation of bipolar pulses in order to be able to communicate with BPSK or RA-OOK modulations. The pulses which are generated on $s(t)$ are obtained by subtracting the two shifted filter outputs called $s_1(t)$ and $s_2(t)$.

As shown in Fig. 3, the transmitter design can also be cut into two parts. The first part is composed of two current driven filters which allow bipolar high energy pulses to be generated on a 100 Ω differential load. Frequency responses of both filters are sized in order to make pulses compliant with the fourth channel of the IEEE 802.15.4a standard which has a -3 dB (-10 dB) bandwidth equal to 1.33 GHz (1.73 GHz) and centered at 3996.6 MHz. The second part of the proposed pulse generator consists in a double baseband pulse generator which drives the double filter by generating shifted synchronized baseband pulses thanks to the bipolar pulse manager.

3.1 Double filter design

The double filter is based on two classical Bessel-Thompson filters. This filter type is especially interesting for IR-UWB pulse generation since it generates short pulses with regard to filter bandwidth. The filter order is chosen to be as low as possible to match the targeted channel in order to keep the number of inductors, the transmitter die area and the losses low. However, the double filter has to be cautiously designed in order to reduce losses with the help of short interconnections between LC resonators. Moreover, parasitic capacitances of each inductor must be taken into account to maintain a compliant frequency response with the fourth IEEE 802.15.4a channel.

With regard to the different filter topologies which respect to the previous points, the proposed one offers advantages in terms of pulse dynamic and parasitic element compensation. As for the first advantage, the first resonator allows the filter to be driven in current mode which gives high peak to peak voltage pulses but also requires large MOS transistors which are adjusted to keep the energy efficiency of the filters high. Then, the double filter is based on two class C amplifiers built with Low Leakage MOS transistors in order to minimize the leakage consumption which degrades the power consumption especially when no pulses are generated. For the same reasons, the C_s capacitor achieves a DC isolation which avoids high power consumption since the MOS transistor is biased thanks to L_1 and L_2 with L_1 equals to L_2 . Moreover, it is important to highlight that at a frequency around 4 GHz the quality factor of the equivalent inductor achieved by L_1 in parallel with L_2 is much higher than the one of the inductor (L) given by the filter synthesis ($L = L_1 L_2 / (L_1 + L_2) = L_1 / 2$). This results in a higher output dynamic at the cost of an increased die area.

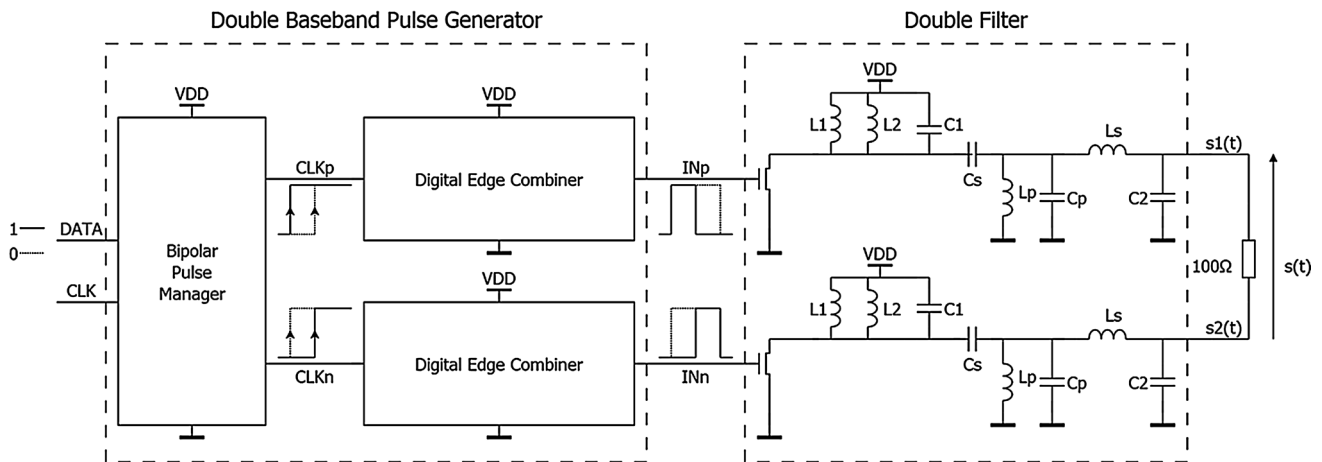


Fig. 3 Principle of the proposed pulse generator

Concerning the second advantage, C_1 and C_2 can respectively compensate the C_{DS} of the large MOS transistor and the pad capacitance and, C_1 , C_2 , and C_p can be reduced in order to compensate L_1 , L_p , and L_s parasitic capacitors.

3.2 Double baseband pulse generator design

The double baseband pulse generator can be divided into three parts. The first part is a bipolar pulse manager which generates shifted rising edges where INn is in late ahead INp when $DATA$ is equal to 1, and conversely when $DATA$ is equal to 0. The other two consist of two digital edge combiners which transform a rising edge in a baseband pulse with a duration of $1/(2f_M)$ where f_M is the frequency where the PSD is at its maximum value. Then, the peak to peak pulse voltage is also maximized.

The bipolar pulse manager which enables bipolar modulations like BPSK or RA-OOK but also OOK to be used, generates two rising edges delayed with a duration equal to $1/(2f_M)$ from a CLK rising edge in order to maximize the pulse amplitude on $s(t)$ after subtraction of $s_1(t)$ and $s_2(t)$ as shown in Fig. 4. $CLKp$ is also in advance of $1/(2f_M)$ in front of $CLKn$ when $DATA$ is equal to '1', and $CLKn$ is in advance of $1/(2f_M)$ regarding to $CLKp$ when $DATA$ is equal to '0'.

Next, the two edge combiners transform rising edges from $CLKp$ and $CLKn$ into baseband pulses with a duration of $1/(2f_M)$ thanks to delay cells and a fast CMOS logic gate [9]. To match the small transistors used in the logic gate with the large ones used in the double filter, a CMOS inverter string is connected between the two.

Finally, bipolar pulses with a high peak to peak voltage are obtained by combining the two responses $s_1(t)$ and $s_2(t)$ of the double filter around the antenna which have a phase shift of 180° as shown in Fig. 4. It is also possible to use a

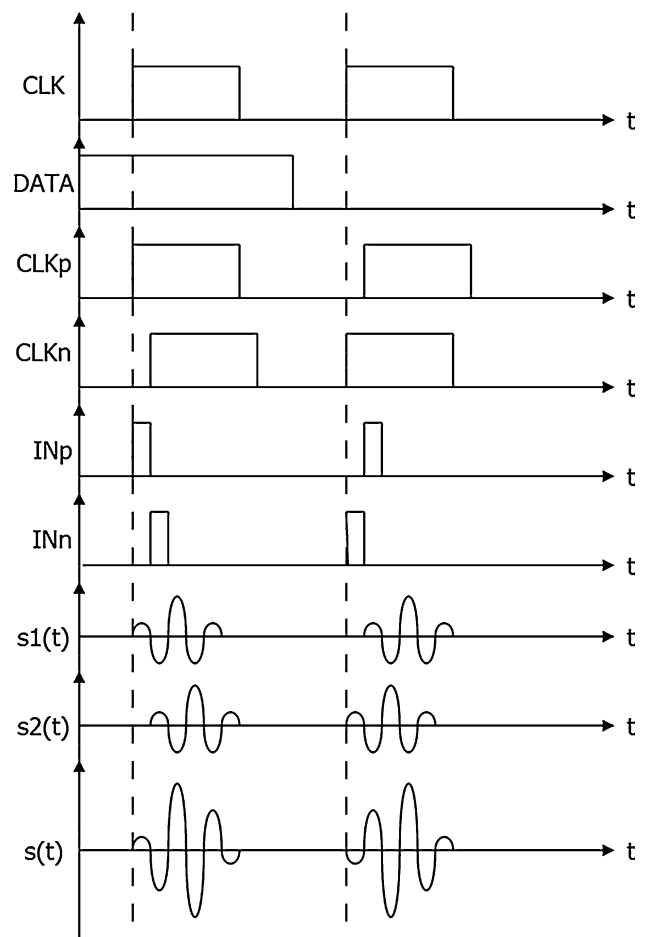


Fig. 4 Main signals of the presented pulse generator in time domain

RA-OOK modulation by driving $DATA$ with a randomized binary sequence and CLK with a rising edge when a '1' has to be sent. OOK is also obtained by setting $DATA$ at a given constant logic state. To use BPSK modulations,

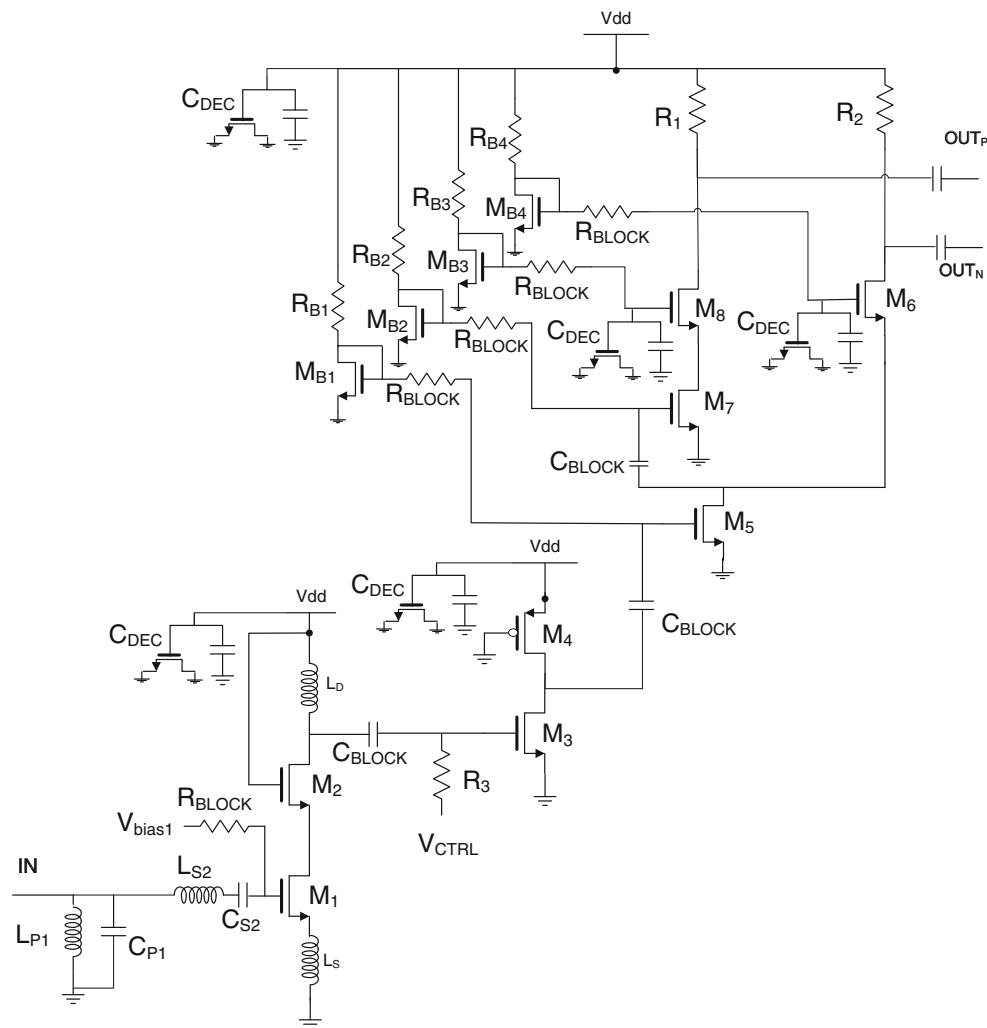


Fig. 5 High gain single ended to differential ended LNA architecture

DATA have to be controlled by the sent binary sequence and *CLK*, by a rising edge for each bit duration.

4 Receiver design

4.1 LNA

As shown in the receiver architecture depicted in Fig. 1, the LNA is inserted between the antenna and the squarer. Because antennas are usually single ended while squarer circuits have generally a differential input [10], the LNA must perform a single to differential conversion. In a low-cost perspective, the use of an off chip filter should be avoided. So a LNA with a bandpass response reduces both parasitic signals and equivalent noise bandwidth before the squarer input. Finally, since conversion gain of squarer functions is typically very low when input signal magnitude is small, an LNA with a large voltage gain is useful to

ensure that the output signal of the squarer exceeds the noise floor of the stages located downstream.

The LNA architecture is depicted in Fig. 5. The LNA includes three stages. The LC matched input stage (M_1 , M_2) achieves a bandpass response in the 3–5 GHz bandwidth [11]. The active load second stage (M_3 , M_4) provides an additional gain controlled by the voltage V_{CTRL} . The third stage (M_5 – M_8) achieves the single ended to differential ended conversion and provides some additional gain. The LNA sizing process to minimize the noise figure and to maximize the voltage gain is presented in [11]. For such a high gain amplifier at high frequency, signal integrity and stability are important issues. The power supply pads (V_{DD}) are decoupled by using several MIM and MOS capacitors (C_{DEC} in Fig 5) in order to get a large on chip capacitor value (a few hundred pF) leading to low return path ground impedance at high frequencies.

The simulated LNA voltage gain and noise figure versus frequency obtained in the high gain mode are given in

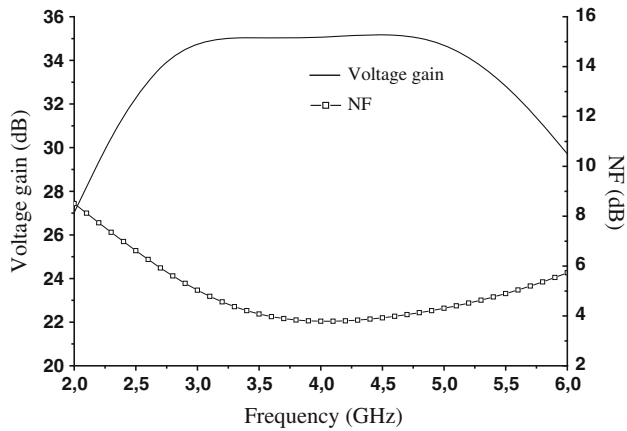


Fig. 6 Simulated LNA voltage gain and noise figure

Fig. 6. The noise figure ranges from 3.8 to 5 dB in the 3–5 GHz bandwidth. The maximum voltage gain is 35.5 dB with a gain ripple of 0.4 dB in the 3–5 GHz bandwidth. The simulated LNA transient response to a 3–5 GHz bandwidth incoming UWB pulse, given in Fig. 7, shows low distortion on the output pulse. The ratio between the output pulse peak magnitude and the incoming pulse peak magnitude is 58 in good concordance with the LNA AC response.

4.2 Detector

The architecture of the non-coherent envelope detector is composed of a squarer, an amplifier and a decision stage, as shown in Fig. 8. The envelope detection process in the frequency domain is also illustrated in this figure. The principle of the proposed detector is, first, to extract the envelope of the input UWB pulse. To do that, the 3–5 GHz UWB pulse V_{SQin} is squared to transpose it around 0 Hz. The pulse envelope, which occupies the frequency band from 0 to 1 GHz, is then filtered and amplified. As the pulse envelope is the image of the transmitted information, its amplitude can then be used to decide if a bit has been transmitted or not. For that, a decision stage based on a comparator scheme is used.

4.2.1 Squarer

The squarer circuit is based on the self-mixer architecture shown in Fig. 9.

The principle is to use two coupled PMOS transistors (M_1 and M_2), biased in the sub threshold region, in order to generate a current I_{SQ} whose amplitude is proportional to the squared amplitude of the input signal $V_{SQin} = V_{SQimp} \cdot V_{SQin}$ while minimizing the squarer power consumption. In the proposed schematic, PMOS devices M_1 and M_2 are loaded

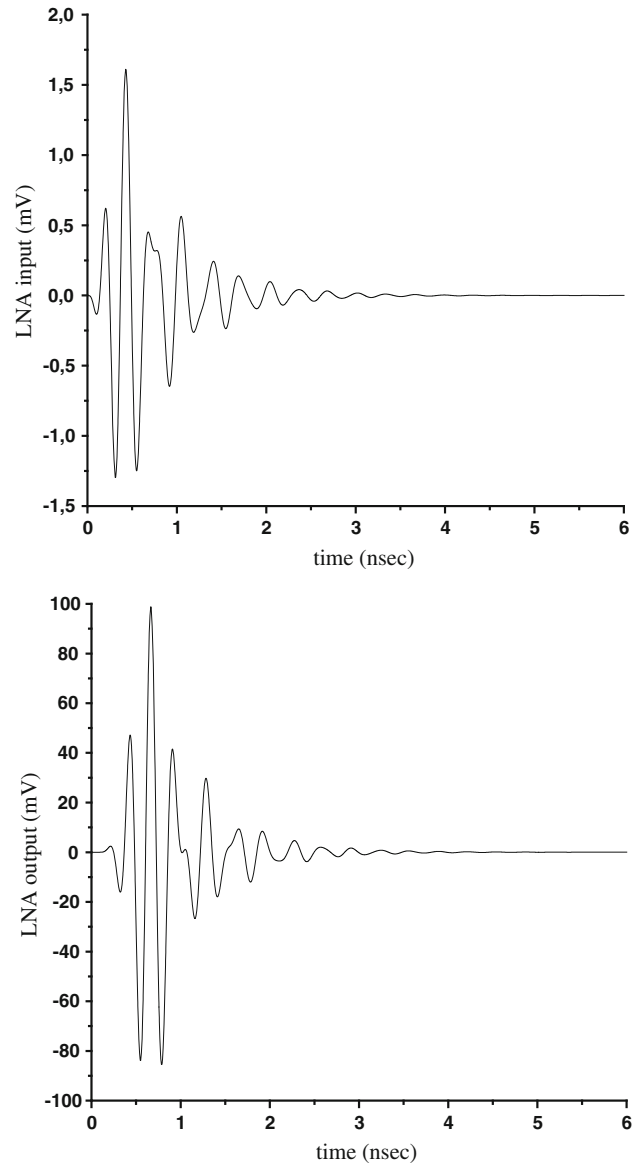


Fig. 7 Simulated transient LNA response

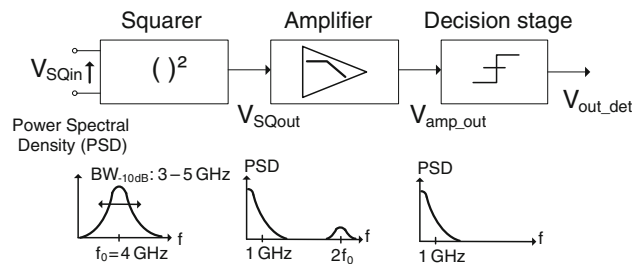


Fig. 8 Non coherent receiver architecture

by a diode-connected PMOS transistor (M_3). To operate in the sub-threshold region, the gate-source voltages of M_1 and M_2 are biased at $V_{gs0M1} = V_{gs0M2} = V_{gs0} = -0.2$ V

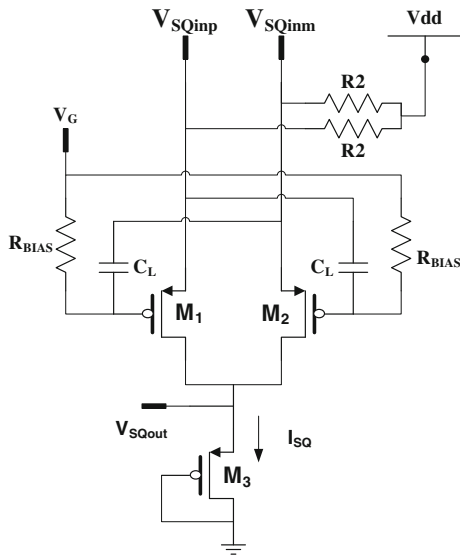


Fig. 9 Squarer circuit

(lower in absolute value to the threshold voltage $V_{th} \sim -0.35$ V). In sub-threshold region, the I_{ds} current of a MOS transistor is a strongly non-linear function of V_{gs} and can be written as [12]:

$$I_{ds} = I_S \cdot e^{\left(\frac{V_{gs} - V_{th}}{nU_T}\right)} \text{ with } I_S = \mu_0 C_{ox} \frac{W}{L} (n - 1) U_T^2. \quad (15)$$

where n is the sub-threshold slope factor and $U_T \sim 25$ mV@T = 290 K. Writing the gate-sources voltages of M1 and M2 as:

$$V_{gsM1} = V_{gs0} + v_{gs1} \text{ and } V_{gsM2} = V_{gs0} + v_{gs2}. \quad (16)$$

Considering a second order Taylor series expansion of (15) and combining the output current of M1 and M2, this leads to the following expression for I_{SQ} :

$$I_{SQ} = I_{ds0} \cdot \left[2 + \frac{v_{gs1} + v_{gs2}}{n \cdot U_t} + \frac{v_{gs1}^2 + v_{gs2}^2}{2 \cdot (n \cdot U_t)^2} \right] \quad (17)$$

with $I_{ds0} = I_S \cdot \exp\left(\frac{V_{gs0} - V_{th}}{n \cdot U_t}\right),$

with $v_{gs2} = -v_{gs1} = V_{SQin}$, I_{SQ} can be written as a function of the squared input signal V_{SQin}^2 :

$$I_{SQ} = I_{ds0} \cdot \left[2 + \frac{V_{SQin}^2}{(n \cdot U_t)^2} \right]. \quad (18)$$

The signal V_{SQout} at the squarer output can then be expressed as:

$$V_{SQout} = I_{SQ} \cdot \frac{1}{g_{dsM1} + g_{dsM2} + g_{mM3}}, \quad (19)$$

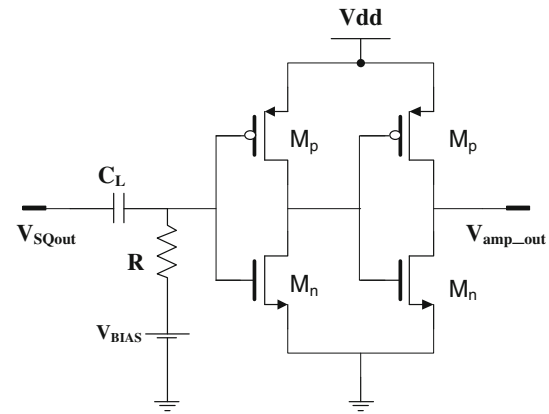


Fig. 10 Amplifier circuit

g_{dsM1} , g_{dsM2} are respectively the output conductance of M1 and M2 and g_{mM3} the transconductance of M3. Following (19), M3 is sized by choosing a low ratio ($W = 0.15 \mu\text{m}/L = 0.13 \mu\text{m}$) to increase V_{SQout} . The size (W/L) of M1 and M2 is set thanks to simulations ($10 \mu\text{m}/0.2 \mu\text{m}$) in order to maximize the output voltage V_{SQout} .

4.2.2 Amplifier and decision stage circuits

It is worth noting that, as the input UWB pulse has been squared, its amplitude is very low. The pulse has then to be first amplified to be correctly detected by the decision stage. Accordingly, two CMOS inverters (cf Fig. 10), used as voltage amplifiers, are chosen since they offer an interesting trade-off between a high gain and a low power consumption.

The inverters are biased and sized so that both M_n and M_p operate in the saturation region ($V_{BIAS} \sim 0.6$ V) in order to maximize the voltage gain in the 0–1 GHz band. A voltage gain of 20 dB for a power consumption of 98.6 μW is reached for the proposed amplifier. The biasing voltage V_{BIAS} is set externally so that it can be tuned to counter-balance the influence of process, voltage and temperature (PVT) variation.

For the decision stage, the principle is to compare the amplitude of the UWB pulse envelope (V_{amp_out}) with a decision threshold S_d . If the pulse envelope is lower than the threshold, no pulse is detected and the output signal remains at 0 V; if the pulse envelope crosses the threshold, a pulse is detected and the output signal goes to 1 (Vdd) long enough to enable the post-detection circuits to properly process the signal. The choice of the threshold voltage must then be made as a trade-off between the false alarm rate, due to the influence of noise, and the non-detection rate and so the receiver sensitivity. The decision stage circuit is also built from CMOS inverters as shown in Fig. 11.

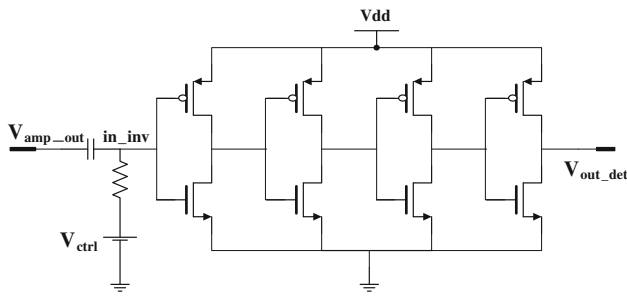


Fig. 11 Decision stage circuit

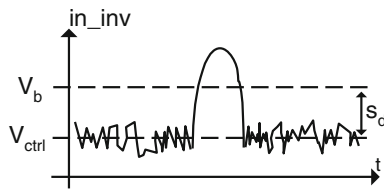


Fig. 12 Definition of the decision threshold

The gate of the first inverter is externally biased around a voltage V_{ctrl} so that the noise amplitude at its input remains below the switching threshold V_b of the inverter, as illustrated in Fig. 12. The decision threshold is then defined as:

$$S_d = V_b - V_{ctrl}. \quad (20)$$

A set of three other CMOS inverters follows the first one in order to generate a properly shaped logic signal V_{out_det} .

4.2.3 Simulation results

The processing of 3–5 GHz UWB pulses by the non-coherent detector is illustrated in Fig. 13.

In the given example, a sequence ‘101’ is sent into the detector. The 3–5 GHz pulse amplitude is set at 44 mV (peak-to-peak), which corresponds to the minimum detectable level in simulation for the proposed detector. At the output of the squarer function, the pulses (V_{SQ_out} in Fig. 13) have been nearly squared (not strictly due to the bandwidth limitation of the squarer). The pulse envelope clearly appears (amplitude of 2.5 mV) and can be used for the decision step. The envelope is then amplified to reach an amplitude of ~ 25 mV before the decision stage (V_{amp_out}). The decision threshold is set through V_{ctrl} in order to minimize the false alarm rate in an additive white Gaussian noise channel (AWGN). The correctly recovered sequence V_{out_det} is shown in Fig. 13 for $V_{ctrl} = 0.595$ V. The maximum achievable PRF for the receiver is around 100 Mpps.

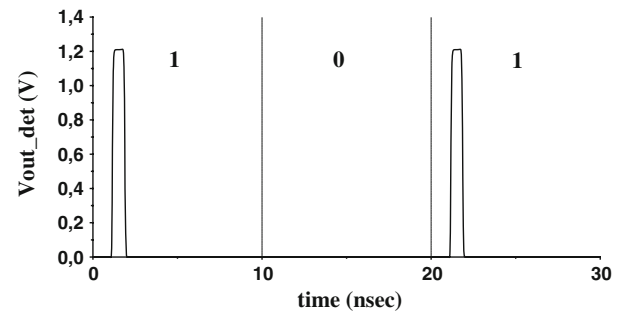
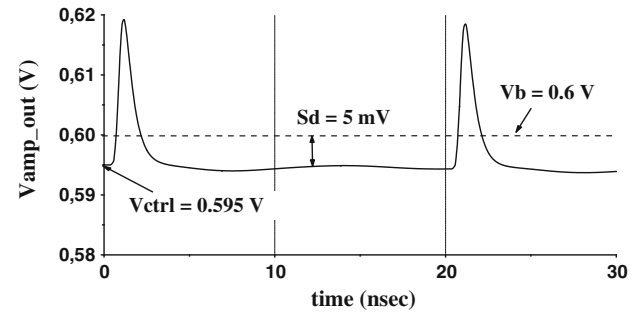
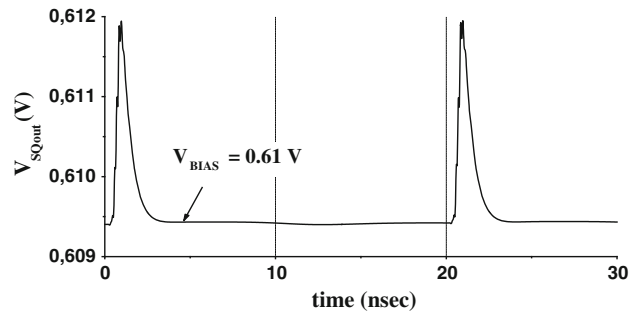
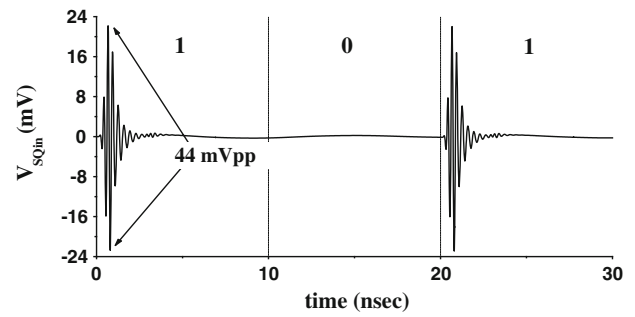


Fig. 13 Processing of a sequence ‘101’ by the non-coherent detector

5 Measurement results

The presented transceiver has been realized in a 130 nm CMOS technology from STMicroelectronics.

5.1 Transmitter

The die area of the proposed pulse generator is about 2.9 mm² due to the integration of a double filter and the use of inductors as shown in Fig. 14.

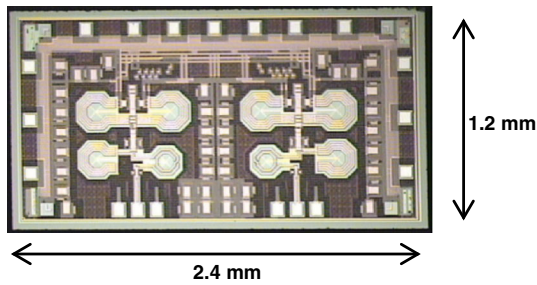


Fig. 14 Chip micrograph of the proposed pulse generator

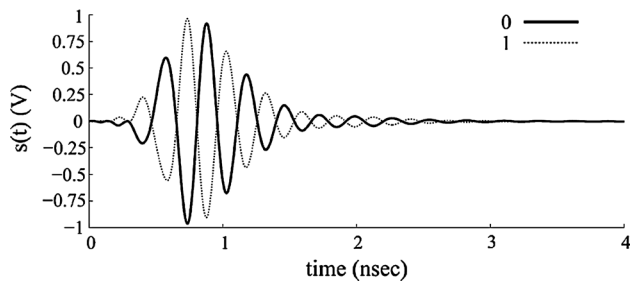


Fig. 15 Measured responses of the presented pulse generator in time domain for DATA equal to '1' and '0'

The measured transient responses of the pulse generator are shown in Fig. 15 and demonstrate the pulse generator capability for bipolar modulations such as BPSK and RA-OOK. The measured peak to peak voltage of obtained pulses is about 1.9 Vpp on a 100 Ω differential load which gives an emitted pulse energy E_p of 1.78 pJ. Regarding the power consumption, the mean power P_C consumed by the pulse generator can be expressed as a function of the PRF as follows [8]:

$$P_C(PR F) = E_{AC} \cdot PR F + P_{DC}. \quad (21)$$

where P_{DC} is the constant DC power when no pulses are emitted and E_{AC} is the active energy added while a pulse is generated. By measuring the consumed current by the pulse generator, it is possible to match its power consumption with the expression given in (21). This leads to a P_{DC} equal to 120 μW, an E_{AC} equal to 196pJ/pulse (for a RA-OOK modulation), and a P_C equal to 139 μW@100 kpps and 19.7 mW@100 Mpps for a supply voltage of 1.2 V. Finally, the transmitter keeps its output dynamic until 50 Mpps, as shown in Fig. 16, and allows bursts to be emitted at this rate.

5.2 Receiver

The chip micrograph of the IR-UWB non-coherent receiver (LNA and detector) is shown in Fig. 17. The die area is 1.43 mm² including the pads.

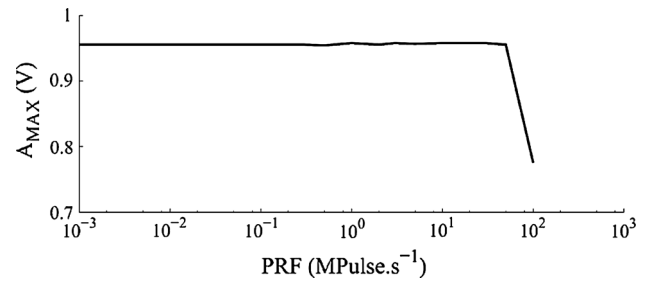


Fig. 16 Measured peak voltage at the output of the transmitter versus the pulse repetition frequency

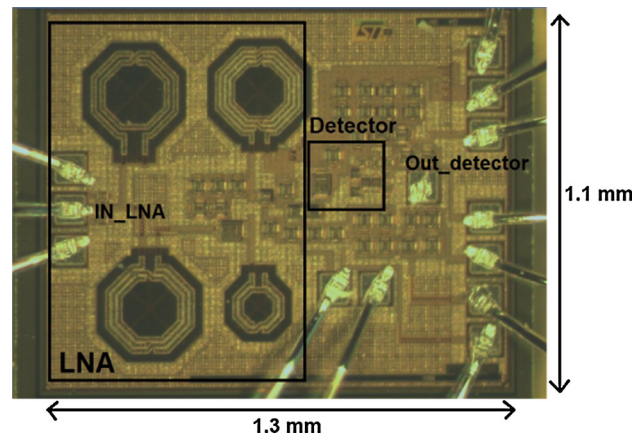


Fig. 17 Die micrograph of the non-coherent receiver

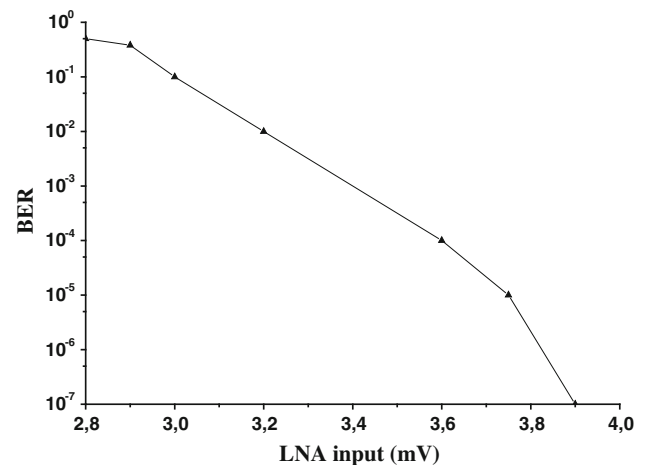


Fig. 18 BER measurement of the non-coherent receiver

The performance of the non-coherent receiver has been measured through the bit error rate (BER) characteristic. The test setup consists in simply connecting the non-coherent receiver to the 3–5 GHz pulse generator through a SMA cable and an attenuator in order to control the pulse

amplitude. A pseudo-noise sequence is sent to the pulse generator. The demodulated data (V_{out_det}) are registered in a 12 GHz DSO81204A oscilloscope from Agilent to then processed in Matlab in order to compute the BER. The measured BER as a function of the 3–5 GHz peak-to-peak pulse amplitude applied at the receiver input (LNA input) is given in Fig. 18 for a PRF of 100 Mpps. The receiver has been measured while setting the biasing voltages as follows: $V_{bias1} = 0.35$ V, $V_{ctrl} = 0.45$ V for the LNA and $V_{BIAS} = 0.59$ V, $V_{ctrl} = 0.6$ V for the detector. The voltage sensitivity is 1.7 mV_{peak} for a 10^{-3} BER and the power consumption of the RF front-end is 14.4 mW. The sensitivity is scaled at 100 kbps to facilitate comparison and is -89.3 dBm. At 100 Mbps, which is the maximum rate of the transceiver, the receiver consumption is 144 pJ/b.

5.3 Overview

The final link budget based on measurement results is presented in Table 2. From the emitted pulse magnitude ($0.95 V_{peak}$) and the voltage sensitivity (1.7 mV_{peak}), the

Table 2 Final link budget

PRF_{MEAN} (MHz)	49
PSD_{MAX} (dBm/MHz)	-41.34
BW_{-3dB} (GHz)	1.15
E_{p-MAX} (pJ)	1.78
A_{-MAX} (V) ^a	0.95
G_{TX} (dB)	3
G_{RX} (dB)	3
M_{dB} (dB)	6
A_{RX} (mV) ^b	1.7
E_{RX} (pJ)	12×10^{-6}
$P_{RX@30}$ Mpps (dBm)	-62.4
$P_{RX@100}$ kpps (dBm)	-89.3
d (m)	2.36

^a On a 100 Ω impedance

^b On a 50 Ω impedance

maximum communication range is evaluated to 2.36 m using (14) with $G_a = 3$ dB and $M = 6$ dB. This gives additional fade margin since 1.5 m is sufficient for WBAN applications. Compared with the preliminary link budget, the emitted energy is lower which allows the mean PRF to be increased to 49Mbps while complying with FCC. The overall performances of the transceiver are compared with previous published works in Table 3. In a burst mode with a burst PRF equal to 100 Mbps, and discounting the output dynamic reduction of the transmitter which occurs at 100 Mbps, T_{BURST} is equal to 490 μs and the idle time is 510 μs to maintain the same PSD and ensure FCC compliance at 49 Mbps. Such an idle time highly reduces the constraints on the power management function.

6 Conclusion

A high rate 3–5 GHz transceiver chipset for WBAN and medical applications has been implemented in a 130 nm CMOS process. The transmitter can generate bipolar pulses with a peak-to-peak amplitude of 1.9 V for a power consumption of 139 μW@100 kpps. A non-coherent receiver based on an envelope detector has been implemented. Bit error rate measurements show that a BER of 10^{-3} is achieved for a peak-to-peak amplitude of 3.4 mV at the receiver input. This corresponds to a receiver sensitivity of -89.3 dBm at 100 kbps and a power consumption of 14.4 mW. The calculated communication range of the proposed transceiver is 2.36 m in a free space propagation channel, which is sufficient for WBAN applications.

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Table 3 Transceiver performances and comparison with previous published works

Ref.	Tech. (nm)	Size (mm ²)	BW (GHz)	Fo (GHz)	d (m)	Tx-cons. (pJ/b)	Rx-Se (dBm)	Rx-cons (mW)	Rx-cons (nJ/b)
This Work	CMOS 130	4.33	2	4	2.36	196	-89.3@100 kbps	14.4	0.144@100 Mbps
[4]	CMOS 90	2.3	1–2	nc	2.5	45	-81@100 kbps	0.0143	0.143@100 kbps
[17]	CMOS 90	2	1.9	3	0.1	90	-64@125 Mbps	nc	0.09@500 Mbps
[14]	CMOS 130	2.25	1.25	7,25–8,5	3 ^a	186	-87@@100 kbps	4.2	0.84@5 Mbps
[15]	CMOS 65	0.3	4.6–5.4	5	0.05	25	-52.5@1 Mbps	0.290	0.29@1 Mbps
[13]	CMOS 90	0.6	3.6–4.3		1.5	258	-60/-66@1 Mbps	1.64/2.8	1.64/2.8@1 Mbps
[16]	CMOS 130	8	0.1–1	4.5	nc	23	-78	34	1.10@31 Mbps

^a With $G_a = 2$ dB and $M_{dB} = 2.2$

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