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# High Efficiency UWB Pulse Generator for Ultra Low Power Applications

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*This paper presents the design of a fully integrated ultra low power Ultra Wide Band (UWB) pulse generator. The circuit is designed and optimized for low rate and localization applications. This UWB transmitter is based on the impulse response filter method in order to achieve high energy sub-nanosecond pulses. The circuit has been integrated in a ST-Microelectronics CMOS 0.13 $\mu\text{m}$  technology with a supply voltage of 1.2V on a die area of 0.56mm<sup>2</sup>. A power manager is used to reduce the power leakages to 3.91 $\mu\text{W}$  which gives a power consumption of 3.98 $\mu\text{W}@10\text{Kbs}^{-1}$ . The measured dynamic energy consumed per pulse is 68pJ and the measured energy of the emitted pulse is 2.15pJ.*

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## I INTRODUCTION

Thanks to the gated nature of the signal, Ultra Wide Band Impulse Radio (IR-UWB) is a promising technology for ultra low power application. When efficient power gating techniques are used, the power consumption between two consecutive pulses can be highly reduced and the overall power consumption is scalable with the bit rate. Consequently, IR-UWB is a good candidate for ultra low power applications such as Radio Frequency Identification (RFID), or autonomous Wireless Sensor Network (WSN) in particular when localization capabilities are needed. For these applications, the need for (low cost) self or remotely powered communication systems is very high.

The design of an ultra low power communication system is a very challenging issue, especially concerning the radio-frequency front-end which generally consumes the greatest part of the power budget. For example, in a remotely powered RFID UHF transmitters commonly named passive TAGs, the available power is only about few micro-watts at 10 meters from the reader and has to supply the TAG [1]. In the case of a 10cm<sup>2</sup> photovoltaic harvesting system, the available power is around 100 $\mu\text{W}$  under 100lm (lumen) lighting which corresponds to a typical indoor environment. In both cases, the

energy must be stored which is a major drawback. First, the use of an energy tank such as external capacitors or micro-battery (cell) increases the manufacturing cost. Second, the communication is turned off when the battery is charging which reduces the instantaneous bit rate. IR-UWB can resolve these issues since previous published works present fully integrated transmitters having a power consumption of few micro-watts [2]. Such power consumption allows the system to be always powered and lower than the constraint on the storage. Since it reduces the storage constraints and can be fully integrated, IR-UWB appears to be a good low cost solution for ultra low power applications.

Moreover, IR-UWB is also a promising technology for localization systems due to the high temporal resolution of the signal. Both localization and low cost are interesting properties for ultra low power applications such as RFID or WSN, but they need high energy pulses to be efficiently exploited. Indeed, high energy pulses increase the localization precision [3] and enable the use of a low cost non-coherent receiver [4]. Finally, to meet these application requirements, the transmitted energy must be increased while the energy consumed by pulse must be reduced. In other words, the energy efficiency of the transmitter must be increased as much as possible. Consequently, this energy efficiency appears to be the most significant Figure Of Merit (FOM) in order to evaluate performance in such a context.

In this paper, we present the design of an ultra low power pulse generator providing high energy pulses. The power consumption and the energy efficiency have been optimized for ultra low power and low cost systems. In the first part, starting from the analysis of the FOM presented in the literature dedicated to pulse generators, a design strategy which optimizes the energy efficiency for a given low power application is presented. Then the proposed architecture, based on an integrated filter excitation technique, is described in section III. Particular attention is paid to the power management and to the output dynamic. The last section presents measurement results of the pulse generator realized in a standard 130nm CMOS technology.

## II POWER EFFICIENT TOPOLOGY

### A) Figure of Merit

For pulse generator design, the most often used FOM is the consumed energy per bit  $E_C$  which is easily derived from the power measurement as follows:

$$E_C = \frac{P_{DC}@PRF}{PRF} \quad (1)$$

where  $PRF$  is the pulse repetition frequency and  $P_{DC}@PRF$  the power consumption measured at a given  $PRF$ . In a practical implementation, due to leakage or biasing, some energy is consumed between the emission of two consecutive pulses and  $E_C$  varies with  $PRF$  as shown in Fig. 1. It is therefore difficult to extrapolate from  $E_C$ , the power consumption at any  $PRF$  and then to compare different architectures designed for different bit rates.

To overcome this limitation, [5] gives the power consumed at a  $PRF$  equal to 0Hz ( $P_{0Hz}$ ) which represents the leakage power and the energy dynamically consumed by the generator ( $E_{AC}$ ). As shown in Fig. 1, these metrics give the power consumption as a

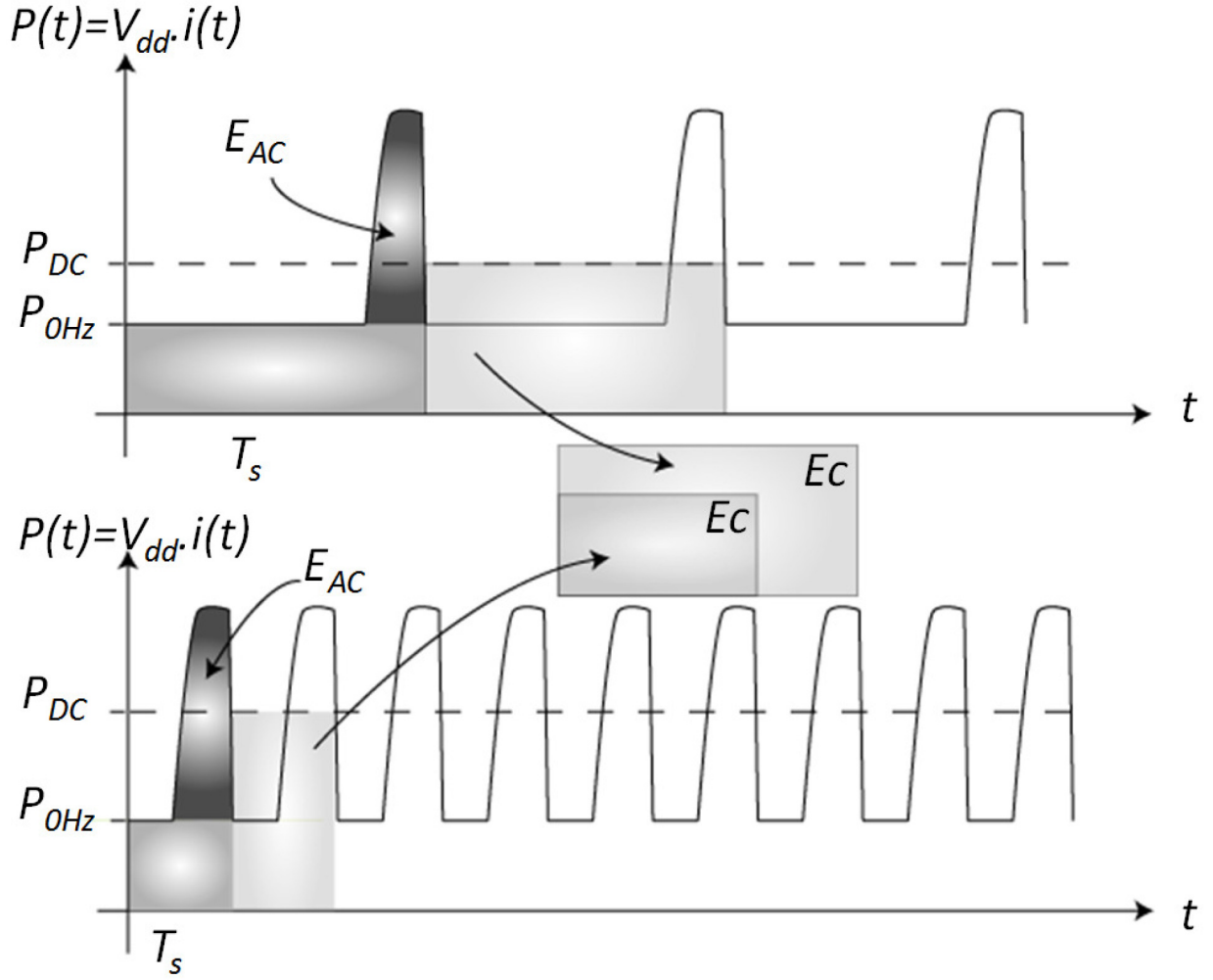


Figure 1: Instantaneous consumed power.

function of the  $PRF$  as follows :

$$P_{DC}(PRF) = P_{0Hz} + E_{AC} \cdot PRF \quad (2)$$

These FOM are interesting since they give the power consumption at any bit rate. Moreover, these FOM can be easily extracted from measurements since  $P_{DC}$  linearly varies with  $PRF$ .

However, this FOM has some limitations. Since it does not take the emitted power  $P_E$  into account, it is not possible to compare pulse generators that produce pulses with different energies. It is then relevant to evaluate the power efficiency which is finally equal to the energy efficiency shown as follows :

$$\eta(PRf) = \frac{P_E}{P_{DC}} = \frac{E_P \cdot PRF}{E_C \cdot PRF} = \frac{E_P}{P_{0Hz}/PRF + E_{AC}} \quad (3)$$

where  $E_P$  is the energy of the emitted pulse. This FOM can also be obtained from measurement data ( $E_P = P_E/PRF$ ). Due to the frequency limitation of some topologies,  $E_P$  can decrease with the  $PRF$ . This FOM enables this effect to be taken into account.

## B) Design strategies

Fig. 2 presents the power consumption of different published pulse generators. [5] and [6] principally use CMOS digital circuits which have no DC power consumption. This leads to a low  $P_{0Hz}$  which is mainly due to leakage current ( $96\mu\text{W}$  and  $5\mu\text{W}$  for [5] and [6] respectively). It appears that a low  $P_{0Hz}$  performs best at low rate and leakage is one of the main issues in this context. In [7], differential MOS Current Mode Logic cells are used. This gives a high DC power consumption ( $3.2\text{mW}@0\text{Hz}$ ) and a small  $E_{AC}$  ( $6.4\text{pJ/pulse}$ ) compared to other works ( $47$  and  $30\text{pJ/Pulse}$  for [5] and [6] respectively) since differential structures do not consume dynamic current. Fig. 2 clearly shows that this topology performs better for  $PRF$  higher than  $100\text{MHz}$  and that reducing  $E_{AC}$  is the main issue for the design of high speed pulse generators.

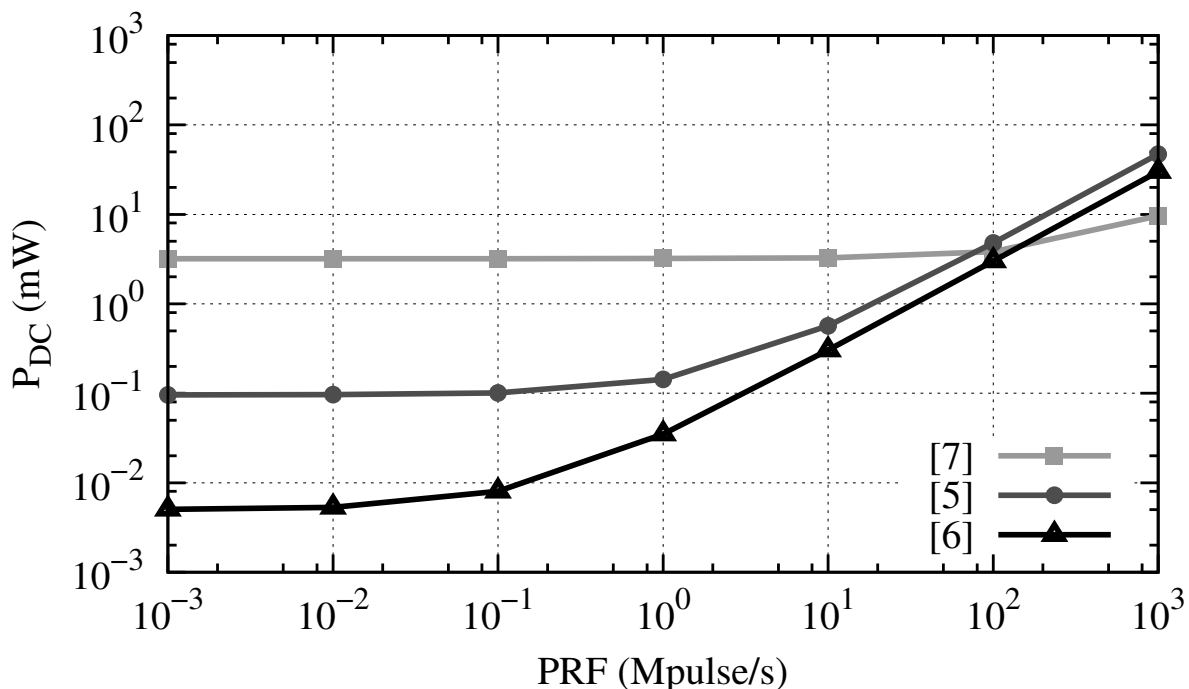


Figure 2: Power consumption of several published pulse generators.

The efficiency is given by (3) and shows relevant information. In Fig. 3 the efficiency is plotted as a function of the bit rate for the same generators as in Fig. 2. Since  $E_P$  is rarely given, it has been approximated using (6) and (7). For a better approximation, the effect of the pulse envelope on the energy is taken into account. Depending on the pulse shape, the pulse is modeled by a sine wave modulated by square function (4) or by a Gaussian pulse transposed at the center frequency  $f_M$  of the pulse (5).

$$p_S(t) = A \sin(2\pi f_M t) \pi_\tau(t) \quad (4)$$

$$p_G(t) = A \exp(-at^2) \cos(2\pi f_M t) \quad (5)$$

The energy of the pulse can then be easily derived from the maximum value of the pulse  $A$  and its width  $\tau$  as follows:

$$E_{PS} = \frac{A^2}{Z_L} \left[ \frac{\tau}{2} - \frac{\sin(2\pi f_M \tau)}{4\pi f_M} \right] \quad (6)$$

$$E_{PG} = \frac{A^2}{2Z_L} \sqrt{\frac{\pi}{2a}} \left[ 1 + \exp\left(-\frac{|4\pi f_M|^2}{8a}\right) \right] \quad \text{with } a = \frac{\pi^2 BW_{-XdB}^2}{2 \ln(10^{XdB/10})} \quad (7)$$

where  $Z_L$  is the load impedance of the pulse generator and  $BW_{-XdB}$  the  $-XdB$  bandwidth. An analysis of the efficiency gives interesting information for the design strategies. [5] achieves a higher output dynamic  $A$  than [6] which consequently increases the dynamic consumed energy  $E_{AC}$ . It is a drawback when only the power consumption is considered but, as shown in Fig. 3, the efficiency is finally higher for bit rates higher than a few MHz. It also appears that maximizing the output dynamic is an important issue when high efficiency is needed, even if it is at the cost of an increased  $E_{AC}$ .

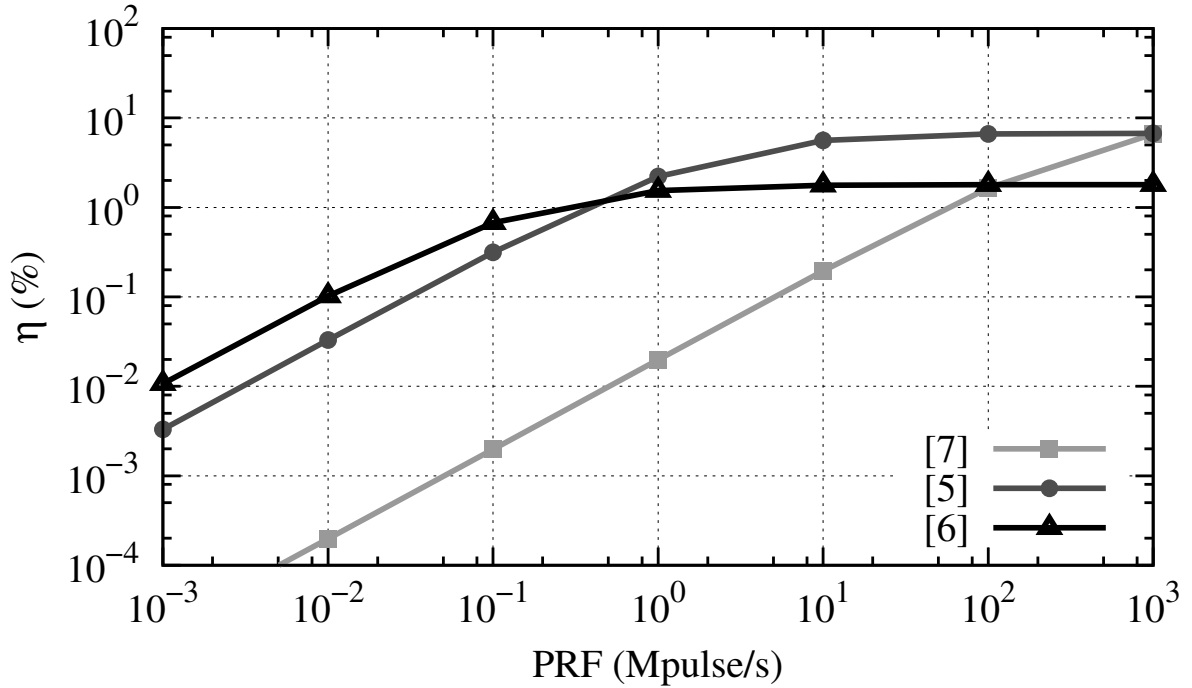


Figure 3: Energy efficiency of several published pulse generators.

Based on these observations, the presented design will first focus on leakage current reduction methods to address ultra low power and low rate applications. Secondly, the output dynamic will be maximized (at the cost of an increased  $E_{AC}$ ) to improve the efficiency and also to optimize the power budget which is an important issue in low power applications.

### C) Architecture Choice

Among the different techniques used for pulse generation, ON/OFF Local Oscillator (LO) and filter excitation are the most promising topologies to reduce power consumption. To

maximize the output dynamic and the bandwidth in ON/OFF LO, the LO start time must be as small as possible and an inverter based ring oscillator should be preferred [8]. With such topology, CMOS technology can be used which reduces the  $P_{0Hz}$ . ON/OFF LO technique highly reduces the  $P_{0Hz}$  since the LO is turned on only during the pulse duration. To be fully efficient, the power amplifier or the antenna driver must be power managed [9, 10]. To reduce further the time conduction of the active cells, it is possible to use filter excitation. With such a technique, a very short baseband pulse is used to excite a filter to produce its impulse response. Here, the conduction time of the active cells is around 100ps [7] and is independent of the pulse bandwidth  $BW$  whereas in ON/OFF LO it depends on  $1/BW$ . A short time conduction of the active cells limits  $E_{AC}$  and improves the efficiency. Moreover, the filter excitation technique can achieve large amplitude pulses which lead to high  $E_P$ . It also facilitates the integration and the packaging process [11]. At last, the filter excitation well suits the generation of sub-nanosecond duration pulses needed to reach high localization precision [7]. The proposed architecture is based on an integrated filter excitation technique and the principle is given in Fig. 4. The baseband pulse used to excite the filter is generated by a Low-Vt Digital Edge Combiner implemented with CMOS logic cells. To reduce the leakages, a high-Vt Managed Power Supply (MPS) which control managed power lines (V-VDDX and V-GNDX) is used. The filter is a passive fully integrated circuit and is driven by a C class amplifier to reduce  $P_{0Hz}$  consumption.

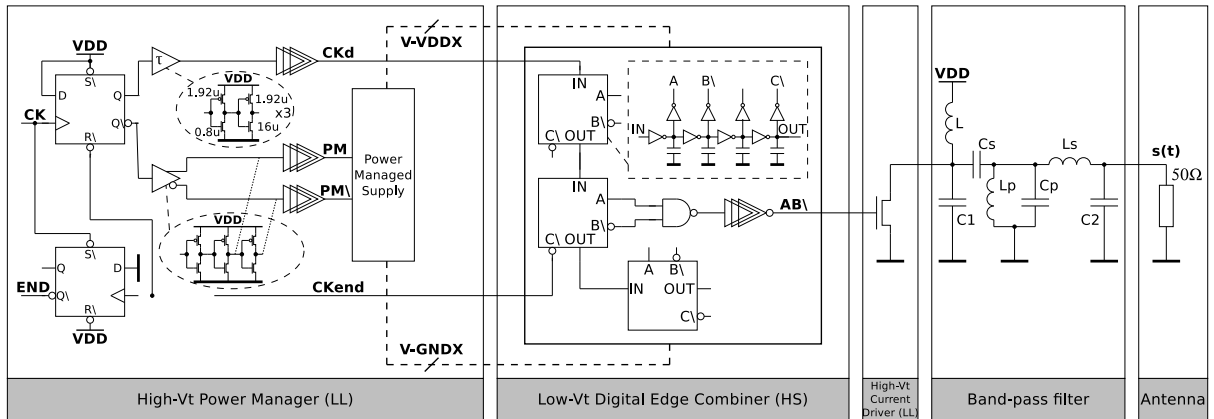


Figure 4: Proposed pulse generator principle.

### III PULSE GENERATOR DESIGN

The pulse  $s(t)$  produced by the excitation filter technique is the response of the filter to a baseband pulse  $\pi_\tau(t)$ . The expression of  $s(t)$  and its Fourier transform are given by :

$$s(t) = \frac{B}{\sqrt{l}} \cdot \pi_\tau(t) * h_E(t) \quad (8)$$

$$S(f) = \frac{B\tau \text{sinc}(\pi\tau f) \cdot H_E(f)}{\sqrt{l}} \quad (9)$$

where  $l$  represents the power loss of the filter,  $H_E(f)$  the normalized transfer function of the filter,  $B$  the magnitude of the baseband pulse and  $\tau$  its time duration. The main characteristics of the pulse are given by the baseband pulse (through  $B$  and  $\tau$ ) and by the filter impulse response. This technique has been widely presented and a detailed sizing method is given in [7]. In this design, we use a third order Bessel-Thompson filter driven by a 1.2V magnitude and 75ps width baseband pulse. A standard CMOS 130nm technology is used.

## A) Power Management System

The aim of the power manager is to reduce the leakage current when no pulses are generated. Several techniques have been proposed to reduce leakage current of CMOS logic circuits. A first technique named VTCMOS consists in applying different bias voltages to the substrate depending on the operating mode of the cell [12]. When the cell is off, the substrates of the NMOS transistor (resp. PMOS) can be for example connected to VDD (resp. GND) in order to increase (resp. decrease) the threshold voltage  $Vt$  and thus limiting the leakages. A second technique (DTCMOS) consists in dynamically changing the threshold voltage when the circuit is commuted [13]. In the CMOS inverter case, the gates of the PMOS and NMOS are connected to the substrate. For both VTCMOS and DTCMOS, an isolated substrate is needed and triple-well or SOI technologies must be used which increase the manufacturing cost. A third solution is to use a multi-Vt CMOS technology [14] which provides transistors having different threshold voltages. Most of the standard CMOS technologies offer Low Leakage (LL) transistors having high-Vt and High Speed (HS) transistors having low  $Vt$ . The proposed power manager uses a multi-Vt-CMOS approach where Low Leakage (LL) transistors are used to power supply the High Speed (HS) transistors which are used to implement the Low-Vt Digital Edge Combiner.

The elementary inverter used in the design of the Digital Edge Combiner is presented in Fig. 5. The NMOS and PMOS HS transistors have respectively their bulks connected to GND and VDD whereas their sources are respectively connected to the managed power line V-GNDX and V-VDDX provided by the MPS. The MPS is based on LL inverters which are sized in order to deliver the same drain source current  $I_{DS}$  than the HS transistors. Since  $I_{DS}$  is a linear function of the saturation current density  $J_{SAT}$  (A.m-1) and of the MOS width  $W$  [15], the required size of the LL is given by :

$$W_{LL} = \frac{J_{SAT-HS}}{J_{SAT-LL}} \cdot W_{HS} \quad (10)$$

where the NMOS, or the PMOS transistors of the HS and LL inverters can be considered. The idle state of the HS inverter output defines the signal to be connected at the input of the LL inverter of the MPS. When the idle state is 0, the LL inverter input which provides V-GNDX is connected to VDD and the LL inverter input which provides V-VDDX is connected to PM since it is the power management signal active on the high state provided by MPS. When the idle state is 1, the LL inverter input which provides V-GNDX is connected to PM and V-VDDX is connected to GND. Thus, when power management is active ( $PM = 1$ ), HS inverter is short-circuited since its V-GNDX, V-VDDX and also OUT are equal to the same voltage. In this case, the total leakage



depends only on twice the sum of leakage current of the LL inverter which is much lower than the HS inverter leakage for an equivalent saturated current. The gain  $g_{OFF}$  on the leakage power  $P_{0Hz}$  achieved by this power management technic only depends on the saturation current density  $J_{SAT}$  of the LL and HS transistor and is given by :

$$g_{OFF} = \frac{J_{OFF-HS} \cdot W_{HS}}{2 \cdot J_{OFF-LL} \cdot W_{LL}} = \frac{J_{OFF-HS} \cdot J_{SAT-LL}}{2 \cdot J_{OFF-LL} \cdot J_{SAT-HS}} \quad (11)$$

where  $J_{OFF}$  is the linear leakage current density ( $A.m^{-1}$ ) of the considered MOS transistor. It clearly appears that the proposed power management technic has benefits only when the ratio between  $J_{SAT}$  and  $J_{OFF}$  of the LL inverters is greater than twice the one of the HS.

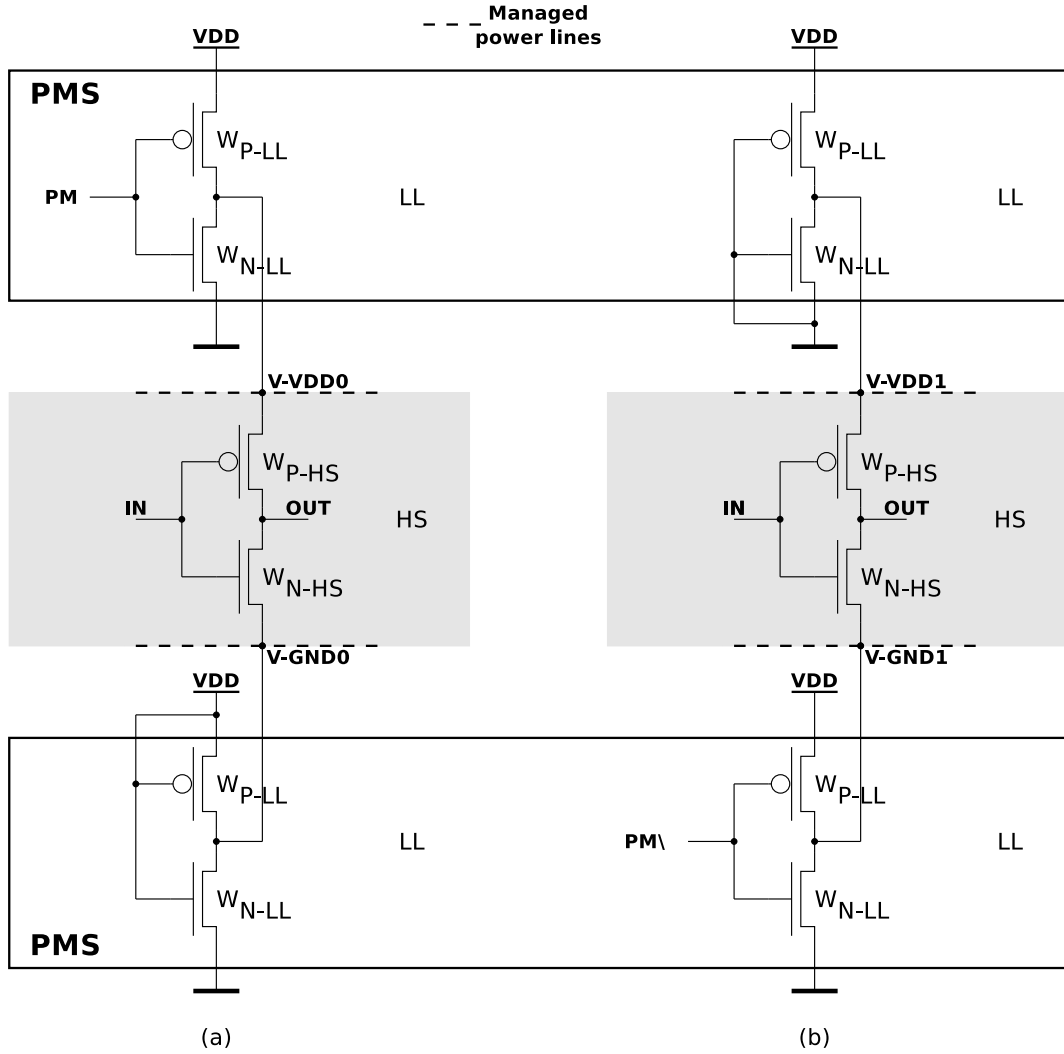


Figure 5: Inverter set to 0 (a) and set to 1 (b) in the idle state with its associated Managed Power Supply (MPS).

In the case of a more complex logic function such as the inverter chains used in the edge combiner or in the power manager, a particular focus has to be done on the chosen idle state of each stage which composes the function. Here the idle states have to be alternatively 0 and 1 in order to keep coherent logic states with the realized logic function inside each HS stage as shown on Fig. 6 where an inverter chain with a growth factor of  $h$  is represented. To reduce the complexity, LL inverters with an identical input signal can be merged in order to simplify the final circuit. To limit the current driven by each inverter and to improve the decoupling, the LL inverters are split into several parts which are distributed all along the power line.

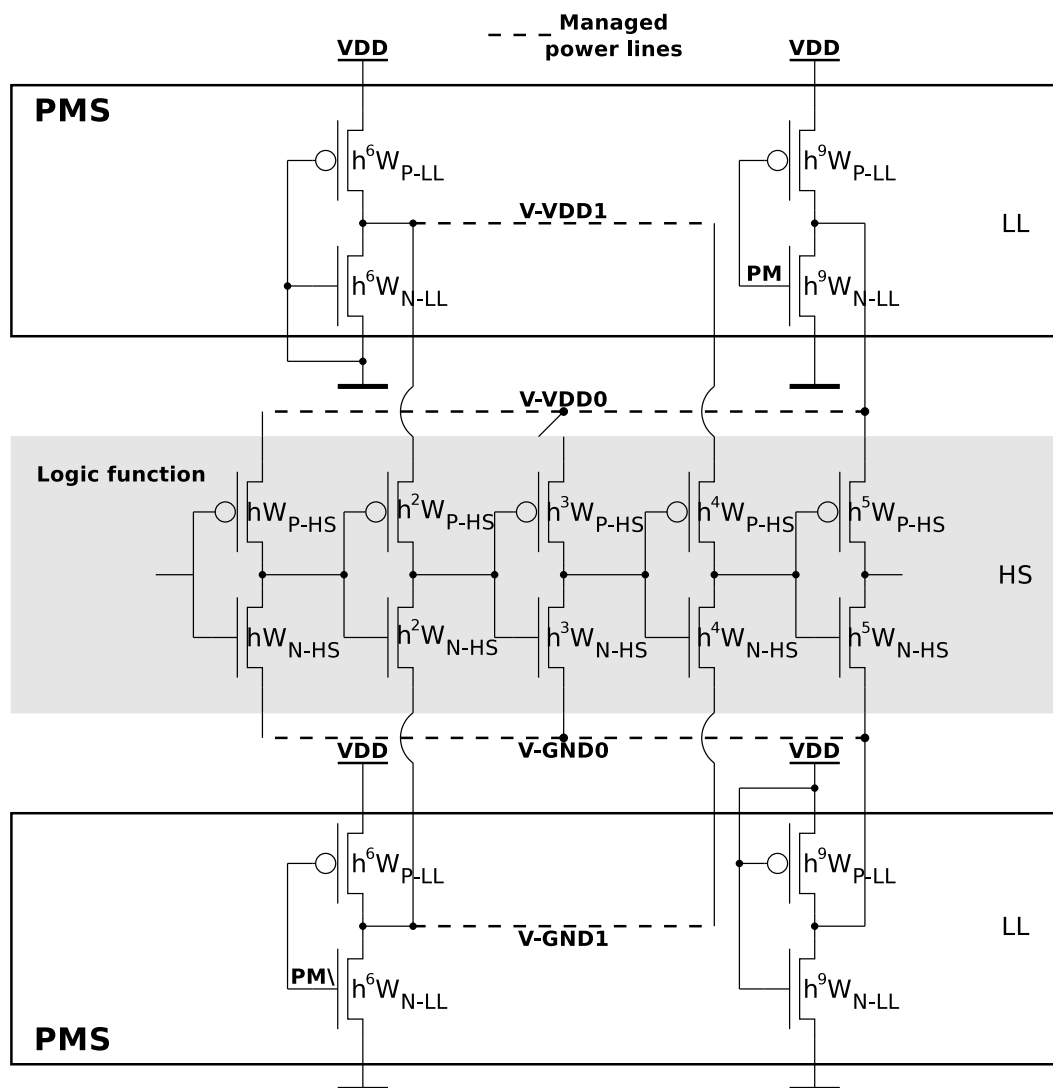


Figure 6: Inverter chain with MPS.

## B) Edge combiner

The edge combiner used has to generate the baseband pulse required by the filter excitation technique when a rising edge appears on CK. Then, CK is used to set PM and PM $\setminus$  to GND and VDD respectively and then to control the MPS. As shown in Fig. 7, CK is delayed (CKd) before being provided to the edge combiner in order to ensure that the circuits are turned on when the signal is applied to the input. CKd is propagated through a delay line. Two consecutive edges (A and B $\setminus$ ) are combined to produce the baseband pulse needed to excite the filter. CKd is further delayed to produce the signal (CKend) which is used by the power manager to shut down the power lines. The edge combiner uses only CMOS logic gates implemented with HS transistors and driven by the MPS. The baseband pulse is produced by using a simple CMOS NOR gate based on inverters designed as described above. A driver based on an inverter string is inserted at the output to match the small transistors ( $W=10\mu\text{m}$ ) used in the NOR gate with the large ones used in the filter driver.

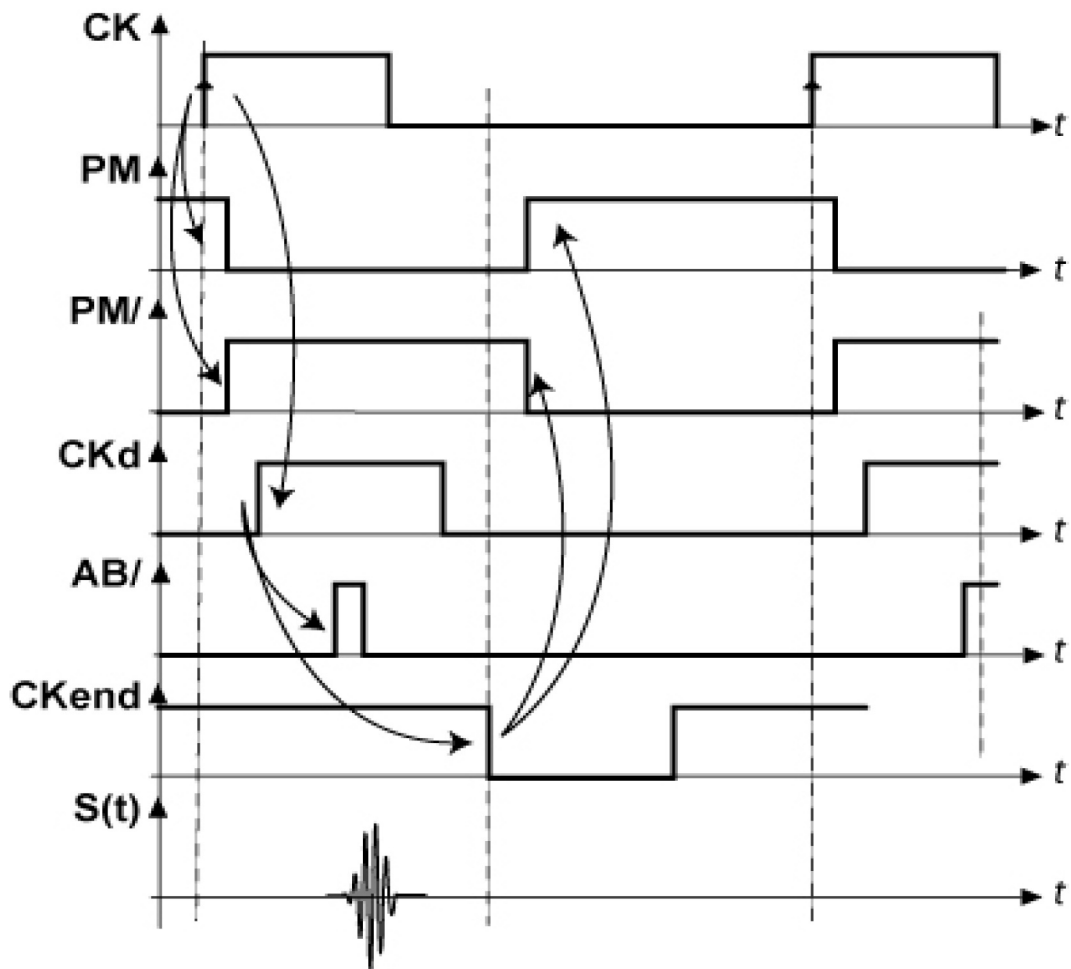


Figure 7: Main signal chronograms.

### C) Band pass filter and filter driver

The band pass filter is a Bessel-Thompson filter. This filter is chosen because a third order is sufficient to match the FCC mask. Low order reduces the number of inductors needed and then reduces the loss in the filter which finally maximizes the  $E_P$ . The filter must be carefully designed and the interconnected wires must be shortened during the layout realization to limit loss. The parasitic capacitances of the inductors must be compensated to avoid the degradation of the filter impulse response and to ensure that the pulse complies with the FCC mask. Among the different possible filter structures, the one chosen offers many advantages. The first resonator (L-C1) can be used to bias the filter driver. Cs achieves a DC isolation and C2 can be used to compensate the pad capacitance. Moreover, Cp can be reduced to compensate the parasitic capacitance of Lp. Cp and Cs can be reduced to compensate that one of Ls and C1 can be reduced to compensate both the output capacitance of the filter driver and the parasitic capacitance of L. The filter is driven in a current mode in order to achieve a pulse magnitude greater than the supply voltage on the  $50\Omega$  input impedance of the filter. The driver is a class C amplifier to avoid power consumption when no pulse is generated. To further reduce the leakage, a LL transistor is used. The width of the transistor M1 is tuned to maximize the energy efficiency given by (3) which leads to a value of  $560\mu\text{m}$ . The main parameters of the filter design are summarized in Table 1.

Table 1: Main design parameters summary.

L (pH)	C1 (fF)	Cs (fF)	Lp (nH)	Cp (fF)	Ls (nH)	C2 (fF)	$W_{M1}$ ( $\mu\text{m}$ )
326	486	584	1.08	338	1.05	32	560

## IV MEASUREMENT RESULTS

The pulse generator has been designed with a  $0.13\mu\text{m}$  standard CMOS technology from ST Microelectronics. The die is shown in Fig. 8 and its area is  $0.56\text{mm}^2$ . The measured time and normalized frequency responses of the generated pulse are given in Fig. 9. The -10dB bandwidth ( $BW_{-10dB}$ ) is 5.22GHz and is centred on 6.25GHz. The very wide bandwidth of the pulse leads to a very short time duration equal to 0.6ns which is a large benefit for localization precision but a major drawback for the emitted energy. The pulse magnitude is 2Vpp and produces high pulse energy although the duration of the pulse is short. The measured energy of the emitted pulse is 2.15pJ whereas the approximation given by (7) is 2.37pJ which confirm the accuracy of this approximation.

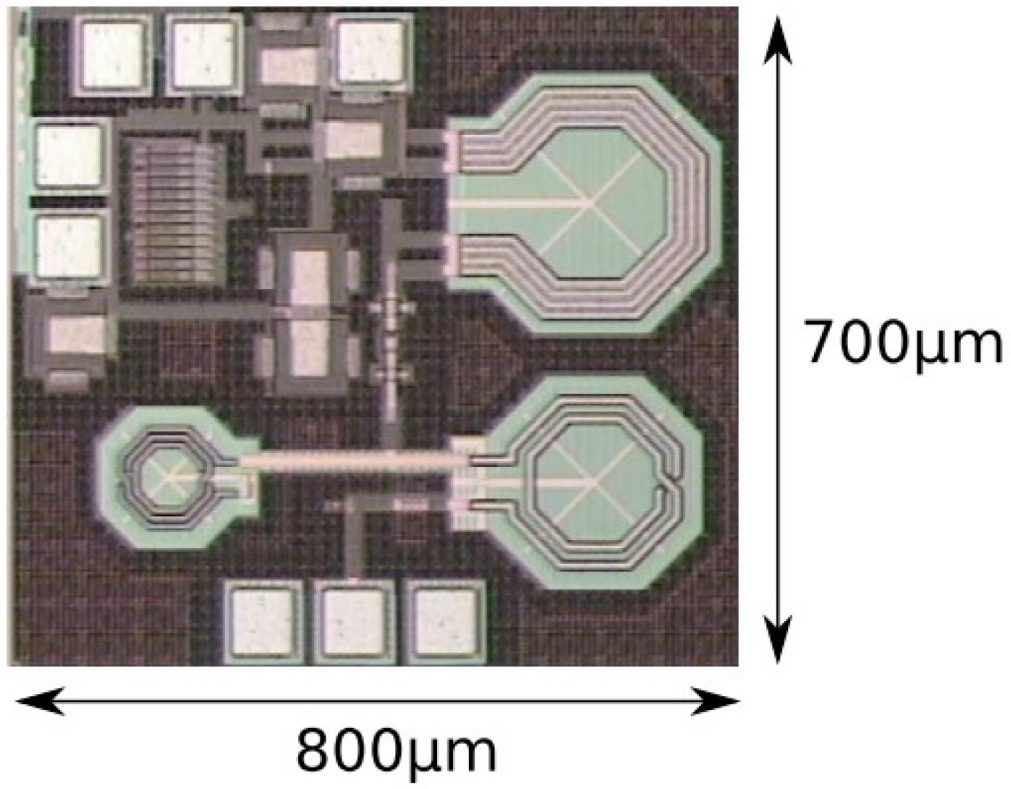


Figure 8: Die photograph of the proposed pulse generator.

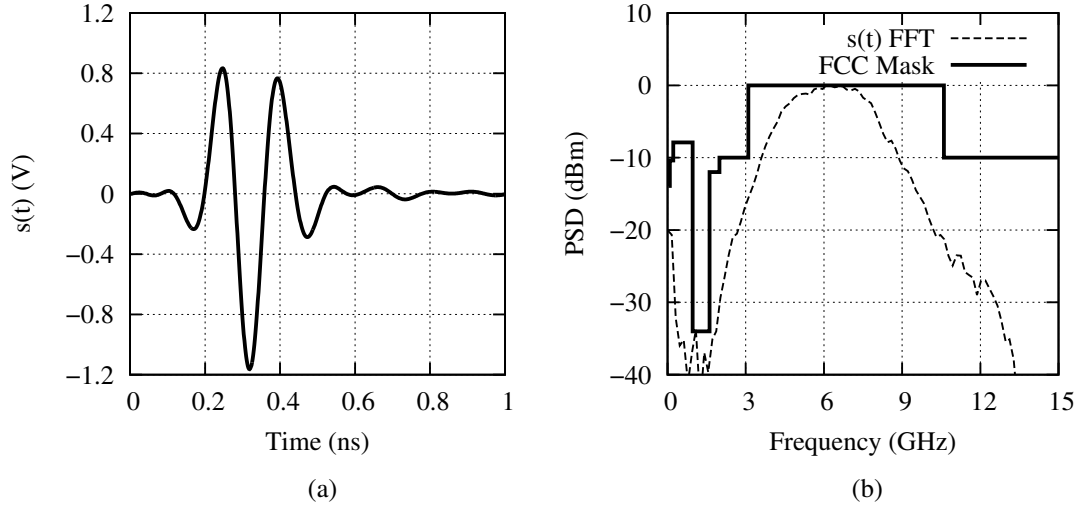


Figure 9: Measurement of the time response (a) and the frequency response (b).

The static leakage current is equal to  $3.26\mu\text{A}$  which leads to a power leakage  $P_{0Hz}$  of  $3.91\mu\text{W}$  for a voltage supply of 1.2V. Half of the power leakage is due to the filter driver. The measured power consumption is plotted for different PRF in Fig. 10 and is identical to the one obtained (2). The performances are compared with previous works in Fig. 10. The power consumption is only  $3.98\mu\text{W}@1\text{kbs}^{-1}$  and  $10.7\mu\text{W}@100\text{kbs}^{-1}$  which is well suited for ultra low powered applications. The value of  $E_{AC}$  is extracted from this measurement and is 68pJ. Most of the consumed dynamic energy is due to the inverter string needed to match the edge combiner with the filter driver. In Fig. 11, the efficiency is plotted as a function of the PRF as introduced in (3) and is compared to previously published works which are summarized in Table 2. The pulse generator also exhibits good efficiency at low rates ( $0.06\%@1\text{kbs}^{-1}$  and  $2.22\%@100\text{kbs}^{-1}$ ).

Table 2: Performance summary of the proposed pulse generator and comparison with previous works.

Ref.	V <sub>pp</sub> (V)	VDD (V)	Width (ns)	BW (-10dB)	f <sub>M</sub> (GHz)	P <sub>0Hz</sub> (μW)	E <sub>AC</sub> (pJ)	E <sub>P</sub> (pJ)	Area (mm <sup>2</sup> )	CMOS (nm)
[2]	0.61	0.9	2.0	0.5GHz	2.9-3.8	184	65	1.60 <sup>2</sup>	0.60 (die)	90
[5]	0.65	1.0	3.0	0.5GHz	3.5-4.5	96	47	3.17 <sup>1</sup>	0.08 (core)	90
[6]	0.45	1.0	3.0	1.0GHz	3.5-4.5	5	30	0.54 <sup>2</sup>	0.42 (core)	90
[7]	1.42	1.2	0.5	6.8GHz	7.3	3200	6.4	0.64 <sup>2</sup>	0.54 (die)	130
[9]	0.16	1.5	3.5	0.5GHz	3.8	3900	17	0.11 <sup>2</sup>	0.66 (die)	180
[16]	0.60	1.0	2.5	0.5GHz	2.1-5.7	124	17	1.75 <sup>2</sup>	0.07 (core)	90
[17]	0.09	0.9	3.5	0.5GHz	3.5-4.5	170	12	0.03 <sup>2</sup>	0.03 (core)	65
[18]	0.45	0.9	2.4	0.5GHz	3.5-4.5	2.8	29	1.20 <sup>1</sup>	1.30 (die)	90
This work	2.00	1.2	0.6	5.2GHz	6.3	3.91	68	2.37 <sup>2</sup>	0.56 (die)	130

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<sup>1</sup>Computed with (6)

<sup>2</sup>Computed with (7)

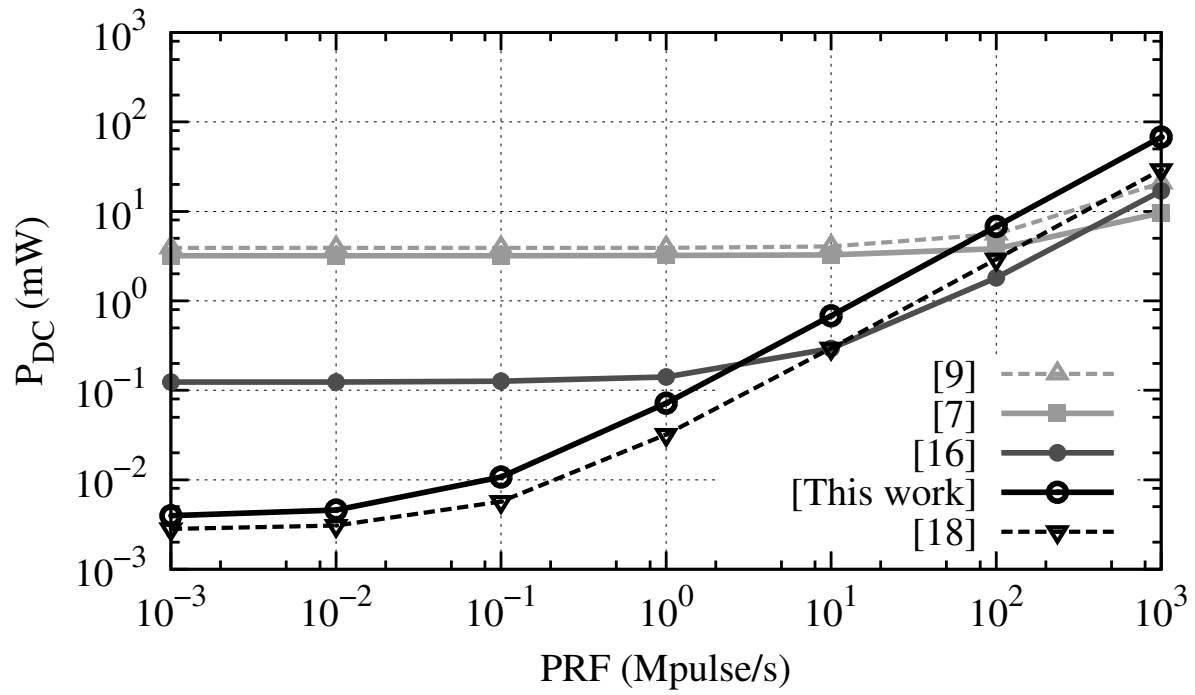


Figure 10: Measured power consumption as a function of the PRF.



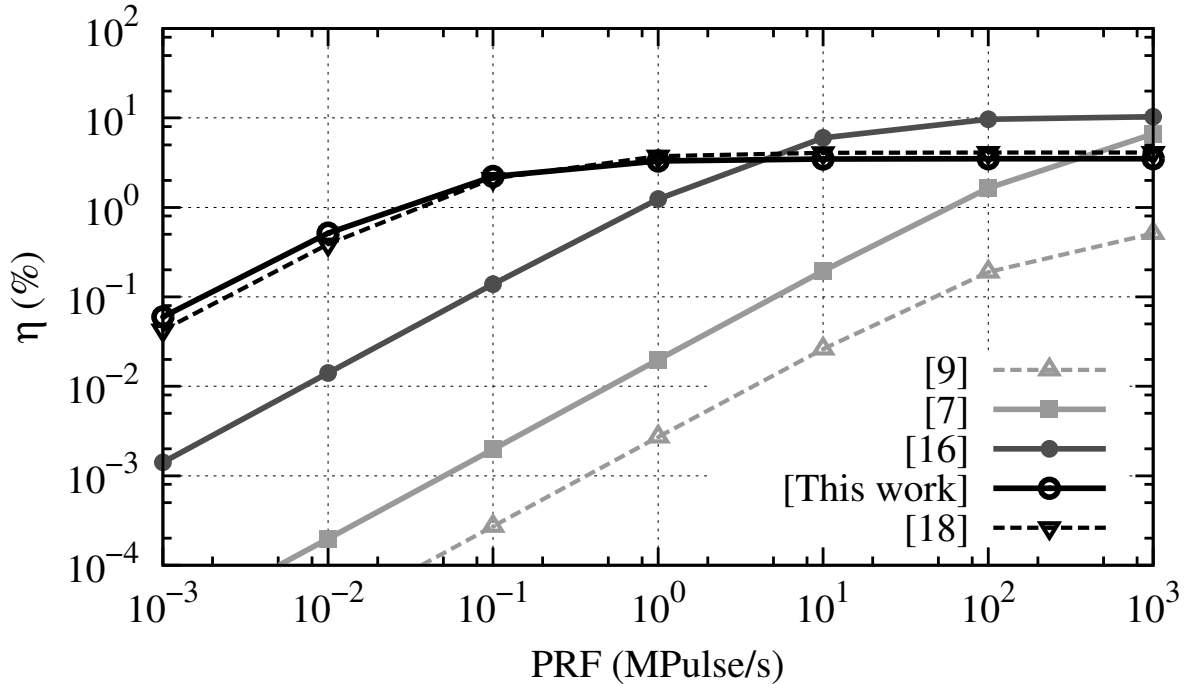


Figure 11: Estimated efficiency as a function of the PRF.

## V CONCLUSION

The design of an ultra low power and high efficient pulse generator has been presented. The topology has been carefully chosen to achieve good performances at low rates. It is demonstrated that the filter excitation technique can generate very short 2.15pJ pulses which can be helpful for high precision location applications. Associated to a power management technique which reduces leakage current, this topology demonstrates also low power capabilities ( $3.98\mu\text{W}@10\text{kb/s}^{-1}$ ) and could be used in ultra low power systems.

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