Remarkable Strength Characteristics of Defect-Free SiGe/Si Heterostructures Obtained by Ge Condensation

Thomas David, Kailang Liu, Sara Fernandez, Marie-Ingrid Richard, Antoine Ronda, Luc Favre, Marco Abbarchi, Abdelmalek Benkouider, Jean-Noël Aqua, Matthew Peters, et al.

Remarkable Strength Characteristics of Defect-Free SiGe/Si Heterostructures Obtained by Ge Condensation

Thomas David,[*,†] Kailang Liu,[†] Sara Fernandez,[‡] Marie-Ingrid Richard,[‡,†] Antoine Ronda,[†] Luc Favre,[†] Marco Abbarchi,[†] Abdelmalek Benkouider,[†] Jean-Noël Aqua,[¶] Matthew Peters,[§] Peter Voorhees,[§] Olivier Thomas,[†] and Isabelle Berbezier[†]

Aix-Marseille Univ. CNRS IM2NP, St Jérôme F-13397 Marseille France, ESRF, ID01 beamline, CS 40220, 38043 Grenoble Cedex 9 France, INSP, Boite 840; 4 pl. Jussieu; 75005 Paris., and Department of Materials Science and Engineering, Northwestern University, 2220 Campus Drive, Evanston, IL 60201, USA

E-mail: thomas.david@im2np.fr

Abstract

In this work, we compare the morphological and structural features of SiGe membranes fabricated by three different processes: direct deposition of $Si_{0.5}Ge_{0.5}$ on Si(001) nominal substrate, direct deposition of $Si_{0.5}Ge_{0.5}$ on silicon on insulator, and deposition of SiGe with low Ge concentration on silicon on insulator followed by Ge enrichment by condensation. We show that the formation of fully strained Ge rich layers free of defects with flat surface is only possible by the two-steps epitaxy/condensation process. We demonstrate that the condensation based process enables the total inhibition of the morphological instability, together with the hindering of dislocations for critical thickness much larger than the ones commonly obtained by direct deposition. Those behaviors could be explained by the injection of self-interstitials in the Ge rich layers during condensation. Such remarkable properties could be generalized to many other systems using similar condensation process.

Introduction

Microelectronic industry needs to combine various strain additives techniques to achieve the mobility enhancement needed in each transistor and raise the drive current of the device. Compressive stress liners and SiGe compressively strained channels have been engineered to increase the level of stress and produce the desired stresses to benefit nMOS and pMOS transistors. Furthermore, the benefits of strain are not limited to transistors, they also improve the charge retention and reduce the tunneling leakage current in memory devices. Since the advent of Silicon On Insulator (SOI) technology, its implementation in microelectronics and photonics systems is more pervasive and widespread than ever. The benefits of SOI could be efficiently combined with strained semiconductors approaches to yield additional

[*]To whom correspondence should be addressed

[†]Aix-Marseille Univ. CNRS IM2NP, St Jérôme F-13397 Marseille France

[‡]ESRF, ID01 beamline, CS 40220, 38043 Grenoble Cedex 9 France

[¶]INSP, Boite 840; 4 pl. Jussieu; 75005 Paris.

[§]Department of Materials Science and Engineering, Northwestern University, 2220 Campus Drive, Evanston, IL 60201, USA

performance enhancement. The ability to fabricate SOI and SiGe On Insulator (SGOI) fully strained layers offers various advantages to produce mixed substrates in which n-channels are made of thin SOI layer while p-channels are made of thin SGOI films.[1,2] These two systems have been reported to exhibit the ultimate in mobility and current drive characteristics.[3–6]

SOI is then anticipated to become the future substrate for the mainstream electronic applications. Many of the expected advances will depend on the further steps of the CMOS process on SOI and in particular the epitaxy of defect-free Si and SiGe ultra-thin layers. SGOI is commonly produced by the germanium condensation technique. In this technique a dilute (typically $Si_{0.9}Ge_{0.1}$ layer) is first epitaxially grown on SOI. Then, an oxidation step is performed to produce a Ge-enriched layer which intermixes with the underlying Si layer to form a quasi-homogeneous SiGe layer. This epitaxial approach has the drawback of being carried out at high temperature and results in the formation of a high density of mismatch defects in the SiGe layer.[1,7] In terms of elastic properties, such very thin crystalline layers on a compliant ultra-thin buried oxide layer (UT-BOX) pose their own challenges. SOI could act as a compliant substrate if it is mechanically decoupled from the wafer at the Si/SiO_2 interface. Compliant substrates represent one of the most promising approaches for the growth of heteroepitaxial layers virtually free of dislocation defects.[8] A sufficiently thin or elastically soft compliant substrate becomes strained by the deposition of the epitaxial layer and the lattice mismatch should be accommodated by elastic strain in the compliant layer.[9–11]

The partitioning of strain between the epitaxial layer and its substrate causes a reduction in the overall strain energy. Despite extensive studies, the major issue whether SOI behaves as a compliant substrate is still under debate. The first problem is that, in several studies, the thickness of the compliant top Si SOI layers was not thin enough to avoid dislocations in the epitaxial layers according to our model.[11–14] The second problem comes from the Si/SiO_2 interface which is not fully slippery at temperatures of growth[15] and only started to glide at very high temperature in conjunction with the formation of misfit dislocations.[16]

Moreover, several studies focus on the formation and compositional evolution of SiGe layers epitaxially deposited on SOI during thermal oxidation. It is commonly reported that at a high oxidation temperature SiGe interdiffusion is dominant and allows the formation of SiGe layer with smooth but gradually decreasing Ge concentration profile. Such layer can be easily homogenized by a non-oxidizing high temperature annealing and form a dilute SiGe layer on top of the oxide. In these conditions, the process of SiGe interdiffusion is strong enough to homogenize all the Ge accumulated beneath the oxidation front across the SiGe/Si system.[15] The composition of these homogeneous diluted SiGe layers results from the perfect intermixing between the nominal SiGe epitaxial layer and the SOI pseudo-substrate without any visible loss of Ge during oxidation.[17] Even if this composition can be tuned as a function of the nominal SiGe concentration/thickness, SOI thickness and annealing conditions, it remains lower than that of the nominal diluted epitaxial SiGe layer.

In contrast, at low oxidation temperature, the Ge repulsion mechanism is dominant and produces a Germanium Rich Layer (GRL) with a surprisingly fixed Ge concentration x=0.5 whatever the experimental conditions are (*i.e.* initial SiGe composition, epitaxial stress, oxidation duration).[18] The very abrupt GRL/SOI interface and the constant composition of the GRL ($Si_{0.5}Ge_{0.5}$) over a 700-850 °C oxidation range of temperatures, follows from the dramatic decrease of germanium diffusion in Si compared to $Si_{0.5}Ge_{0.5}$. In these conditions the final GRL concentration is enriched as compared to that of the initial $Si_{0.8}Ge_{0.2}$ and reaches $Si_{0.5}Ge_{0.5}$. The layers obtained are fully strained, perfectly flat and free of extended defects.

To understand the role played by SOI substrate on the strain and morphology of GRL, we analyse in the present work, the morphological and structural features of SiGe membranes fabricated by three different processes: (1) di-

rect deposition of $Si_{0.5}Ge_{0.5}$ on Si(001) nominal substrate, (2) direct deposition of $Si_{0.5}Ge_{0.5}$ on SOI and (3) an epitaxy of dilute $Si_{0.8}Ge_{0.2}$ on SOI followed by Ge enrichment during thermal oxidation. After precise strain characterization of the three samples, we show that the formation of fully strained GRL free of defects with a flat surface is only possible by the two steps epitaxy/condensation process (*i.e* process 3). We demonstrate that only in these conditions, the morphological instability is inhibited and the nucleation of dislocations is hindered. These behaviors are attributed to the reduced surface diffusion at the SiO_2/SiGe interface and the injection of self-interstitials produced by the oxidation process respectively. We suggest that the phenomenon could be generalized to other systems if appropriate experimental conditions are available.

Experimental details

In this study we focus on the comparison of three samples: sample A was obtained by the condensation process, *i.e.* epitaxy of a 30 nm thick $Si_{0.8}Ge_{0.2}$ layer on SOI followed by rapid thermal oxidation (RTO) to obtain 8 nm of $Si_{0.5}Ge_{0.5}$ on the SOI. Sample B was obtained by direct MBE of 8 nm of $Si_{0.5}Ge_{0.5}$ on SOI and sample C was obtained by direct MBE of 8 nm of $Si_{0.5}Ge_{0.5}$ but on nominal (001) Si substrate. A schematic representation of the three structures is given in Fig. 1.

The specific Ge-rich layers have been obtained via three different processes either on a Silicon-On-Insulator (SOI) substrate or a Si (001) nominal substrate. The SOI substrate was fabricated using the SmartCut^{TM} process.[19] It consists of a top 12 nm ultra-thin Si layer on 10 nm UT-BOX. Then, $Si_{1-x}Ge_x$ layers of different thicknesses, with x=0.2 or x=0.5 were epitaxially grown by Molecular Beam Epitaxy on the cleaned SOI substrates. Surface preparation for epitaxy consists of *ex situ* and *in situ* cleaning. *Ex situ*, the silicon cleaning follows a modified Shiraki recipe: (i) 10 min in HNO_3(65 %) heated at 70 °C, (ii) 1 min in deionized water, and (iii) 30 s in HF (5 %). The samples are introduced into an ultrahigh-vacuum MBE RIBER MBE32 growth chamber with a base pressure below 10^{-10} torr. As a consequence of the dewetting instability[20,21] *in situ* heating cannot be applied to very thin SOI. Instead, we finish the *ex situ* clean by HF to leave the surface unoxidized and we introduce the sample right away in the chamber. Then, we *in situ* anneal it at 550 °C for 30 min. SiGe layers are deposited at 450 °C.

Low temperature oxidation was carried out at 750 °C for 8h by steps of 30 min in accordance with the Rapid Thermal Oxidation (RTO) furnace JIPELEC technical specifications. These conditions were extracted from previous experiments using similar condensation process,[18] that provided accurate data on the experimental RTO conditions to obtain a single $Si_{0.5}Ge_{0.5}$ layer on SOI. To prevent SiGe/Si intermixing, the RTO temperature was kept low as compared to conventional temperatures typically reaching 1100 °C. A complete study on the formation of this $Si_{0.5}Ge_{0.5}$ layer has already been published.[18] The two steps-process with oxidation refers to the condensation process (sample A), while the direct deposition of $Si_{0.5}Ge_{0.5}$ refers to the epitaxy processes (samples B and C).

Cross section samples were prepared using a dual-beam FIB HELIOS 600 nanolab or tripod polishing followed by PIPS (Ar+) thinning. Transmission Electron Microscopy (TEM) was done using a FEI Tecnai G2, and a FEI Titan 80-300 with Cs corrector in TEM and Scanning Transmission Electron Microscopy (STEM) modes. EDS analysis and line profiles are carried out with the FEI Tecnai G2 using a probe size of approximately 3nm. The k factors of Si, Ge and O were measured on reference samples and allowed the determination of absolute concentrations. Geometric Phase Analysis (GPA) was done using Digitalmicrograph software on HRTEM and HRSTEM images.

X-ray measurements were performed using a nano-focused X-ray beam at beamline ID01 of the European Synchrotron Facility in Grenoble (France). The nano-beam was focused down to a 150 × 300 nm^2 (vertical × horizontal) spot size using a Fresnel Zone-plate (FZP) of

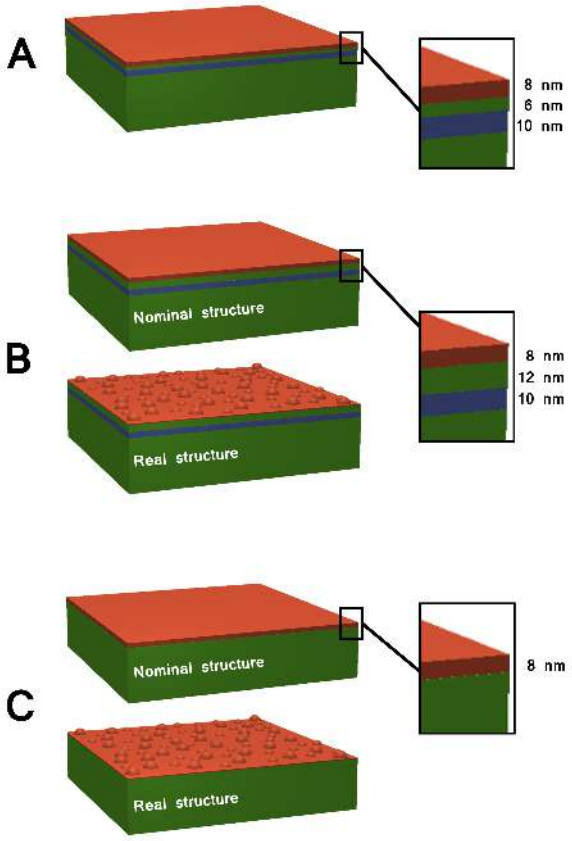


Figure 1: schematic representation of the three structures. Sample A is a 8 nm thick $Si_{0.5}Ge_{0.5}$ layer on a 6 nm thick Si on insulator (10 nm) obtained by oxidation of a thicker (30 nm) initial $Si_{0.8}Ge_{0.2}$ layer. Sample B is a 8 nm thick $Si_{0.5}Ge_{0.5}$ layer on a 12 nm SOI and sample C is a 8 nm thick $Si_{0.5}Ge_{0.5}$ layer on a bulk Si substrate. Sample B and C were both obtained by direct MBE deposition so the $Si_{0.5}Ge_{0.5}$ layer is not flat and islands formation occurred.

270 μm diameter and 80 nm outer-most zone width. The nano-diffraction experiments were carried out at a beam energy of 8 keV (wavelength λ of 1.55 Å). The diffracted beam was recorded with a two-dimensional (2D) MAXIPIX photon-counting detector, characterized by 516 $\times$ 516 pixels of 55 μm pixel size. The sample was mounted on a fast xyz scanning piezoelectric stage, with a lateral stroke of 100 μm and a resolution of 2 nm.

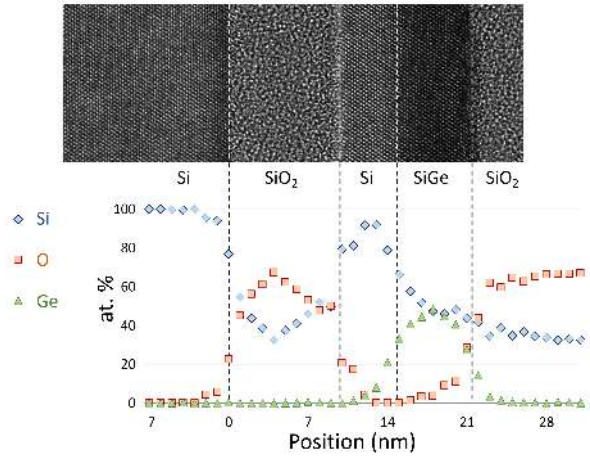


Figure 2: TEM EDS profile of sample A, and the corresponding HRTEM image identical to the one in Fig. 3.

Results

First the composition of the SiGe layers obtained by the three different processes was measured by semi-quantitative EDS. We show here the in-depth line profile of Si, Ge and O only for sample A (Fig. 2). A similar composition close to $x = 0.50 \pm 0.05$ was found in the three samples. In the present case (sample A, condensation process), the $Si_{0.5}Ge_{0.5}$ rests on top of a 6 nm thin layer of pure Si remaining from the initial UT-SOI. The interface between the two layers ($Si_{0.5}Ge_{0.5}$/Si) is very abrupt and is lower or equal to the resolution limit of EDS. The latter is limited by probe size and fluorescence effects and can be estimated to 3 nm.

Fig. 3 shows cross-section TEM images of the three structures. Sample B and C both exhibit island and/or dislocations in the $Si_{0.5}Ge_{0.5}$ layer. Defects are highlighted in the case of sample B in the higher magnification image shown in the insert. On a semi-infinite silicon substrate such as sample C, the critical thickness for island nucleation (h_{3D}) is evaluated in our experimental conditions to 2 nm (see results below) and slightly larger for dislocations nucleation (h_c). Both are much lower than the deposited thickness. The results are then consistent with previous studies[22] and the morphologies and structures are explained by the biaxial strain relaxation. On the two substrates,

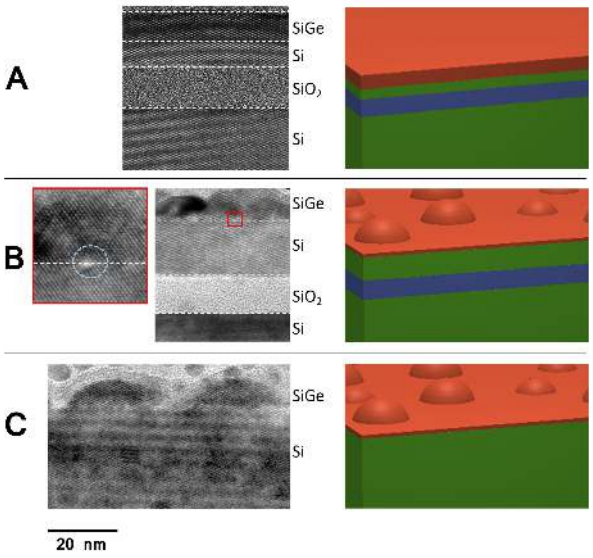


Figure 3: High resolution TEM cross-section images of the three structures A, B and C. For each structure, the corresponding schematic representation similar to Fig. 1 is presented on the right. For sample B, an insert shows a higher magnification TEM image to highlight the presence of defects in the cristal.

the SiGe epitaxial layers evolve similarly, so an initial observation is that in spite of the small thickness (12nm) of the Si top layer, the relative compliance of UT-SOI is not sufficient to avoid 3D islands or dislocations in these experiments.

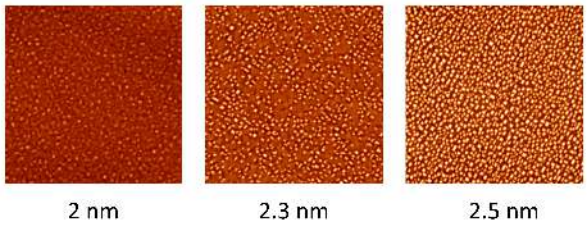


Figure 4: AFM images of a 2×2 μm^2 area of the surface of a respectively 2, 2.3 and 2.5 nm thick $Si_{0.5}Ge_{0.5}$ layer which were epitaxially deposited on silicon at 550 °C.

We then investigated more precisely the 2D-3D growth transition for $Si_{0.5}Ge_{0.5}$ deposition. In these experiments, the growth temperature was maintained at a lower value, typically 550 °C, in order to avoid the nucleation of dislocations. As attested by AFM images of three $Si_{0.5}Ge_{0.5}$ layers with h=2, 2.3 and 2.5 nm, the 2D-3D transition occurs at a critical thickness of approximately 2 nm (Fig. 4). One can easily observe the increasing density of small islands from h=2.3 and h=2.5 nm while only pre-pyramids are observed at h=2 nm. It is the nucleation of these pre-pyramids which attests the onset of the 2D-3D growth transition.[23]

In contrast, neither dislocations nor islands could be observed on sample A obtained in similar experimental conditions *via* the two steps process. An even more intriguing result is that while critical thicknesses of both island nucleation and dislocation nucleation are largely overcomed, the $Si_{0.5}Ge_{0.5}$ layers about 8 nm thick remain totally flat and free of extended defects.

In order to address this question we undertook a detailed study of the strain in the different samples using geometric phase analysis (GPA) on TEM images[24] and X-Ray diffraction.

When applied to the very flat and uniform layer of sample A, the GPA method provided accurate measurements while it was made difficult by the presence of islands and dislocations that relieve inhomogeneously the strain in samples B and C.

Fig. 5 shows GPA analysis of a TEM image of sample A. The HRTEM image analyzed is shown on Fig. 5 a. Fig. 5 b shows the corresponding GPA image of the deformation along in-plane x axis. No variation of the lattice parameter could be observed between the silicon substrate, the UT-SOI and the $Si_{0.5}Ge_{0.5}$ layer. This accounts for a fully biaxially strained $Si_{0.5}Ge_{0.5}$/UT-SOI, having a lattice parameter aligned to that of the relaxed Si and without any strain sharing between the Si and SiGe membranes. Along the out-of-the-plane y axis, the SiGe lattice parameter is distorted following Poisson's law.

We name $a(x)$ the lattice parameter of a fully relaxed $Si_{1-x}Ge_x$. When the SiGe is epitaxially grown on silicon, the lattice is deformed and we name b the in-plane lattice parameter (equal to the silicon lattice parameter a_{Si}), and $c(x)$ the out-of-the-plane lattice parameter resulting from the tetragonal deformation dictated by Poisson's law. The lattice deformation under bi-axial strain is given by[25] :

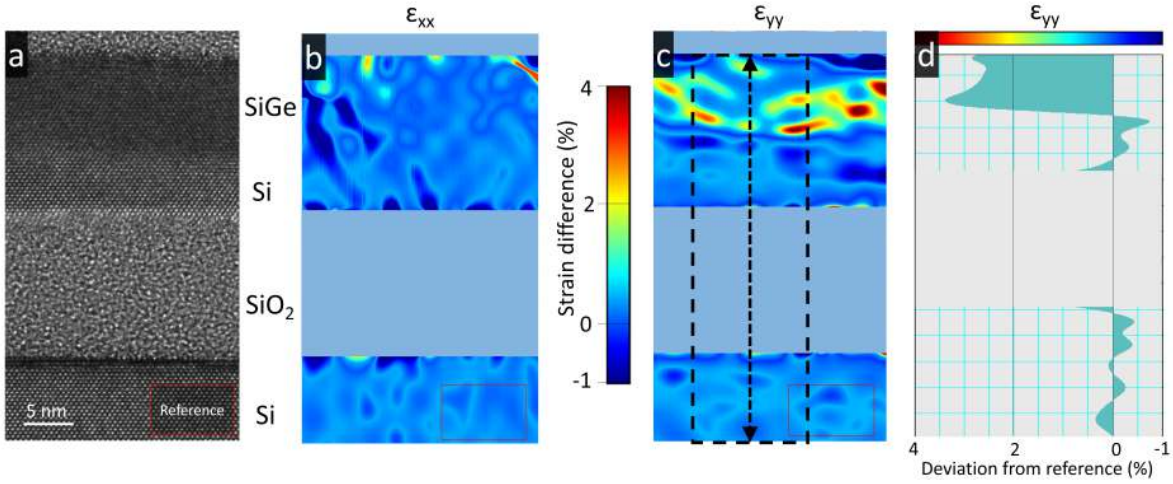


Figure 5: TEM cross-section image of sample A (a) and geometric phase analysis of the image along x (horizontal) axis (b) and y (vertical) axis (c). GPA is irrelevant in the SiO_2 part of the image and was masked to improve clarity. (d) is a line profile along y (vertical) axis from GPA image (c) and summed over 250 pixels. Corresponding area is marked by a black dashed rectangle on GPA image (c). Reference for the lattice deformation was taken in the red rectangle area indicated on the STEM image (a) and on both GPA images (b and c). The color scale for GPA images is indicated along the axis of the plot (d).

$$a(x) = (c(x) + bP)/(1 + P), \qquad (1)$$

with $P = \frac{2\nu}{1-\nu}$, ν being Poisson's ratio. The lattice parameter of relaxed $Si_{x1-}Ge_x$ can be calculated from a_{Si} and a_{Ge} (lattice parameters of pure relaxed Si and pure relaxed Ge respectively):[26]

$$a(x) = 0.02733x^2 + 0.1992x + 5.431 \qquad (2)$$

On the GPA image representing the deformation along out-of-the-plane y axis (Fig. 5 c), it is clear that the lattice parameter in the $Si_{0.5}Ge_{0.5}$ layer is higher than the one in Si. As evidenced on the plot (d), the difference is approximately 3 % .Since the composition of this layer is known (50 % Ge) and thanks to relations 1 and 2, we can deduce a corresponding 3.4 % out-of-the-plane expected expansion, resulting from the bi-axial in-plane compressive strain between the $Si_{0.5}Ge_{0.5}$ and Si layers. The slight difference with the GPA measurements (4 %) is attributed to the imprecision of this technique in the determination of stress and strain values. An important issue with GPA measurements is also the very small size of the surface measured which does not give a statistical representation of the full sample. More global and accurate information can be provided by X-ray diffraction experiments.

Figures. 6a,b,c show reciprocal space maps (RSMs) around **004** Si and SiGe Bragg peaks on the three samples (respectively A, B and C) and a RSM around **115** Si and SiGe Bragg peaks on the sample A (Fig. 6a, right panel). The intensity attributed to the SiGe layer has been circled in black in all RSMs and the expected Q_z positions for the Si and pseudomorphic $Si_{0.5}Ge_{0.5}$ layer on Si are indicated by horizontal dashed lines. RSMs around **004** reflections give information about out-of-plane lattice parameters of Si and SiGe while the RSM around **115** reflections shows information about both the in plane and the out-of-plane lattice parameters.

For the three samples, the RSMs around **004** Si and SiGe reflections exhibit a sharp intense peak centred at $Q_z = 4.62\,\text{Å}^{-1}$ attributed to the Si substrate. In samples A and B, the SOI system is slightly twisted from the Si substrate as evidenced by the small difference in Q_y between

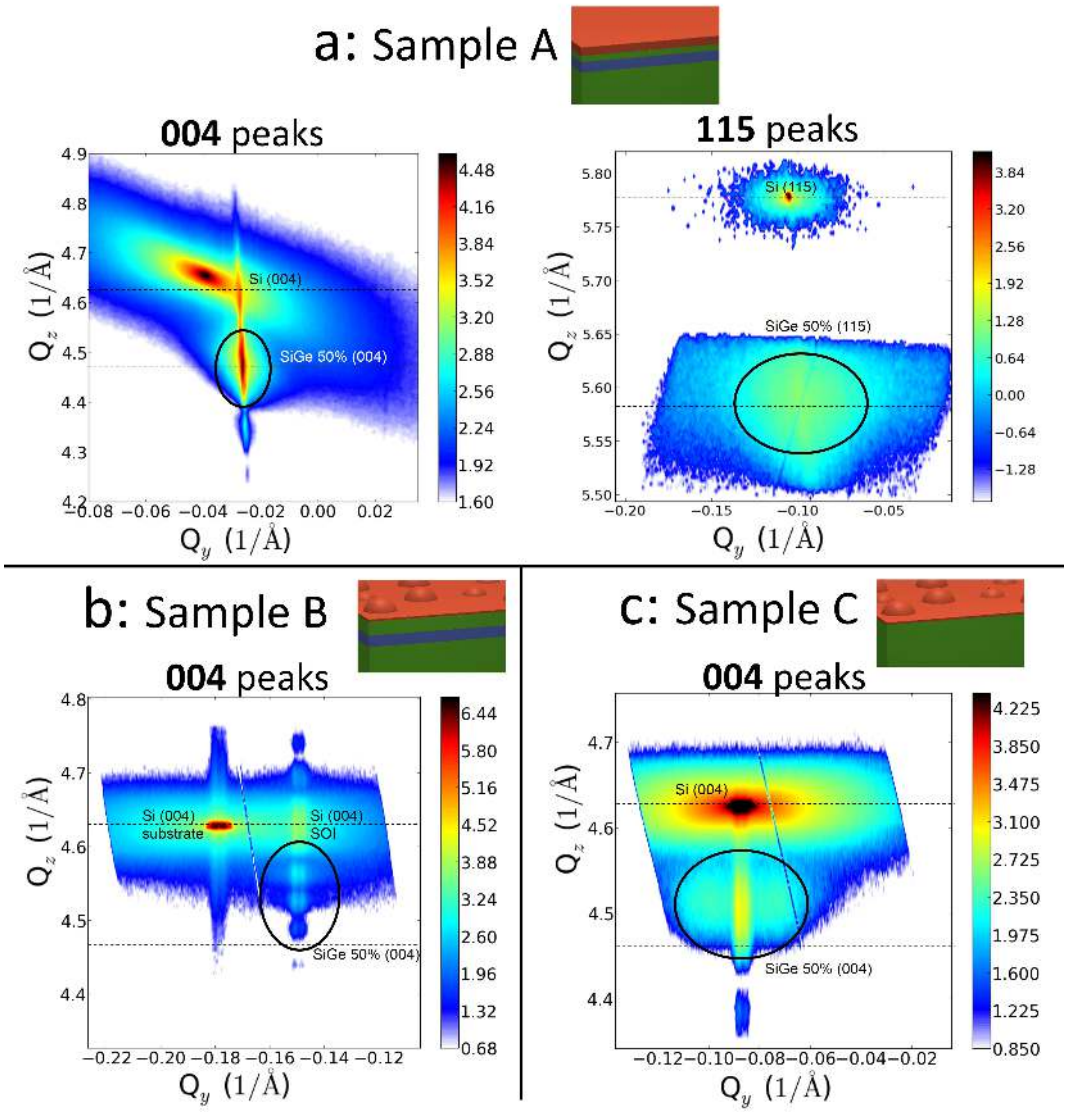


Figure 6: (a): Reciprocal space maps (RSMs) around **004** (left panel) and **115** (right panel) Si and SiGe Bragg peaks of sample A. (b) and (c): RSMs around **004** Si and SiGe Bragg peaks of respectively samples B and C.

the peaks of the Si top-SOI layer and the Si substrate on RSMs (see Fig. 6a, left panel and b). The peak of the Si_xGe_{1-x} layer is broader and positioned at $Q_z = 4.47\,\text{Å}^{-1}$ for sample A and $Q_z = 4.51\,\text{Å}^{-1}$ for sample C. It is virtually invisible for sample B, because of thickness fringes coming from the 12 nm thick silicon layer of the SOI.

On the RSM around **115** (see Fig. 6a, right panel), the peak of the SiGe layer is positioned at the same Q_y as the peak of the Si substrate. This confirms that the SiGe layer is pseudomorphic - *i.e.* has the same in-plane lattice parameter as the Si substrate.

From the Q_z coordinates of the peaks, we can deduce the lattice parameters along the out-of-plane axis for Si and SiGe and then calculate a difference of lattice parameter (Δa_z).

For sample A using the **004** RSM (see Fig. 6a, left panel), we find a difference of $\Delta a_z = 3.5$ % and using the **115** RSM (see Fig. 6a, right panel), a difference of $\Delta a_z = 3.68$ %. These distorsions correspond (following Equations 1 and 2) to a concentration in Si of respectively 52.2 % and 50.1 %, in good agreement with the 50 % value determined by EDS (Fig. 2).

For sample C using the **004** RSM (see Fig. 6c), we find a noticeably smaller value of

$\Delta a_z = 2.6$ %. This smaller strain is representative of a partial relaxation of the $Si_{0.5}Ge_{0.5}$ layer in agreement with the presence of dislocations and islands evidenced in Fig. 3.

For sample B (see Fig. 6b), while an accurate position of the SiGe peak along the z-axis could not be determined, a bright diffuse intensity is attributed to SiGe at a Q_z position larger than 4.5 $Å^{-1}$, which is again representative of a partial relaxation exactly like in the case of sample C.

We did not record RSMs around **115** reflections for sample B and C, but the difference in Q_z between the peak of the SiGe and the one of the Si visible on the **004** RSMs shows the partial relaxation of the SiGe.

These measurements already show that the strain of the SiGe layers obtained by direct deposition (on Si and on SOI) is completely different from the one with the two-step deposition/condensation process.

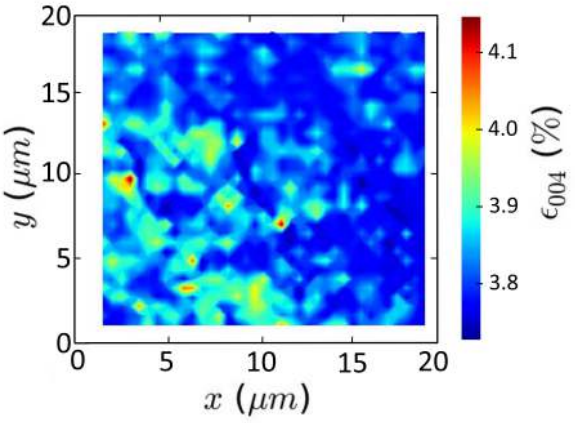


Figure 7: Map of a region of 20 × 20 μm^2 of the strain of the **004** planes of the SiGe layer for sample A. The strain is calculated with strain-free silicon as a reference (a_{Si}=5.4309 Å).

Using the focused x-ray beam, a mapping of a 20 × 20 μm^2 region of sample A was performed using the quicK continuous Mapping (K-Map) technique developed at the ID01 beamline.[27] Fig. 7 show a map of the strain on the (004) planes of the SiGe in this region. The origin of the strain values is taken for strain-free silicon. The map shows an average strain of about 3.85±0.05 % on large areas (20 × 20 μm^2) with low variations, which reflects a very good homogeneity over the entire region. This average strain corresponds to a $Si_{0.47}Ge_{0.53}$ alloy fully biaxially strained on Si substrate. This result is in very good agreement with the electron microscopy results. It confirms the absence of relaxation of the $Si_{0.5}Ge_{0.5}$ layer over large areas and probably over the entire sample.

Discussion

In summary, we have compared the morphological and structural evolution of $Si_{0.5}Ge_{0.5}$ epitaxial layers obtained by direct deposition on Si and on SOI and by a two-step deposition/condensation process. It should first be noted that the Si-top SOI layer is in principle sufficiently thin (12 nm) to produce a significant increase of the critical thickness of misfit dislocations nucleation as would predict the effect of the substrate compliance.[8] The experiments were then well suited to determine the compliant effect of SOI substrate.

In spite of that, it is found that the relaxation of $Si_{0.5}Ge_{0.5}$ is similar on bulk Si and SOI. This first reveals that the SiO_2/Si interface is rigid as discussed below. In both cases, relaxation is accompanied by both the growth of 3D islands and the introduction of misfit dislocations at the SiGe/Si interface. Tensile strain in the Si-top layer, as predicted for a sufficiently thin compliant substrate, has not been observed either by GPA or by X-ray diffraction.

In addition to that, even in sample A obtained *via* deposition/condensation (where the $Si_{0.5}Ge_{0.5}$ layer after condensation is much thicker and unrelaxed), the amount of strain in the Si-top layer was also too low to be observed. These results confirm that at this temperature (750 °C), the SiO_2/Si interface is fully rigid and the SOI does not behave as a compliant substrate for the epitaxial growth of SiGe.

In this last case, the large increase of the critical thickness for an epitaxial overlayer i.e. for both the 2D-3D growth transition and dislocations nucleation is then only attributable to the deposition followed by condensation process. Indeed with this process, the 8nm-thick

$Si_{0.5}Ge_{0.5}$ layer is still flat and fully strained as attested by both GPA and X-Ray diffraction measurements. In similar conditions, the same SiGe layers obtained by direct deposition, exhibit 3D islands and are partially relaxed by misfit dislocations.

The delay of the nucleation of 3D islands in sample A is easily understood by the presence of the SiO_2 cap layer which fully inhibits the surface diffusion at the $Si_{0.5}Ge_{0.5}$ top surface and thus prohibits the nucleation of islands.

The increase of the critical thickness of dislocation nucleation is more difficult to understand. Indeed, it should be noticed that in spite of the extensive literature on dislocations, the nucleation mechanism is extremely difficult to observe and then the nature of dislocation sources remains unknown. Various mechanisms have been suggested to favor the nucleation of dislocations, such as the presence of surface steps, surface dislocation loops, point defects, extended defects, interfacial impurities.[28,29]

The presence of the SiO_2 cap layer could inhibit the nucleation of dislocations. However, while surface mechanisms prevail in various heteroepitaxial systems, they are commonly considered as negligible in SiGe/Si.[30]

In this system, the source of dislocations commonly reported is the density of point defects and their ability to nucleate clusters.[31–35] In our experimental conditions, the SiGe layers are subjected to thermal oxidation which is known to induce silicon self-interstitial (I's) injection into the subsurface.[17] So, in the whole SiGe/SOI system considered, the density of self-interstitials is much larger than in conventional epitaxial systems. We suggest that this large density of I's could be at the origin of the strengthening of the SiGe layer. The increase of the critical thickness of nucleation of dislocations would then be attributed to a mechanism similar to Cottrel atmosphere in face-centered cubic (FCC) metals.[36]

Conclusions

In conclusion, we compared SiGe membranes fabricated by three different processes: direct deposition of $Si_{0.5}Ge_{0.5}$ either on Si(001) nominal substrate or on UT-SOI, and deposition of SiGe with low Ge concentration on silicon on insulator followed by Ge enrichment by condensation.

In spite of the very thin top Si layer of the UT-SOI, no compliance effect was observed for the sample of $Si_{0.5}Ge_{0.5}$ deposited on UT-SOI. Instead, we observed the same relaxation by island nucleation and dislocation nucleation as on Si(001) nominal substrate.

We show that the formation of 8 nm-thick fully strained Ge rich layers free of defects with flat surface is only possible by the two-steps epitaxy/condensation process. We demonstrate that this process enables the total inhibition of the morphological instability, together with the hindering of dislocations for a $Si_{0.5}Ge_{0.5}$ thickness of 8 nm, which is much larger than the ones commonly obtained by direct deposition. We verify that the $Si_{0.5}Ge_{0.5}$ layer is fully strained and homogeneous over large areas. This remarkable stability could be explained by the injection of self-interstitials in the GRL during the condensation even if a reduced surface diffusion at the SiO_2/SiGe interface could not be ruled out. The results can be generalized to different systems and we think that this work will promote and expand possibilities on a wide variety of devices.

Acknowledgement This work has been carried out thanks to the support of the NANOALLIANCE project.

References

(1) Tezuka, T.; Moriyama, Y.; Nakaharai, S.; Sugiyama, N.; Hirashita, N.; Toyoda, E.; Miyamura, Y.; ichi Takagi, S. Lattice Relaxation and Dislocation Generation/Annihilation in SiGe-On-Insulator Layers During Ge Condensation Process. *Thin Solid Films* **2006**, *508*, 251 – 255, Proceedings of the Fourth International Conference on Silicon Epitaxy and Heterostructures (ICSI-4)ICSI-4Proceedings of the Fourth International

Conference on Silicon Epitaxy and Heterostructures (ICSI-4).

(2) Littlejohns, C. G.; Nedeljkovic, M.; Mallinson, C. F.; Watts, J. F.; Mashanovich, G. Z.; Reed, G. T.; Gardes, F. Y. Next Generation Device Grade Silicon-Germanium on Insulator. *Sci. Rep.* **2015**, *5*, 8288.

(3) Park, S. B.; Kim, Y. W.; Ko, Y. G.; Kim, K. I.; Kim, I. K.; Kang, H.-S.; Yu, J. O.; Suh, K. P. A 0.25–μm, 600–MHz, 1.5–V, Fully Depleted SOI CMOS 64-bit Microprocessor. *IEEE J. of Solid-State Circuits* **1999**, *34*, 1436–1445.

(4) Park, J.-T.; Colinge, J. P. Multiple–Gate SOI MOSFETs: Device Design Guidelines. *IEEE Transactions on Elec. Devices* **2002**, *49*, 2222–2229.

(5) Chau, R.; Kavalieros, J.; Doyle, B.; Murthy, A.; Paulsen, N.; Lionberger, D.; Barlage, D.; Arghavani, R.; Roberds, B.; Doczy, M. A 50nm Depleted-Substrate CMOS Transistor (DST). Electron Devices Meeting, 2001. IEDM '01. Technical Digest. International. 2001; pp 29.1.1–29.1.4.

(6) Bin Yu et al., FinFET Scaling to 10nm Gate Length. Electron Devices Meeting, 2002. IEDM '02. International. 2002; pp 251–254.

(7) Colinge, C. A.; Byun, K. Y.; Ferain, I. P.; Yu, R.; Goorsky, M. In *Semiconductor-On-Insulator Materials for Nanoelectronics Applications*; Nazarov, A., Colinge, J.-P., Balestra, F., Raskin, J.-P., Gamiz, F., Lysenko, V., Eds.; Springer Berlin Heidelberg: Berlin, Heidelberg, 2011; Chapter Low-Temperature Fabrication of Germanium-on-Insulator Using Remote Plasma Activation Bonding and Hydrogen Exfoliation, pp 31–46.

(8) Berbezier, I.; Aqua, J.-N.; Aouassa, M.; Favre, L.; Escoubas, S.; Gouyé, A.; Ronda, A. Accommodation of SiGe Strain on a Universally Compliant Porous Silicon Substrate. *Phys. Rev. B* **2014**, *90*, 035315.

(9) Lo, Y. H. New Approach to Grow Pseudomorphic Structures over the Critical Thickness. *Appl. Phys. Lett.* **1991**, *59*, 2311–2313.

(10) Ayers, J. Compliant Substrates for Heteroepitaxial Semiconductor Devices: Theory, Experiment, and Current Directions. *J. of Electronic Mat.* **2008**, *37*, 1511–1523.

(11) Aqua, J.-N.; Favre, L.; Ronda, A.; Benkouider, A.; Berbezier, I. Configurable Compliant Substrates for SiGe Nanomembrane Fabrication. *Crystal Growth & Design* **2015**, *15*, 3399–3406.

(12) Pei, C. W.; Héroux, J. B.; Sweet, J.; Wang, W. I.; Chen, J.; Chang, M. F. High Quality GaAs Grown on Si-On-Insulator Compliant Substrates. *J. of Vac. Sci. & Tech. B* **2002**, *20*, 1196–1199.

(13) Powell, A. R.; Iyer, S. S.; LeGoues, F. K. New Approach to the Growth of Low Dislocation Relaxed SiGe Material. *Appl. Phys. Lett.* **1994**, *64*, 1856–1858.

(14) Yang, Z.; Guarin, F.; Tao, I. W.; Wang, W. I.; Iyer, S. S. Approach to Obtain High Quality GaN on Si and SiC on Silicon-On-Insulator Compliant Substrate by Molecular-Beam Epitaxy. *J. of Vac. Sci. & Tech. B* **1995**, *13*, 789–791.

(15) Boureau, V.; Benoit, D.; Warot, B.; Hytch, M.; Claverie, A. Strain/Composition Interplay in Thin SiGe Layers on Insulator Processed by Ge Condensation. *Mat. Sci. in Semicon. Proc.* **2016**, *42, Part 2*, 251 – 254, E-MRS Spring Meeting 2015 Symposium Z: Nanomaterials and processes for advanced semiconductor {CMOS} devices.

(16) Rehder, E. M.; Inoki, C. K.; Kuan, T. S.; Kuech, T. F. SiGe Relaxation on Silicon-On-Insulator Substrates: An Experimental and Modeling Study. *J. of Appl. Phys.* **2003**, *94*, 7892–7903.

(17) Napolitani, E.; Di Marino, M.; De Salvador, D.; Carnera, A.; Spadafora, M.; Mirabella, S.; Terrasi, A.; Scalese, S. Silicon Interstitial Injection During Dry Oxidation of SiGe/Si Layers. *J. Appl. Phys.* **2005**, *97*, 036106.

(18) Thomas David et al., Kinetics and Energetics of Ge Condensation in SiGe Oxidation. *The J. of Phys. Chem. C* **2015**, *119*, 24606–24613.

(19) Aspar, B.; Bruel, M.; Moriceau, H.; Maleville, C.; Poumeyrol, T.; Papon, A.; Claverie, A.; Benassayag, G.; Auberton-HervÃĺ, A.; Barge, T. Basic Mechanisms Involved in the Smart-Cut Process. *Microelec. Eng.* **1997**, *36*, 233 – 240, Proceedings of the biennial conference on Insulating Films on Semiconductors.

(20) Abbarchi, M.; Naffouti, M.; Vial, B.; Benkouider, A.; Lermusiaux, L.; Favre, L.; Ronda, A.; Bidault, S.; Berbezier, I.; Bonod, N. Wafer Scale Formation of Monocrystalline Silicon-Based Mie Resonators via Silicon-on-Insulator Dewetting. *ACS Nano* **2014**, *8*, 11181–11190, PMID: 25365786.

(21) Naffouti, M.; David, T.; Benkouider, A.; Favre, L.; Ronda, A.; Berbezier, I.; Bidault, S.; Bonod, N.; Abbarchi, M. Fabrication of Poly-Crystalline Si-Based Mie Resonators via Amorphous Si on SiO_2 Dewetting. *Nanoscale* **2016**, *8*, 2844–2849.

(22) Berbezier, I.; Descoins, M.; Ismail, B.; Maaref, H.; Ronda, A. Influence of Si(001) Substrate Misorientation on Morphological and Optical Properties of Ge Quantum Dots. *J. of Appl. Phys.* **2005**, *98*, 063517.

(23) Ramalingam, G.; Floro, J. A.; Reinke, P. Three-Dimensional Nanostructures on Ge/Si(100) Wetting Layers: Hillocks and pre-Quantum Dots. *J. of Appl. Phys.* **2016**, *119*, 205305.

(24) Snoeck, E.; Warot, B.; Ardhuin, H.; Rocher, A.; Casanove, M. J.; Kilaas, R.; Hètch, M. J. Quantitative Analysis of Strain Field in Thin Films from HRTEM Micrographs. *Thin Solid Films* **1998**, *319*, 157–162.

(25) Zaumseil, P.; Kozlowski, G.; Schubert, M. A.; Yamamoto, Y.; Bauer, J.; Schülli, T. U.; Tillack, B.; Schroeder, T. The Role of SiGe Buffer in Growth and Relaxation of Ge on Free-Standing Si(001) Nano-Pillars. *Nanotechnology* **2012**, *23*, 355706.

(26) Dismukes, J. P.; Ekstrom, L.; Paff, R. J. Lattice Parameter and Density in Germanium-Silicon Alloys. *The J. of Phys. Chem.* **1964**, *68*, 3021–3027.

(27) Gilbert André Chahine et al, Imaging of Strain and Lattice Orientation by Quick Scanning X-ray Microscopy Combined with Three-Dimensional Reciprocal Space Mapping. *J. of Appl. Crystallogr.* **2014**, *47*, 762–769.

(28) Pichaud, B.; Burle, N.; Texier, M.; Alfonso, C.; Gailhanou, M.; Thibault-PÃľnisson, J.; Fontaine, C.; Vdovin, V. I. Dislocation Nucleation in Heteroepitaxial Semiconducting Films. *physica status solidi (c)* **2009**, *6*, 1827–1835.

(29) Vdovin, V. I. Mechanisms of Dislocation Generation in Si Structures with Strained Layers: Intrinsic Point Defects in Dislocation Nucleation. *J. of Surf. Investig. X-ra.* **2009**, *3*, 598–603.

(30) Rzaev, M.; Schäffler, F.; Vdovin, V.; Yugova, T. Misfit Dislocation Nucleation and Multiplication in Fully Strained SiGe/Si Heterostructures under Thermal Annealing. *Mat. Sci. in Semicon. Proc.* **2005**, *8*, 137 – 141, Proceedings of the Second International SiGe Technology and Device Meeting (ISTDM 2004) Kleist-Forum, Frankfurt (Oder), Germany, 16 - 19 May, 2004: From Materials and Process Technology to Device and.

(31) Eaglesham, D. J.; Kvam, E. P.; Maher, D. M.; Humphreys, C. J.; Bean, J. C.

Dislocation Nucleation Near the Critical Thickness in GeSi/Si Strained Layers. *Philos. Mag. A* **1989**, *59*, 1059–1073.

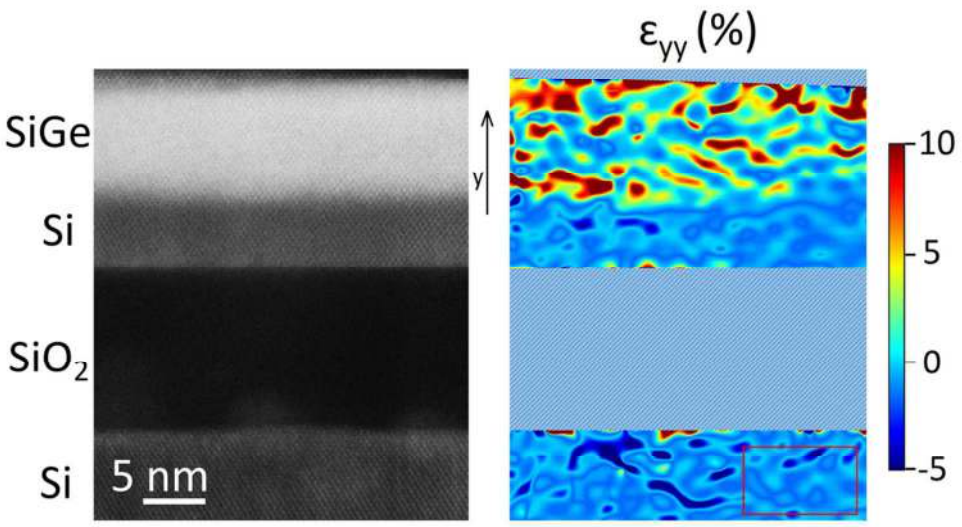
(32) Bolkhovityanov, Y.; Deryabin, A.; Gutakovskii, A.; Sokolov, L. Mechanism of Induced Nucleation of Misfit Dislocations in the Ge-on-Si(0 0 1) System and its Role in the Formation of the Core Structure of Edge Misfit Dislocations. *Acta Materialia* **2013**, *61*, 617 – 621.

(33) Vdovin, V. I.; Mühlberger, M.; Rzaev, M. M.; Schäffler, F.; Yugova, T. G. Dislocation Structure Formation in SiGe/Si(001) Heterostructures with Low-Temperature Buffer Layers. *J. of Phys.: Cond. Matt.* **2002**, *14*, 13313.

(34) LeGoues, F. K.; Meyerson, B. S.; Morar, J. F. Anomalous Strain Relaxation in SiGe Thin Films and Superlattices. *Phys. Rev. Lett.* **1991**, *66*, 2903–2906.

(35) Hull, R.; Parvaneh, H.; Andersen, D.; Bean, J. C. Materials Genomics of Thin Film Strain Relaxation by Misfit Dislocations. *J. of Appl. Phys.* **2015**, *118*, 225306.

(36) Yu, Q.; Qi, L.; Tsuru, T.; Traylor, R.; Rugg, D.; Morris, J. W.; Asta, M.; Chrzan, D. C.; Minor, A. M. Origin of Dramatic Oxygen Solute Strengthening Effect in Titanium. *Science* **2015**, *347*, 635–639.



TOC graphic

47x26mm (600 x 600 DPI)