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A 0.35  $\mu\text{m}$  CMOS AM demodulator

Pietro M. Ferreira · Fernando A. P. Barúqui ·  
Antonio Petraglia

**Abstract** This paper presents a 0.35  $\mu\text{m}$  CMOS AM demodulator circuit. Design details, simulations and measurements results of the monolithic implementation of a highly accurate synchronous rectifier are shown. The circuit implements an envelope detector with a  $\pm 1.5$  V output swing on a 15 pF load. It dissipates 15 mW from a  $\pm 2.5$  V voltage supply, and presents  $\text{SNR} = 81$  dB measured at a  $\text{THD} = -40$  dB for an input signal having 100% modulation index.

**Keywords** AM demodulator · Integrated circuits ·  
Vibration detector · Ideal rectifier

## 1 Introduction

This paper advances the design of an AM demodulator, which is intended as part of a system-on-chip application, as shown in Fig. 1. In this application, an accelerometer picks up the vibration of a metallic structure and produces an electrical signal composed of amplitude modulated (AM) waveform embedded in noise.

The anti-aliasing filter is followed by a fully differential bandpass switched-capacitor filter working at

200 kHz, which rejects a large amount of noise and selects the desired frequency band. Its output is a sampled-and-held waveform, and hence must be applied to a reconstruction filter, so as to remove the undesired replicas of the bandpass signal produced by the switched-capacitor filter. The result is a 5 kHz baseband component modulated in amplitude around 25 kHz with  $\pm 1.5$  V swing. Operating as an envelope detector with a rectifier and a low-pass filter [1], the AM demodulator extracts and delivers the desired signal to a 15 pF capacitive load. This signal is finally converted into a digital bit stream by an off-chip A/D converter, and subsequently processed by a DSP, that obtains the signal properties that are of particular interest for the purposes of understanding and minimizing the causes of the structure vibration.

The AM envelope detector demodulator circuits are widely employed in a large variety of instrumentation applications, to which the one advanced in this paper can be easily adapted. This kind of demodulator is normally implemented by a simple diode and a RC filter. However, this procedure is not appropriate for low AM signal levels, because the diode has a threshold voltage that occasionally exceeds the input signal amplitude. The monolithic implementation proposed here circumvents this drawback by using a synchronous full wave rectifier.

The AM demodulator is basically a peak detector followed by a rectifier and a lowpass filter [1]. Figure 2 shows the AM demodulator block diagram. It uses a voltage comparator as the trigger circuit that controls the analog switches to achieve the synchronous full wave rectification. The synchronous rectifier output is connected to the IC pad, which has a capacitance of 15 pF. Therefore, a buffer circuit is needed to drive this load with a high signal voltage swing.

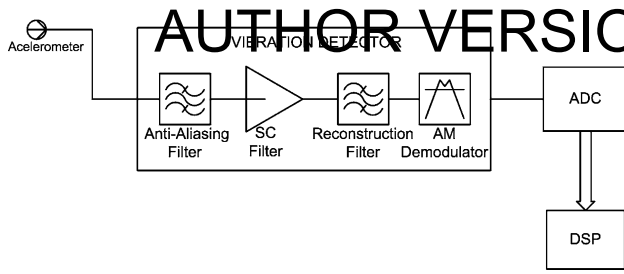


Fig. 1 Vibration detector system

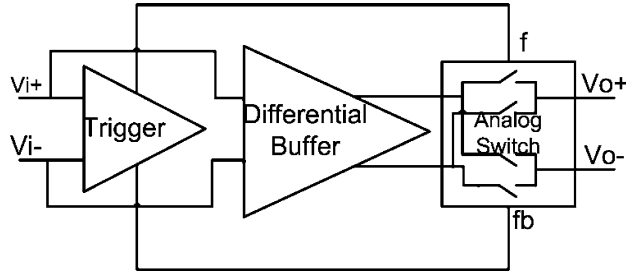


Fig. 2 AM demodulator architecture

This paper focuses on the IC design challenges of the above AM demodulator circuit. The circuit was implemented in a standard 0.35  $\mu\text{m}$  CMOS process, using a  $\pm 2.5$  V supply voltage. Simulation results, obtained with SPECTRE, are presented to verify the effectiveness of the proposed design approach. Finally, the measurement results are shown to verify the circuit performance in real working conditions.

The paper is organized as follows. Section 2 describes the circuit design. Section 3 shows simulation and measurements results for each circuit attaining the design specifications. Section 4 contains the main conclusions of this work.

## 2 AM demodulator design

The AM demodulator is basically a peak detector followed by a rectifier and a lowpass filter [1]. Since the frequency of the modulating signal is around 5 kHz, the time constant of the lowpass filter is 0.2 ms, which requires rather large component values. For this reason, the lowpass filter is implemented with discrete capacitors and resistors.

The envelope detection, after lowpass filtering, requires a rectifier with zero voltage threshold, because the sensor output signal level is smaller than the usual diode threshold voltages. To overcome this problem, the rectifier was designed as a highly precise synchronous rectifier employing an open loop operational transconductance amplifier (OTA), termed trigger in Fig. 2, and analog switches.

In order to drive the larger capacitor of the output pad, it is necessary to use a full differential voltage buffer. A number of buffer structures have been proposed in the literature [2–4]. Continuous effort has been employed to improve their linearity and dynamic range. Section 2.3 shows the design of a buffer that uses two cross-coupled input differential pairs, with large voltage signal swing and low THD. The unity voltage gain is achieved by internal current feedback, thereby avoiding external resistors and/or capacitors.

### 2.1 Trigger

The trigger circuit was implemented by an open loop differential OTA, as shown in Fig. 3. The OTA is implemented by a folded cascode stage with high gain for proper operation of the trigger circuit. In this application, the noise amount was filtered by the switched-capacitor filter, which selects the desired frequency band. However, if the noise could not be filtered then it will be necessary a comparator with hysteresis, adjusted by a positive feedback to improve the noise immunity. The differential input transistor pair has  $W = 36$  and  $L = 0.5$   $\mu\text{m}$ , which is the minimum length necessary for the differential gain and allowed by the chosen technology, using  $\pm 2.5$  V power supply.

The bias sections, shown in Fig. 3, was designed to bias the buffer with a current proportional to  $I_{bias}$ . To mirror this current,  $V_{B1}$  and  $V_{B3}$  are chosen to satisfy the following conditions to guarantee the circuit operation in the saturation region:

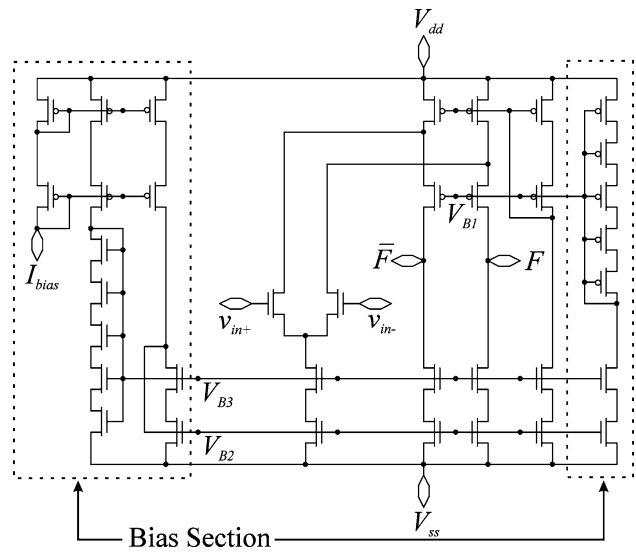


Fig. 3 Trigger schematic

$$\begin{cases} 2V_{ov} + V_{Tn} \leq V_{B3} \leq V_{ov} + 2V_{Tn}; & \text{for NMOS section} \\ V_{dd} - V_{ov} + 2V_{Tp} \leq V_{B1} \leq V_{dd} - 2V_{ov} + V_{Tp}; & \\ \text{for PMOS section} \end{cases} \quad (1)$$

where  $V_{ov}$  is the overdrive voltage, defined as  $|V_{GS} - V_{Tn,p}|$ . The threshold voltage of the NMOS and PMOS transistors are  $V_{Tn} = 0.74$  and  $V_{Tp} = -1$  V, respectively. The two bias circuits, each one implemented by 5 transistors connected in series generate  $V_{B3} = \sqrt{5}V_{ov} + V_{Tn}$  and  $V_{B1} = V_{dd} - \sqrt{5}V_{ov} + V_{Tp}$ , as shown in Fig. 3. As a result, the inequalities (1) are always satisfied, regardless of process variation effects, since the cascode current mirror and its bias circuit are simultaneously affected. The minimum output voltage is given by  $V_{oMIN} = \sqrt{5}V_{ov}$  and the adopted value is equal to 0.6 V, lower than  $V_{Tn}$ , in order to guarantee the turned off state of the NMOS switches. Therefore, the calculated value of  $V_{ov}$  is equal to 0.27 V and also satisfies the turned off state of the PMOS switches. Finally, the transistor dimensions are obtained by using the current-voltage relation for strong inversion operation,

$$I_D = \beta V_{ov}^2 / 2, \quad (2)$$

where  $\beta = k_p W/L$ . The ideal size was computed analytically, and adjusted by simulation using BSIM3V3 model. The sizes of the NMOS devices are  $W = 11$  and  $L = 1$   $\mu\text{m}$  with a bias current of 30  $\mu\text{A}$ . For the PMOS devices, the sizes are  $W = 64$  and  $L = 1$   $\mu\text{m}$  for the upper folded cascode transistors, with a bias current of 60  $\mu\text{A}$ , and  $W = 32$   $\mu\text{m}$  and  $L = 1$   $\mu\text{m}$  for the other ones, with a bias current of 30  $\mu\text{A}$ .

The outputs,  $F$  and  $\bar{F}$ , convey the information about the sign of the input signal, necessary to the switching scheme of the analog switches (see Fig. 2). The outputs are thus logic levels, whose values depend on the signal sign.

## 2.2 Analog switches

Figure 4 presents the schematic diagram of the analog switching circuit that performs zero-threshold signal rectification. Its input is provided by the buffer output. The analog switches perform the full wave rectification by multiplexing the incoming signal. This operation is carried out synchronously with the trigger phases ( $F$  and  $\bar{F}$ ).

If the signal sign is positive, phase  $F$  is high, and the analog switches connect  $V_{o+}$  to  $V_{DEM+}$  and  $V_{o-}$  to  $V_{DEM-}$ . If the signal sign is negative, phase  $F$  is low, and the analog switches connect  $V_{o+}$  to  $V_{DEM-}$ , and  $V_{o-}$  to  $V_{DEM+}$ . As a result,  $V_{DEM+}$  and  $V_{DEM-}$  are the positive and the negative full wave rectified output signal, respectively.

The dimensions (width and length) of the switch transistors were calculated considering a capacitive load of

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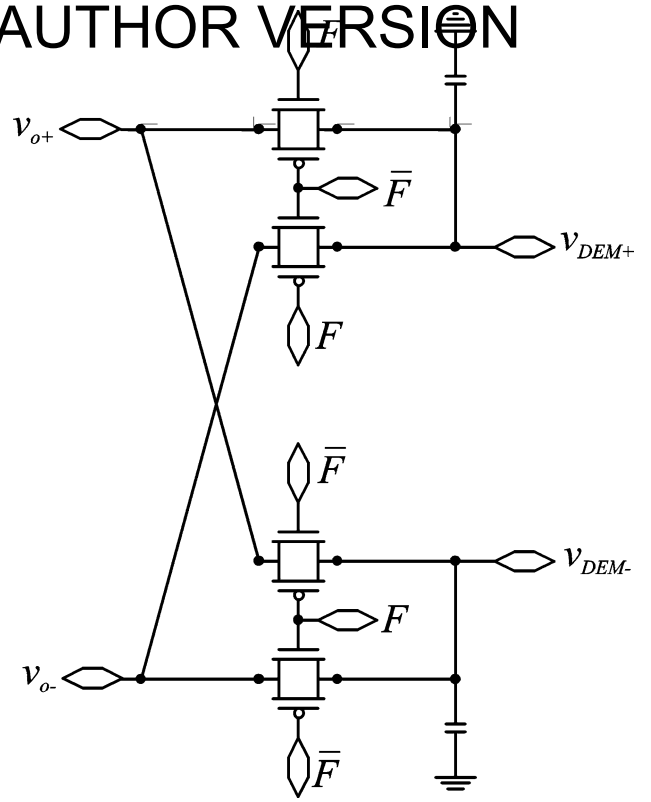


Fig. 4 Analog switches schematic

$C_L = 15$  pF and rise time of  $t_r \leq 30$  ns. The switch on-resistance ( $R_{DS}$ ) can be calculated by

$$t_r \approx 5 R_{DS} C_L, \quad (3)$$

where

$$R_{DS} = \frac{1}{k_p \frac{W}{L} V_{ov}} \quad (4)$$

is the channel resistance of the MOSFET at triode region. Using  $L = 0.5$   $\mu\text{m}$ ,  $t_r = 30$  ns and  $V_{ov} = 1.76$  V, we obtained  $V_{GD} = 2.5$  V ( $V_{GD} > V_t$  for triode) and  $W = 10$   $\mu\text{m}$  for both NMOS and PMOS devices.

## 2.3 Buffer

The differential unitary gain voltage buffer is implemented by an OTA. Similar configuration was presented in [2], except for the operational voltage amplifier used therein. The unitary gain feedback proposed in this paper is realized by an internal current feedback, as indicated in Fig. 5. The buffer was designed to handle a  $\pm 1.5$  V output swing and a capacitive load  $C_L = 15$  pF needed by the target application.

The basic idea of the buffer topology is shown in Fig. 6. The two identical differential pairs implement the input stage and the internal current feedback. The output stage is a folded cascode circuit, and exhibits high output impedance.

In the following preliminary analysis we neglect the parasitic capacitances. The input and output differential

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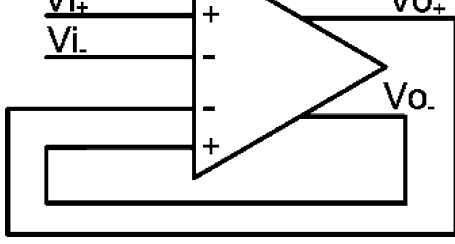


Fig. 5 Buffer architecture

voltages are defined as  $v_d = v_{in+} - v_{in-}$  and  $v_o = v_{o+} - v_{o-}$ , respectively. As will be shown below, the cross-coupled differential pair presents wide input voltage swing and highly linear transconductance  $g_{md}$ . So, the output currents  $i_{in}$  at the input differential pair and  $i_{int}$  at the internal current feedback differential pair can be written as

$$I_{in}(s) = g_{md}V_d(s) \quad (5)$$

and

$$I_{int}(s) = g_{md}V_o(s). \quad (6)$$

Assuming a capacitive load  $C_o$  at the output we can express the output differential voltage in the  $s$  domain as

$$V_o(s) = \frac{(I_{in}(s) - I_{int}(s))R_o}{sC_oR_o + 1}, \quad (7)$$

where  $R_o$  is the parasitic differential output resistance. From Eqs. 5–7 it can be easily shown that

$$V_o(s) = \frac{\frac{g_{md}R_o}{1+g_{md}R_o}}{s\frac{C_oR_o}{1+g_{md}R_o} + 1} V_d(s). \quad (8)$$

The term  $g_{md}R_o$  is the DC gain, and achieves high values for the folded cascode stage. As a result, from Eq. 8 we obtain the first-order transfer function approximation

$$H_1(s) = \frac{V_o(s)}{V_d(s)} \approx \frac{1}{s\frac{C_o}{g_{mo}} + 1} \quad (9)$$

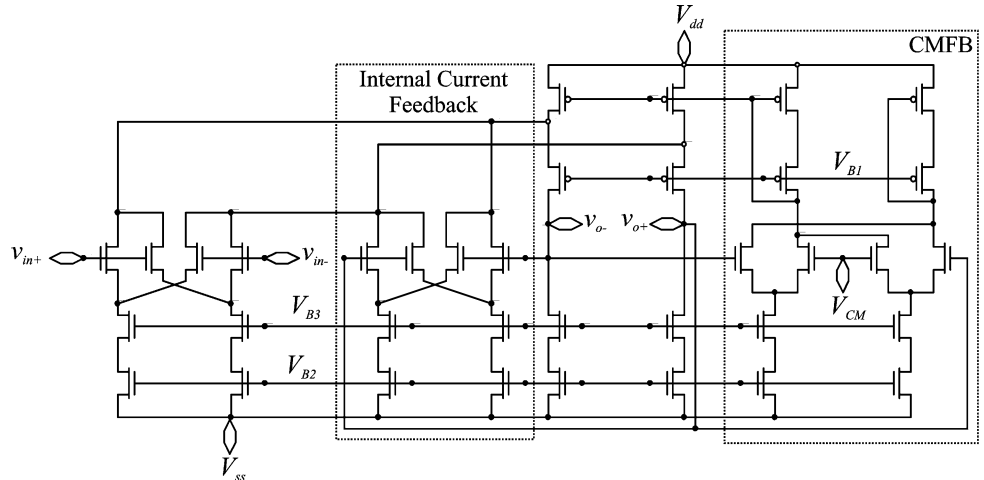
Note that  $g_{md}$  was replaced by  $g_{mo}$ , which is the buffer open-loop transconductance.

The buffer transfer function has a pole at  $g_{mo}/C_o$  and, for relatively low frequencies, the voltage gain is very close to one. A more detailed analysis shows that  $H(s)$  is actually a third-order function, and a second-order approximation would be performed to write  $H(s)$  by a two-pole transfer function, to suit hand calculations. The poles must be carefully allocated, according to the application. In this case, the non-dominant pole has been positioned at a frequency near one decade above the dominant one. The latter was placed at 2.5 MHz to handle dimensions greater enough to validate the transistor model approximations and to meet the integration process technology requirements.

In Fig. 6,  $V_{B1}$  and  $V_{B3}$  are bias voltages determined according to the bias circuit at the trigger scheme, and  $V_{B2}$  is the common mode feedback (CMFB) control voltage. The circuit used is a continuous-time CMFB network as discussed in [5]. The CMFB was implemented with two differential pairs comparing the output voltage with a reference voltage, in order to compensate the variations in the common mode voltage by changing the cascode bias current.

The conventional two-transistor symmetrical differential pair has shown poor linearity because  $g_m$  is strongly dependent on the input voltage. A notable increase in linearity can be obtained by using two asymmetrical and one symmetrical differential pair, as shown in [6, 7]. For the case of unitary gain buffers, the strong feedback guarantees low THD even if the input stage does not present high linearity. Therefore, in this paper we use only two asymmetrical differential pairs for each input stage (the input

Fig. 6 Buffer schematic



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differential pair and the internal current feedback differential pair), as shown in Fig. 6.

In the following design equations, the MOSFETs are assumed to operate in the saturation region and in strong inversion (Eq. 2). The partial transconductances for the MOSFETs  $a$  and  $b$  are given by  $g_{ma} = \partial i_d / \partial v_d$  and  $g_{mb} = \partial i_b / \partial v_d$ , respectively.

It is assumed that  $\beta_a > \beta_b$ , and  $g_{ma}$ ,  $g_{mb}$  are asymmetric with respect to the vertical axis at  $v_d = 0$ . The bias current  $I_s$  and the parameters  $\beta_a$  and  $\beta_b$  can be determined such that the total transconductance,  $g_{m_d}(v_d) = g_{ma}(v_d) + g_{mb}(v_d)$ , is equiripple inside the interval  $[-v_{dM}/2, +v_{dM}/2]$ , as illustrated in Fig. 7. This assumption leads to the following design equations:

$$I_s = 0.53 g_{m_d} v_{dM}, \quad (10)$$

$$\beta_a = 28.74 \frac{g_{m_0}}{v_{dM}}, \quad (11)$$

$$\beta_b = 3.04 \frac{g_{m_d}}{v_{dM}}, \quad (12)$$

where  $v_{dM}$  is the maximum differential voltage.

Numerical computations show that the worst THD value for both  $i_{in}$  and  $i_{int}$  is 2.34%, and is achieved when the input voltage is  $0.21 v_{dM} \sin(\omega t)$ .

Using  $L = 5 \mu\text{m}$  for both the input differential pair and for the internal current feedback differential pair, we obtain  $W_a = 66.7 \mu\text{m}$  from Eq. 11, and  $W_b = 7 \mu\text{m}$  from Eq. 12. The sizes of the CMFB differential pair devices are  $W = 40$  and  $L = 10 \mu\text{m}$ , in order to keep the output common mode voltage very close to the common mode reference, even at of maximum differential output voltage swing.

All current mirrors were calculated to meet the output signal voltage swing and the capacitive load ( $C_L$ ) specifications. The sizes of the NMOS devices are  $W = 110$  and  $L = 1 \mu\text{m}$ , with a bias current of  $300 \mu\text{A}$ . For the PMOS

devices, the sizes are  $W = 640$  and  $L = 1 \mu\text{m}$  for the upper folded cascode transistors, with a bias current of  $600 \mu\text{A}$ , and  $W = 320 \mu\text{m}$  and  $L = 1 \mu\text{m}$  for the other ones, with a bias current of  $300 \mu\text{A}$ .

## 3 Simulations and measurement results

The trigger clocks control the switching sequence of the CMOS switches, producing a highly precise synchronous rectifier. We used an external lowpass passive filter to detect the wrapped sine wave. Both the trigger and the switch circuits were tested under extreme operation conditions.

The buffer has a  $\pm 2.5 \text{ V}$  supply voltage and its power consumption was calculated by a demodulation operation simulation. For a signal swing of  $\pm 1.5 \text{ V}$ , the THD obtained by simulation is  $-60 \text{ dB}$ , computed with a  $5 \text{ kHz}$  sine wave input. The simulated signal swing is presented in Fig. 8. Its transconductance was calculated at the simulation for the maximum input signal swing. The buffer cut-off frequency estimated by simulations is  $2.5 \text{ MHz}$ . The results were obtained with SPECTRE simulator and the general characteristics of the designed buffer are summarized in Table 1.

The demodulator was tested for an input AM signal with carrier at  $25 \text{ kHz}$ , having  $1.5 \text{ V}$  amplitude, modulator signal at  $5 \text{ kHz}$  and modulation index of  $50\%$ . The circuit produces the resulting full wave rectification as shown in dashed line in Fig. 9, and the demodulated (baseband) signal is shown in solid line. This simulation includes the action of a lowpass filter externally connected to the circuit. The Fig. 10 presents the respective measurement results (full wave rectification in dashed line and demodulated signal in solid line), and, as can be observed, agrees closely with those of Fig. 9.

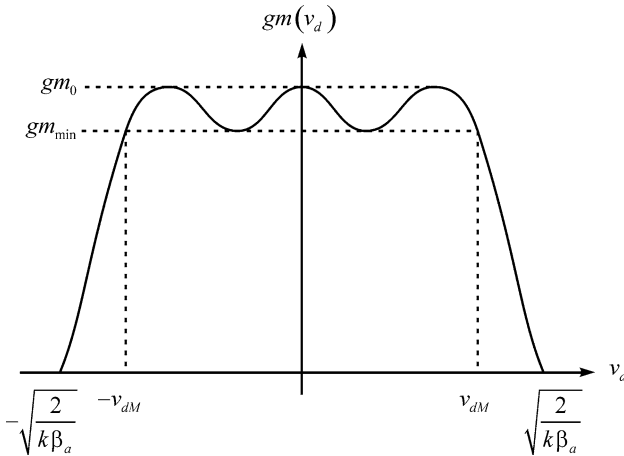


Fig. 7 Buffer transconductance characteristics

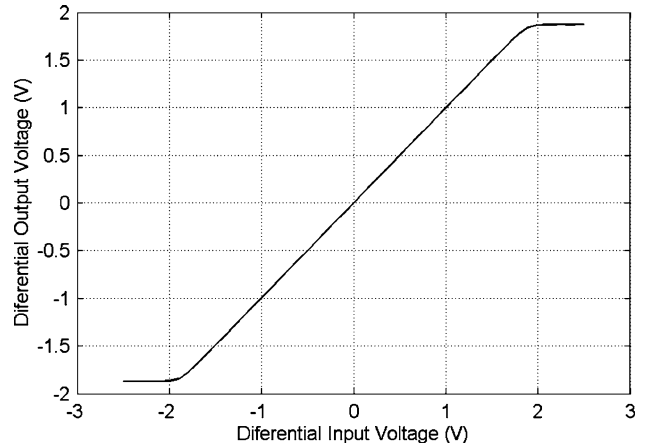
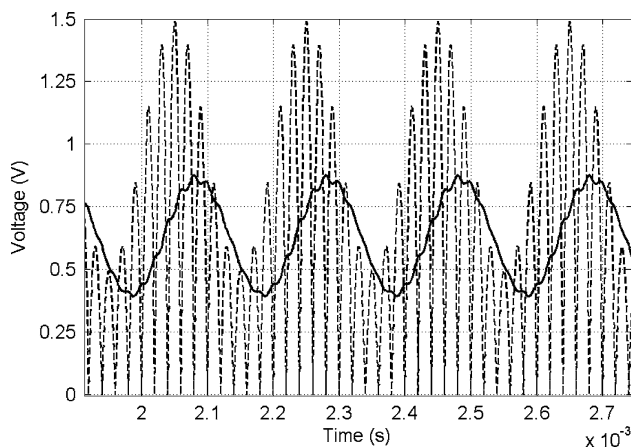


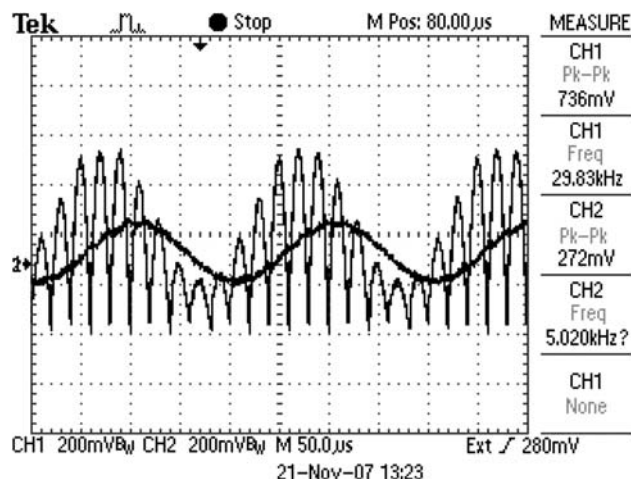
Fig. 8 Simulated buffer signal swing

**Table 1** Simulated buffer general characteristics

Parameter	Value
Power supply voltage	$\pm 2.5$ V
Total power consumption	16.3 mW
Total area consumption	0.026 mm <sup>2</sup>
Input and output voltage swing—peak to peak	$\pm 1.5$ V with THD = -60 dB
Transconductance	$83 \pm 7$ $\mu$ S

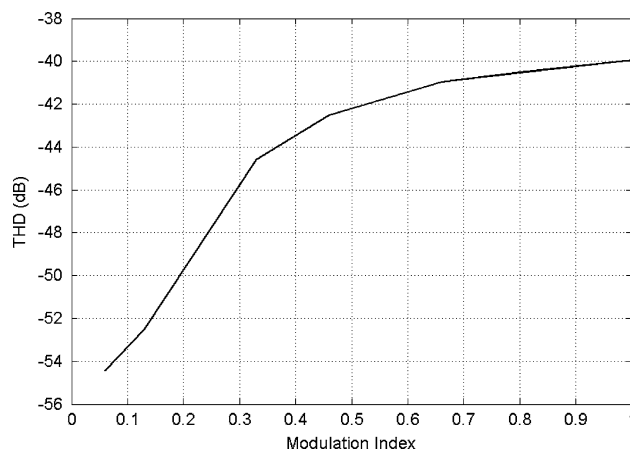


**Fig. 9** Simulated full wave rectification (broken line) and AM demodulation (solid line); both are in differential mode

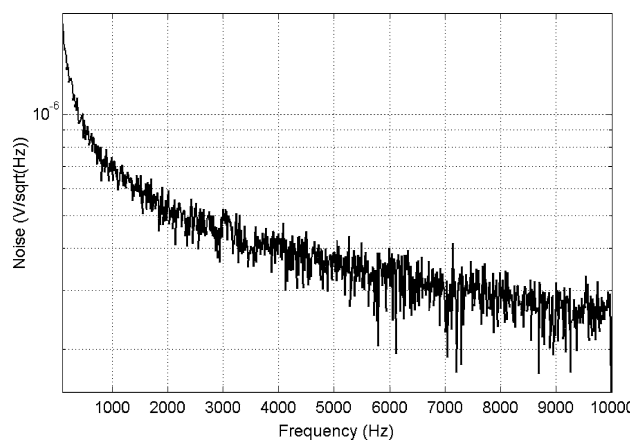


**Fig. 10** Measured full wave rectification and AM demodulation; both are the positive output

The AM demodulator distortion was characterized by applying an input modulated signal with the maximum signal swing and measuring the baseband THD versus its modulation index, as presented in Fig. 11. The input signal has 1.5 V amplitude and 25 kHz carrier, modulated with variable modulation index and 100 Hz baseband sine wave. Up to 10 harmonic components were considered to calculate the THD for each modulation index.



**Fig. 11** Measured baseband THD output signal for various modulation indexes input signal



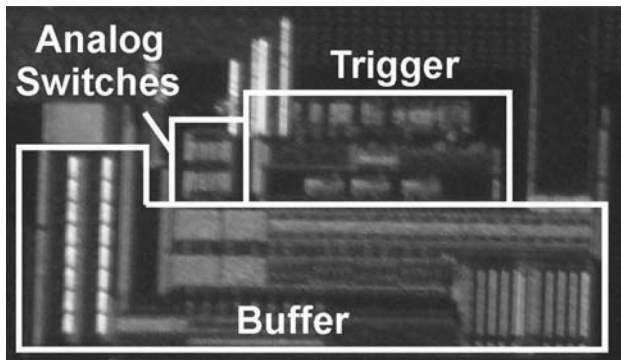
**Fig. 12** Measured circuit input voltage spectral noise density

The output total noise, measured in the frequency band from DC up to 10 kHz, is  $13.6 \mu$  V<sub>RMS</sub>. The measured output noise power spectral density is shown in Fig. 12. As a result the SNR = 81 dB was obtained for an input signal having 100% modulation index producing an output signal with THD = -40 dB. The power supply rejection ratio (PSRR) measured at 60 Hz is -50 dB, and measured at 120 Hz is -40 dB.

Finally, the measured total power consumption is 15 mW and its die area is 0.037 mm<sup>2</sup>, mostly occupied by the buffer circuit. Figure 13 displays the microphotograph of the AM demodulator. The key measured characteristics are summarized in Table 2.

## 4 Conclusions

We have presented an AM demodulator circuit, which is part of a system-on-chip application. The circuit was



**Fig. 13** AM demodulator microphotograph

**Table 2** AM demodulator measured results

Parameter	Value
Power supply voltage	$\pm 2.5$ V
Total power consumption	15 mW
Total area consumption	0.037 mm <sup>2</sup>
SNR 100% modulation index	81 dB with THD = -40 dB
PSRR at 60 Hz	-50 dB
PSRR at 120 Hz	-40 dB

implemented in a standard 0.35  $\mu\text{m}$  CMOS process and implements an envelope detector with a  $\pm 1.5$  V output swing on a 15 pF load. It dissipates 15 mW out of a  $\pm 2.5$  V voltage supply, and presents SNR = 81 dB measured at a THD = -40 dB for an input signal having 100% modulation index. The circuit was tested under extreme operation conditions, and has proved an effective solution for the proposed AM demodulation scheme.

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**Pietro Maris Ferreira** (SIE-EE'03) was born in Rio de Janeiro, Brazil, in 31 January 1984. He received the B.Sc. *cum lauda* in Electronic Engineer from the Federal University of Rio de Janeiro (UFRJ), Brazil, in 2006; and the M.Sc. in Electrical Engineer from the UFRJ in 2008. He is volunteer in UFRJ IEEE Student Branch since 2003, and was the UFRJ IEEE Student Branch Chairman in 2005. He organized many UFRJ and IEEE Student Meet-

ings, and earned the Technology Center Honor Mention paper award *XXVII Jornada Giulio Massarani de Iniciação Científica, Artística e Cultural da UFRJ*, in 2005; and the Technology Center Best paper award in *XXVI Jornada Giulio Massarani de Iniciação Científica, Artística e Cultural da UFRJ*, in 2004.



**Fernando A. P. Barúqui** received the B.Sc., M.Sc. and D.Sc. degrees in 1987, 1990 and 1999, respectively, all in Electrical Engineering from the Universidade Federal do Rio de Janeiro, Rio de Janeiro, Brazil. Since 1990 he has been an Associated Professor at the Department of Electronic Engineering of the Universidade Federal do Rio de Janeiro. His research interests are signal processing and integrated circuit

design for mixed signal applications.



**Antonio Petraglia** (S'89-M'91-SM'99) received the Engineer and M.Sc. degrees from the Federal University of Rio de Janeiro (UFRJ), Brazil, in 1977 and 1982, respectively, and the Ph.D. degree from the University of California, Santa Barbara (UCSB), in 1991, all in Electrical Engineering. In 1979, he joined the Faculty of UFRJ as an Associate Professor of Electrical Engineering, where he served as a Co-Chair in the Department of Electronic Engi-

neering from 1982 to 1984. During the second semester of 1991, he was a post-Doctoral researcher with the Department of Electrical and Computer Engineering at UCSB. Since 1992 he has been on the