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A synthesis methodology for AMS/RF circuit reliability: Application to a DCO design

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1. Introduction

Microelectronics development demands new technologies for new applications, which are driven by many circuit constraints. Circuit ageing degradation is increasing in advanced technologies, while application fields like military, medical and energy demand more reliability. Thus, reliability is one of the most important challenges of the semiconductor industry [1]. Reliability is defined as the ability of a circuit to work in accordance with its specifications over a given period of time and under specified conditions [2].

Circuit performance constraints are usually in terms of area, frequency, bandwidth, power consumption, noise performance, linearity and gain. The ageing stress conditions include temperature, signal swing and bias. Design for reliability means describing the circuit performance by its stress conditions, and finding how to increase the performance and decrease the stress.

The reliability concept is more and more used in digital circuit design [3], but has not been systematically used in AMS or RF circuits [4–6]. In order to design a reliable circuit, we need knowledge of the physical degradation and models to analyze the reliability degradation in earlier stages. Also, it needs to be simple enough to be used in the redesign, pointing out the sensitive components. In this work, we propose and validate a method of AMS and RF circuit design for reliability. For this goal, we have designed a realistic digital controlled oscillator (DCO) for 1 GHz RF applications with classical methodology and a reliable DCO applying our method.

We start our work reviewing the physical phenomena that degrade the circuit performance and how we can avoid them in Section 2. Next, we explain the physical phenomena models implemented by the simulator tool and characterized for the CMOS 65 nm process design kit (Section 3). In Section 4, we propose a synthesis methodology, detailing how we can increase circuit reliability. In Section 5, we explain how the reliability can be analyzed. In Section 6, we compare a realistic digital controlled oscillator (DCO) for 1 GHz RF applications with classical methodology and a reliable DCO applying our method. In Section 7, we check both circuit performance results, including process variability and reliability trends. Finally, we present our conclusions.

2. Physical phenomena

The physical phenomena mostly responsible for the ageing degradation in active devices are:

- *Hot Carrier Injection (HCI)* – the phenomenon that charges gain sufficient energy to overcome a potential barrier and then migrate to a different area of the device [7]. Such phenomenon occurs at the end of the drain junction of a transistor in saturation, creating many interface traps, which increase the substrate leakage current and cause drain current to decrease. The HCI takes effect when the V_{GD} is greater than or equal to zero and the V_{GS} is very high [2]. Therefore, this phenomenon could be avoided if we reduce the time in which the transistors are in strong inversion, by controlling V_{GD} and V_{GS} .
- *Negative Bias Temperature Instability (NBTI)* – the phenomenon that generates positive charges and interface traps. The NBTI is typically seen as a threshold voltage shift after stress [8].

The threshold voltage degradation can be recovered if the stress is stopped. It means that we can avoid the degradation phenomenon if we increase the ratio between the recovery time and stress time, and control the stress conditions (temperature and gate bias) as well.

- **Time Dependent Dielectric Breakdown (TDDB)** – the phenomenon of sudden loss of the layer's insulating properties, where the soft breakdown is more likely causing the circuit to lower its performance [9]. The control of the leakage current leads to a better way of reducing the TDDB probability. The TDDB can be avoided at low enough voltage and small enough gate area. In these cases, the device will show no breakdown before 10 years of lifetime [10].

Passive devices have ageing degradation caused by:

- **Electromigration (EM)** – the phenomenon of transport of mass in metals [11]. EM can be avoided by reducing the length of connections and increasing their width. Also, design with no-passive components (e.g. inductor-less radios) is more robust.

3. Simulation tools

The physical phenomena HCI and NBTI were chosen to be the focuses of the proposed methodology. The reason we chose such focuses is because they cannot be minimized enough to be neglected. However, EM is often treated as post-layout problem. EM can be avoided with inductor-less schematics and careful layout design. Also, the TDDB probability can be reduced by leakage control and careful layout design. Moreover, post-TDDB event behavioral models are being researched and they have not yet been established for commercial tools or characterized for commercial process design kits.

In order to minimize the HCI and the NBTI degradations, the bias and the temperature should be controlled. However, it is not always feasible because it can cause a considerable loss of circuit performance. Therefore, the reliability analysis should take the HCI and the NBTI into account. Next, we shall describe the simulation model implemented by the commercial simulator tool and extracted for the CMOS 65 nm process design kit.

3.1. HCI simulation

The simulator estimates the NMOS or PMOS HCI ageing by the Age parameter defined as [3]:

- NMOS

$$Age = \int_0^T \frac{I_{DS}}{WH_n} \left(\frac{I_{sub}}{I_{DS}} \right)^{m_n} dt, \quad (1)$$

- PMOS

$$Age = \int_0^T \frac{1}{H_p} \left(\frac{I_g}{W} \right)^{m_p} dt, \quad (2)$$

where T is the period of time of stress, W is the device width; I_{sub} , I_{DS} and I_g are the substrate, the drain and the gate currents, respectively; H and m are technology dependent parameters. Afterwards, the amount of degradation suffered by the transistor is monitored in each model parameter (P) (for example the threshold voltage, the channel mobility, etc.) and the degradation dynamics can be written as

$$\Delta P(t) = K(Age \cdot t)^n [3]. \quad (3)$$

Then, it uses computationally simple and BSIM compatible reliability models to predict the degradation.

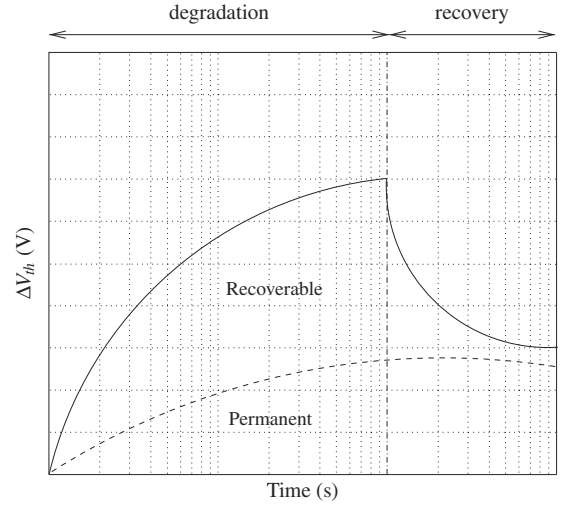


Fig. 1. Behavior monitor of the NBTI permanent and recoverable damage: illustration [3].

3.2. NBTI simulation

The behavior of the NBTI degradation is monitored by the threshold voltage shift (ΔV_{th}), represented in Fig. 1. The ΔV_{th} is induced by both permanent damage and recoverable degradation. As soon as the stress is stopped, the recoverable degradation decreases in time. This degradation is activated by temperature (T) and a high negative field and hence is dependent on the bias (V_{GS}). The permanent damage is modeled using the equation

$$\Delta V_{thp} = A_p \exp(\gamma_p V_{GS}) \exp\left(-\frac{E_{ap}}{kT}\right) t_{stress}^n. \quad (4)$$

The recoverable degradation is modeled by

$$\Delta V_{thr} = A_r \exp(\gamma_r V_{GS}) \exp\left(-\frac{E_{ar}}{kT}\right) \ln\left(1 + \frac{t_{stress}^n}{\tau_r}\right). \quad (5)$$

The recovered degradation is modeled by

$$\Delta V_{thrr} = A_{rr} \exp(\gamma_{rr} V_{GSrecovery}) \times \exp\left(-\frac{E_{arr}}{kT}\right) \ln\left(1 + \frac{t_{recovery}/t_{stress}}{\tau_{rr}}\right) \Delta V_{thr}. \quad (6)$$

In all ΔV_{th} Eqs. (4)–(6) [3], A is the technology dependent pre-factor, γ is the voltage accelerator factor, E_a is the activation energy in each case, τ is the physical time constant, k is Boltzmann's constant and T is temperature. The total threshold voltage shift is monitored by the equation

$$\Delta V_{th} = \Delta V_{thp} + \Delta V_{thr} - \Delta V_{thrr}. \quad (7)$$

This model is simple and BSIM compatible, but, to avoid any ΔV_{th} underestimation, it is important to use the on-the-fly stress and measurement technique [3] to fit the NBTI degradation model.

4. Synthesis methodology

The synthesis of a reliable circuit begins with the study of the transistor degradation. This knowledge show us the phenomena that can be minimized enough to be neglected and which ones should be taken into account. We choose HCI and NBTI to be the focuses of the proposed methodology.

The HCI degradation can be reduced if the drain current is decreased. However, this is not always feasible, since noise and output charge represent a more important constraint in most

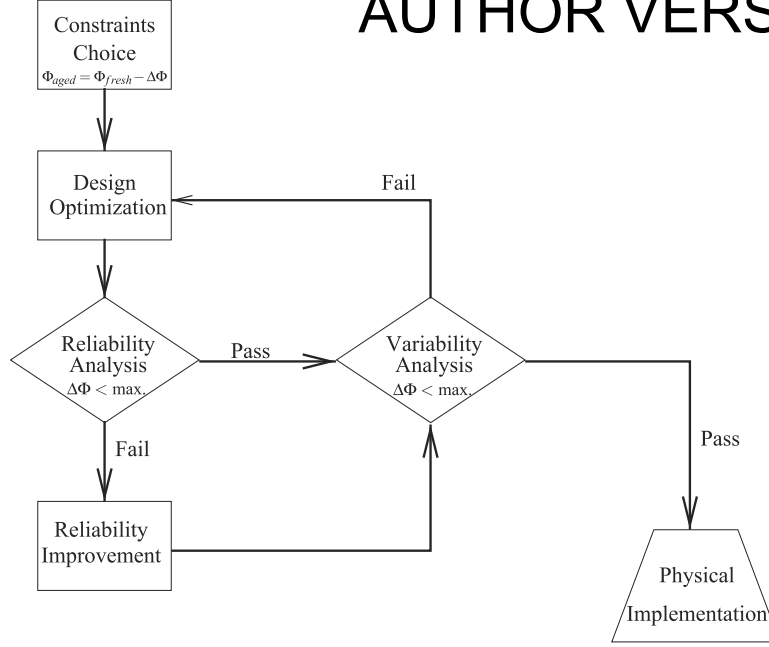


Fig. 2. Design for reliability methodology: diagram.

design cases. Regarding the NBTI, a good way to reduce its degradation is to increase the ratio between the recovery time and stress. However, it is not always the case. In our DCO example, the time constraints are imposed by the speed needs. In order to be reliable, the circuit must follow its performance needs during the whole lifetime despite HCI and NBTI degradations.

Thus, we propose the synthesis methodology shown in Fig. 2. The first step of the design for a reliability method is to choose the important constraints to be considered. Next, we should describe the circuit performance as a function of the behavior of the devices in the hierarchical level below. Then, the chosen performance Φ should be separated as

$$\Phi_{aged} = \Phi_{fresh} - \Delta\Phi, \quad (8)$$

where $\Delta\Phi$ represents the amount of degradation, evaluated between the fresh circuit simulation and the aged circuit simulation.

After that, the circuit would normally be optimized with a classical design method. However, the reliable synthesis imposes the maximum $\Delta\Phi$ in order to fix the minimum circuit lifetime. Then, the reliability analysis (detailed in the next section) could point out the sensitive devices in order to improve the circuit lifetime. Iterating the reliability analysis, we can obtain the optimized and the reliable circuit at same time. Thus, the methodology considers performance and lifetime needs as criteria that can be adjusted, allowing the designer to indicate which one is more important for each circuit application.

Subsequently, the circuit performance is analyzed focusing on the variability of the integration process technology. Using Monte Carlo simulation or circuit performance corner extraction, we can evaluate the variability degradation of Φ and thus redesign the circuit if need be to increase the yield.

Thus, the proposed method can fit quite well the process variability issues. If we consider process variability and reliability, there are basically two different ways to degrade the performance. Both ways can be described as functions of the device parameters. Monte Carlo simulation predicts the impact of variability issues on the performance, and in the proposed analysis, the impact of reliability issues. With both performance deviations, the designer may find how robust the circuit is and how it can be improved.

5. Analysis methodology

We believe that in the near future, reliability analysis tools will be part of the design process in the same way that the variability tools already are. For a reliable design, the reliability analysis must be placed in early stages and must be connected with the design methodology.

Applying the reliability analysis at the transistor level, the device behavior chosen to model the HCI and the NBTI degradations in this method is the transistor drain current. Thus, the Eq. (8) becomes

$$I_{DSaged} = (1 - \alpha)I_{DSfresh}, \quad (9)$$

where $\Delta I_{DS} = \alpha I_{DSfresh}$ and α is the percentage of I_{DS} degradation. α is evaluated between the fresh circuit simulation and the aged circuit simulation as [12]

$$\alpha = \frac{I_{DSaged} - I_{DSfresh}}{I_{DSfresh}}. \quad (10)$$

[13,8] have shown similar models. In order to evaluate the circuit reliability, ΔI_{DS} will feed the model shown in Fig. 3. This transistor model will replace its corresponding transistor and indicate the sensitivity of the devices [12].

The most important step consists in describing the typical environment conditions, such as temperature, signal swing and circuit frequency. In order to obtain a consistent model, the circuit test

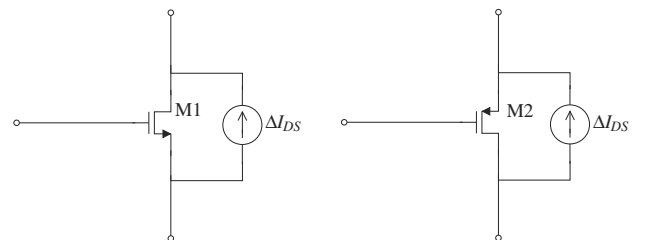


Fig. 3. NMOS and PMOS transistors reliability model for analysis purposes ($\Delta I_{DS} = \alpha I_{DSfresh}$).

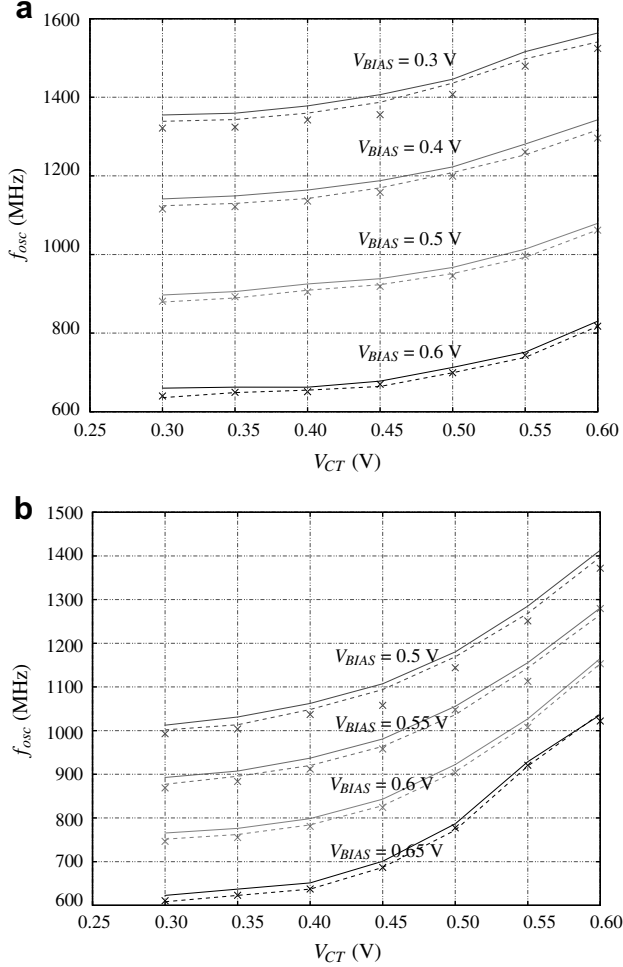


Fig. 4. The DCO oscillation frequency (f_{osc}) simulated at 27 °C during 30 years of degradation for (a) the classical and (b) reliable designed circuit. The result before the stress is represented by the solid line, after the stress by a dashed line and the aged model marked by x.

bench should represent these stress conditions. Thus, the circuit degradation is measured by the chosen behavior of the transistor (I_{DS}) under HCI and NBTI degradations.

The earlier the designer can simulate the cell performance, the better it is to evaluate ΔI_{DS} degradation. Moreover, such degradation represents the behavior variation that the circuit should be robust to. Thus, the design methodology could predict how robust the circuit is and if a possible redesign can increase its reliability. In order to achieve better results, the analysis should be iterated with the design, and this is the core of the design for reliability method.

5.1. Application of the analysis model

In order to demonstrate the reliability analysis method, we show the analysis of a DCO designed with the classical methodology and a reliable DCO (design presented in Section 6). Fig. 4a and b show both DCOs stressed for 30 years of ageing at 27 °C for all digital control words, converted into analog voltages. Actually, the full validation of the analysis model was presented in [6].

6. DCO design example

In order to illustrate the reliability design method, we chose to design a realistic DCO for RF applications near 1 GHz. The 5–3 NOR

interpolative DCO [14] was chosen because it has a large signal at the transistor gates, resulting in HCI degradation. And also, we cannot control the PMOS transistor NBTI stress time, as this time is correlated with the oscillation frequency. The DCO, designed in CMOS 65 nm, has to generate a frequency clock between 600 MHz and 1.2 GHz. The Fig. 5 shows the circuit schematic, where V_{CT} and V_{BIAS} are the control words converted into bias voltages for NMOS and PMOS respectively.

First of all, we do not consider the variability of the integration process technology, and, thus, only the reliability degradation could decrease the circuit performance. In this circuit, the minimum number of stages is 3 and the maximum (N_{max}) is 5, so we have four effective stages (N_{eff}) in the feedback loop. The oscillation frequency is

$$f_{osc} = \frac{1}{2N_{eff}t_d} \quad (11)$$

where t_d is the NOR cell delay. We found $80 \text{ ps} < t_d < 200 \text{ ps}$ to be the cell delay, which can be described as

$$t_d = \frac{C_L}{gm}. \quad (12)$$

We assume that the delay is the same for all cells for both rise and fall transitions of the signal. Approximately

$$gm = \frac{2I_{DS}}{V_{ov}}, \quad (13)$$

where V_{ov} is the overdrive voltage and I_{DS} is the drain to source current. Therefore, f_{osc} is a function of I_{DS} , as

$$f_{osc} = \frac{I_{DS}}{N_{eff}C_LV_{ov}}, \quad (14)$$

and the current degradation will represent a loss in the oscillation frequency. The oscillation frequency degradation can be obtained by deriving Eq. (14). As presented in

$$\Delta f_{osc} = \frac{\Delta I_{DS}}{N_{eff}C_LV_{ov}}, \quad (15)$$

Δf_{osc} has a linear dependence with ΔI_{DS} transistor behavior chosen in the reliability analysis. As the frequency, the maximum power consumption (P_{max}) is a function of the maximum current at the load. Thus, P_{max} , evaluated as

$$P_{max} = N_{max}V_{DD}I_{DS}, \quad (16)$$

is only limited by I_{DS} (assuming constant V_{DD}). Consequently, the maximum power consumption degradation is

$$\Delta P_{max} = N_{max}V_{DD}\Delta I_{DS}. \quad (17)$$

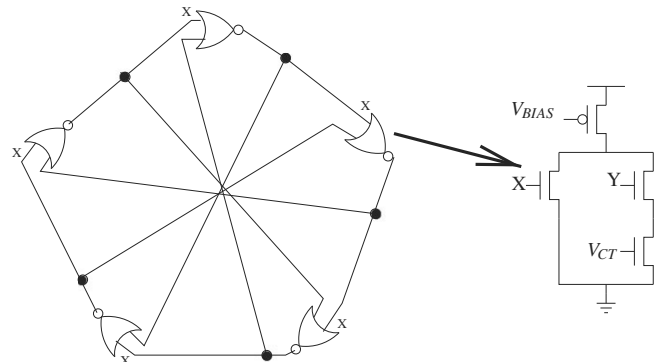


Fig. 5. The 5–3 NOR interpolative DCO schematic [14].

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Another important performance parameter to be evaluated in oscillators is the phase noise ($L(f)$). The f is the frequency distance between the carrier frequency and the noise frequency. According to [15], the $L(f)$ is a function of the transistor bias current (I_{DS} in our design) and a constant γ_n which represents the transistor noise model, as

$$L(f) = 10 \log \frac{\gamma_n}{I_{DS}}. \quad (18)$$

Hence, the phase noise ageing degradation is

$$\Delta L(f) = 10 \log(1 - \alpha), \quad (19)$$

where α was defined in Eq. (10).

During the design optimization, we naturally found that the power consumption is reduced, if the designer choose $V_{DD} - V_{BIAS}$ as low as possible. In this bias condition, the reliability analysis shows lower NBTI degradation. Fig. 6 illustrates the amount of NBTI degradation over years of degradation for each V_{BIAS} at 150 °C of temperature stress. Clearly, the circuit will present lower NBTI degradation for $V_{BIAS} > 0.5$ V and will consume less power. Aiming to cover the oscillation frequency span, the designer has to choose between accepting the degradation presented in Fig. 6 or redesigning the DCO to be reliable. If the reliability and the power consumption constraints are chosen to be optimized, the designer will need an oversized DCO to cover from 600 MHz to 1.2 GHz for $V_{BIAS} > 0.5$ V. Such optimization will be the design for reliability choice. In the other hand, the classical design methodology will choose not to overdesign the DCO, and hence the DCO will be exploited for $0.3 \text{ V} < V_{BIAS} < 0.6$ V.

The classical design indicates that the PMOS width should be three times bigger than the NMOS width (W) for the DCO clock with an equal duty cycle. Increasing the reliability, we propose to use $V_{BIAS} > 0.5$ V and to design the width as to $W/2$ for both NMOS

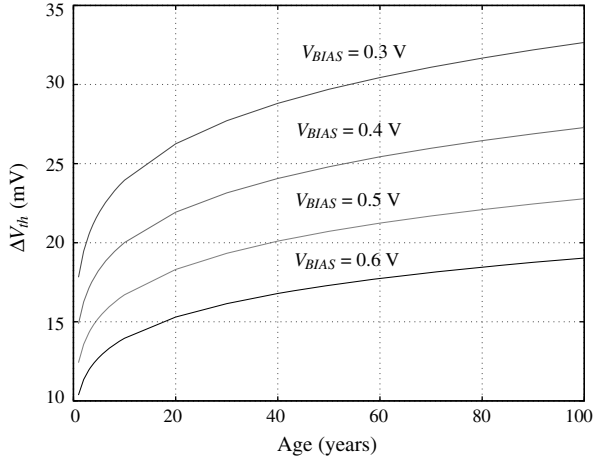


Fig. 6. ΔV_{th} degradation for the PMOS DCO transistors stressed by NBTI at 150 °C.

Table 1
The dimensions of the designed DCO ($L = 0.5 \mu\text{m}$).

	W_X (μm)	W_Y and W_{CT} (μm)	W_{PMOS} (μm)
DCO	5	5	15.0
	4	4	12.0
	3	3	9.0
Reliable DCO	5	2.5	15.0
	4	2.0	12.0
	3	1.5	9.0

Table 2

Phase noise ($f_{osc} = 1$ GHz at 1 MHz off-set) versus the f_{osc} and P ageing degradations at 10 years lifetime for each design and sizing.

	W_X (μm)	$\Delta f_{osc}/f_{osc}$ @ 1 GHz and 10 years (%)	$\Delta P/P$ @ 1 GHz and 10 years (%)	$L(1.0 \text{ MHz})$ @ 1 GHz (dBc/Hz)
DCO	5	1.90	2.2	-94.3
	4	1.86	2.2	-93.4
	3	1.90	2.2	-92.2
Reliable DCO	5	1.6	0.4	-92.7
	4	1.7	0.4	-91.7
	3	1.3	2.1	-90.5

in the Y path (marked with Y and V_{CT} in the transistor gate in Fig. 5). Comparing the classical design and the reliable design options, the dimensions of the DCO are present in Table 1.

In order to reduce the phase noise, the sizes should be increased. Table 2 confirms the phase noise reduction as the NMOS width increases, but it also indicates the increase of the oscillation frequency degradation for $f_{osc} = 1$ GHz and 10 years of ageing. The reliable DCO has the oscillation frequency degradation reduced by a value between 15% and 30%. As a trade-off, the phase noise presented an average increase of 2.0 dBc/Hz. If such phase noise is reasonable for a target RF standard, the reliable DCO will be

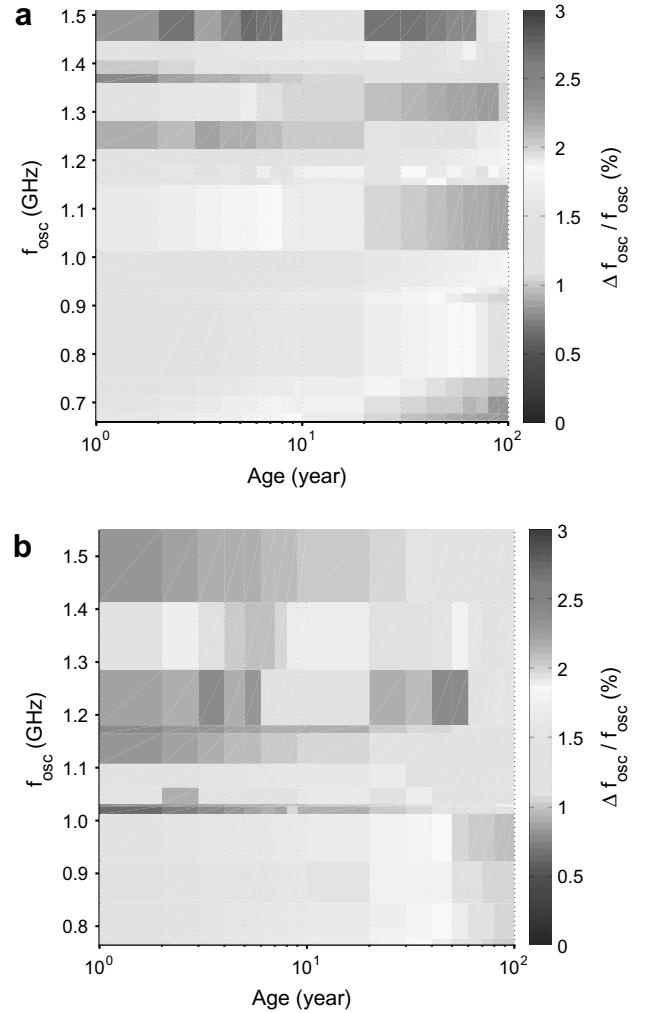


Fig. 7. The $\Delta f_{osc}/f_{osc}$ degradation at 27 °C for (a) the classical and (b) the reliable designed DCO.

the better option. Both DCOs will be designed with $W_X = 5 \mu\text{m}$, aiming at phase noise reduction.

7. Simulation results

Combining the trends indicated by the reliability analysis, both DCO circuits were sized ($L = 0.5 \mu\text{m}$ and the widths are presented in the line of $W_X = 5 \mu\text{m}$ of Table 1) to cover from 600 MHz to 1.2 GHz. The DCO (at 1 GHz) consumed 1.40 mW of power without stress and 1.37 mW after 10 years of stress degradation. The reliable DCO (at 1 GHz) consumed 1.06 mW of power without stress and the same power after 10 years of stress degradation (negligible ageing).

The reliability simulation reveals in Fig. 7a and b the normalized f_{osc} degradation obtained from both DCOs stressed at 27°C for different ageing times. The classical designed DCO presented a bigger frequency range and bigger ageing degradation up to 2.8%. Moreover, the classical designed DCO at 1 GHz results in 2.0% of degradation limiting its lifetime at 10 years. The reliable DCO presented a lower frequency range but achieves a smaller degradation in most cases and 2.5% at worst. Therefore, the reliable DCO can be exploited more than 50 years of lifetime in most part of the frequency range. Its lifetime is 50 years at 1 GHz for 2.0% of degradation.

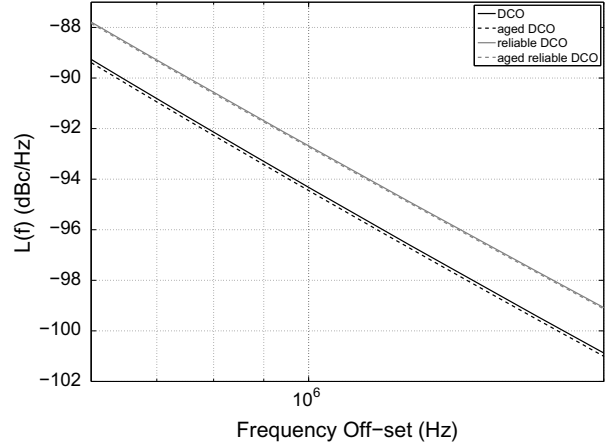


Fig. 9. The phase noise performance of the DCO and the reliable DCO, simulated for $f_{osc} = 1 \text{ GHz}$.

In order to present the strengths of the reliable DCO, we choose to present the reliability simulation in an accelerate environment at 150°C . Fig. 8a and b reveals a bigger NBTI stress. The normalized f_{osc} degradation obtained for the classical designed DCO is more

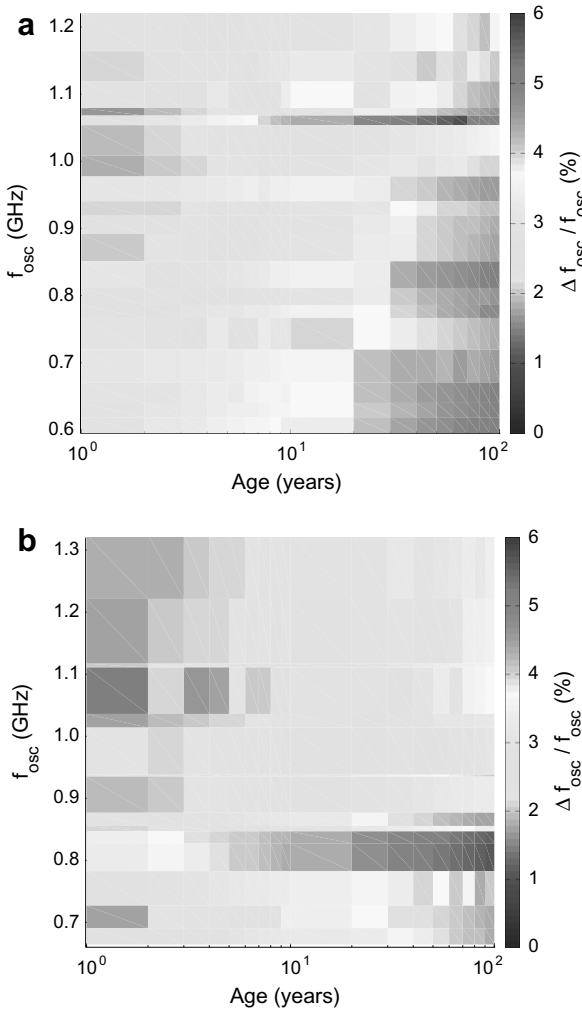


Fig. 8. The $\Delta f_{osc}/f_{osc}$ degradation at 150°C for (a) the classical and (b) the reliable designed DCO.

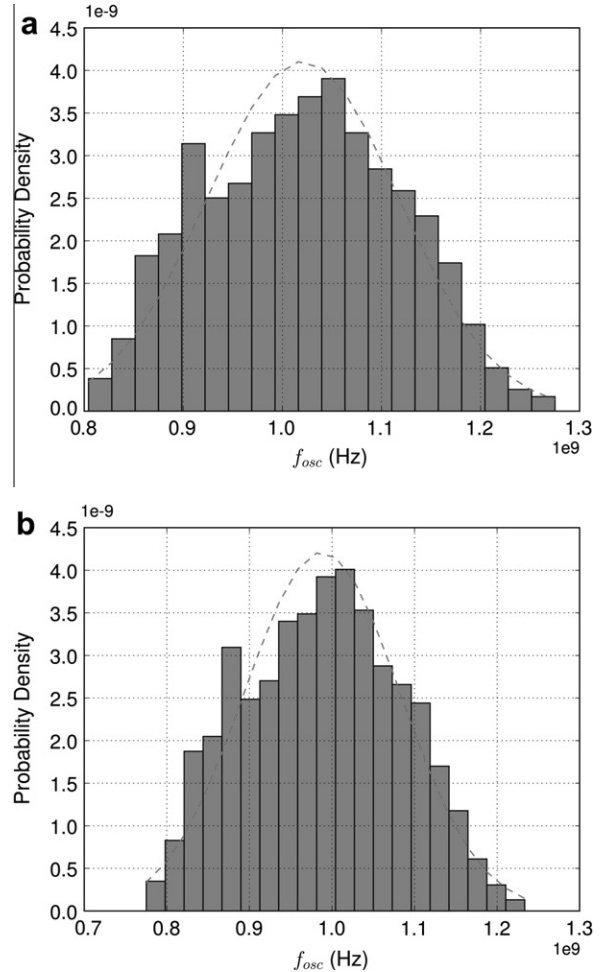


Fig. 10. The DCO f_{osc} variability, simulated at $f_{osc} = 1 \text{ GHz}$ by 1000 Monte Carlo runs. (a) The classical designed circuit presented $\mu = 1.020 \text{ GHz}$ and $\sigma = 97.1 \text{ MHz}$, and (b) the reliable designed presented $\mu = 0.988 \text{ GHz}$ and $\sigma = 94.7 \text{ MHz}$.

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than 3% in mostly cases. In the other hand, the reliable DCO has presented a f_{osc} degradation between 2% and 3% which represents a reduction of 30% of the f_{osc} degradation in mostly cases.

The DCO and the reliable DCO phase noise simulations, presented in the Fig. 9, are very close and only a RF standard choice can limit the phase noise constraint. The ageing simulations performed at each circuit lifetime (also presented in Fig. 9) did not present noise performance degradation big enough.

The variability simulation was performed by 1000 points of Monte Carlo simulation for both DCO programmed at $f_{osc} = 1$ GHz and stressed at 27 °C. First, they are simulated against variability and the results are presented in Fig. 10a and b. After that, they are simulated with the ageing model (presented in Fig. 3) extracted from the nominal run for 10 years of stress (presented in Fig. 11a and b). All results demonstrate that the reliability has no significant impact compared to the variability, and therefore it could be neglected in our example.

Finally, both DCOs can be characterized by the figure of merit for RF oscillators, defined as

$$\text{FoM} = L(\Delta f) - 20 \log \frac{f_{osc}}{\Delta f} + 10 \log P/1\text{mW}[1]. \quad (20)$$

The FoM of the fresh circuits was evaluated as -152.8 dB for the classical designed DCO and -152.4 dB for the reliable DCO. If we

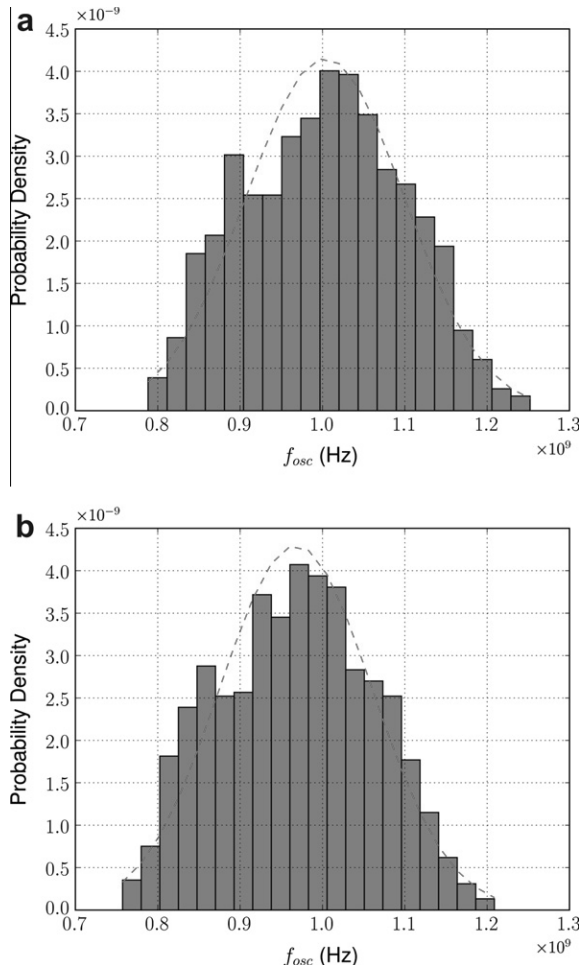


Fig. 11. The DCO f_{osc} variability, simulated with the ageing model for 10 years of stress at $f_{osc} = 1$ GHz by 1000 Monte Carlo runs. (a) The classical designed circuit presented $\mu = 1.003$ GHz and $\sigma = 95.9$ MHz, and (b) the reliable designed presented $\mu = 0.967$ GHz and $\sigma = 92.7$ MHz.

take into account the power consumption (Eq. (17)) and the phase noise (Eq. (19)) degradation, the FoM for RF oscillators does not take the reliability degradation into account. Both degradations compensate each other in Eq. (20), and therefore there is no need to present the FoM for the aged circuits.

8. Conclusions

In this work, we proposed new circuit synthesis method developed for AMS/RF circuits. This method considers the reliability degradation caused by circuit ageing as a design criterion, as important as the classical constraints (noise, signal range, power and die area consumption). For this purpose, we introduced the physical phenomena context and how they could be avoided. Then, we presented the design for reliability method and validated its reliability analysis model.

We checked that the reliability analysis gives us information to improve the method optimization, designing a more reliable circuit. Designing a classical and a reliable DCO, we achieve a frequency degradation reduction by a value between 15% and 30%. And also, the reliable DCO has a circuit lifetime five times longer than the classical DCO, if we fix the maximum frequency range degradation at 2.0%. Disadvantages of the method are the increase in the phase noise and the reduction of the frequency range that could be neglected for a target RF standard.

In this context, the presented methodology put in evidence the reliability as a criterion in the design. Our experiments with the reliability show how to optimize this criterion and reveal their advantages and disadvantages. What's more, we can exploit the design for reliability methodology for any circuit abstraction level. As a result, the device performance in a higher abstraction level can be described by individual circuit behavior in a lower abstraction level. With similar equations to those presented in this work, the behavioral variation can be propagated from the lower to the higher abstraction level. Therefore, the performance variation caused by reliability or by variability issues can be analyzed and improvements may be found.

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