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Synthesized High-Frequency Thyristor for Dielectric Barrier Discharge Excimer Lamps

Marc Cousineau, *Member, IEEE*, Rafael Díez, *Member, IEEE*, Hubert Piquet, and Olivier Durrieu

Abstract—Dielectric barrier discharge (DBD) lamps, being capacitive loads, must be associated with bidirectional current sources for an appropriate control of the transferred power. Pulsed current source supplies, which are known to offer very interesting performances, require specific power switches that are able to manage bidirectional voltage and unidirectional current at much higher frequencies (several hundreds of kilohertz) than commercial thyristors. This paper proposes the detailed design of such a high-speed synthesized thyristor, using discrete components: a MOSFET in series with a high-voltage (HV) diode and a logic circuit that controls its gate. This switch is associated with an optimized self-powered driver, which is a very efficient solution to handle the perturbations associated with the HV and high-frequency operation. Experimental application of this device for DBD excimer lamp supply is proposed.

Index Terms—Charge transfer, dielectric barrier discharge (DBD), excimer UV lamps, semiconductor switches, switched mode power supplies.

I. INTRODUCTION

DIELECTRIC BARRIER DISCHARGES (DBDs) are extensively used nowadays for the generation of cold plasma in gas mixtures [1], [2]. The introduction of dielectric barriers between the electrodes of an ac discharge incorporates two main advantages: It maintains the plasma in the nonequilibrium regime and helps produce homogeneous electrical discharges at relatively high pressures. These attributes are highly demanded in surface treatment processes in order to work at relatively low temperatures and to reduce the production costs [3], [4]; they are also very interesting for ozone generation applications [5], [6], as well as for DBD excimer lamps dedicated to UV generation [7]–[10]: These lamps are electrodischarge sources of

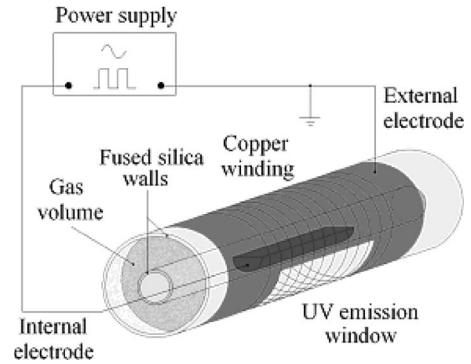


Fig. 1. Geometry of a DBD lamp with coaxial configuration.

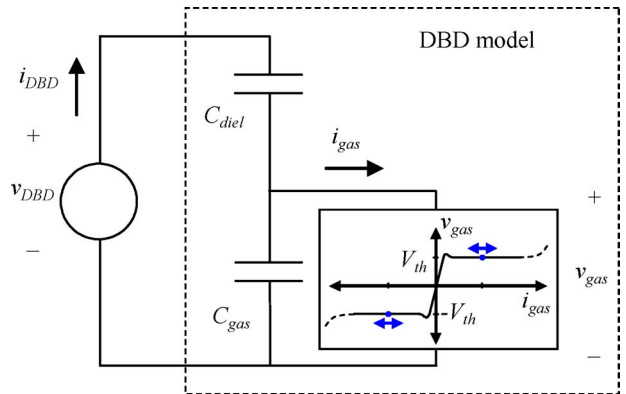


Fig. 2. Electrical model of a DBD: C_{diel} symbolizes the dielectric barriers, C_{gas} corresponds to the isolating nature of the gas before breakdown, and the voltage–current characteristic of the gas introduces the conduction current.

incoherent spontaneous UV and vacuum UV radiation, emitted due to the decay of excimer and exciplex molecules, obtained by means of electrical discharges developed in gas mixtures (typically Xe–Cl and Kr–Br). The gases are maintained in sealed bulbs, and metallic electrodes are wrapped around the bulb, obtaining a DBD structure (see Fig. 1). This paper focuses on this application; however, the proposed approach is applicable for any DBD system.

In contrast with the benefits mentioned in the previous paragraph, DBDs bring out a challenge in the construction of their power supplies. Since DBDs are of a capacitive nature, as shown in the equivalent circuit in Fig. 2, dc voltage or current sources cannot supply this kind of load (with a dc voltage source, the dielectric barriers would charge to the imposed voltage, and hence, the steady-state current would be zero and also the power; for current sources with a dc offset, the dielectrics would accumulate electric charges, and the voltages

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would increase indefinitely to the point of damaging some components of the system).

Previous works [11]–[14] demonstrate that a bidirectional pulsed current-mode source is appropriate to control the power delivered to a DBD; this solution is in good agreement with causality criteria and enables the predictability of all the variables in the converter during the design stage [15], thus improving the dimensioning of the entire power supply. It has also been shown that the control of the current injected into excimer lamps enables the control of the UV emission [16].

As will be explained, the implementation of candidate converter topologies has a primordial need: a thyristorlike component, which is capable of switching at hundreds of kilohertz. Considering that commercial thyristors are rated to operate at high currents and low frequencies (less than 1 kHz) [17], the development of a synthesis device [18] is presented in this paper.

First, in Section II, the current-mode converter is presented, establishing the high-frequency thyristor as the right switch to be used. Then, Sections III and IV are dedicated to the definition of the specifications and to the detailed discussion of the principles and implementation of this synthesized switch; special attention is paid to the development of an optimized self-powered driver (Section IV-D). Finally, experimental validation based on a specific pulsed current source converter for the supply of an excimer lamp is proposed in Section V.

II. POWER SUPPLY DEFINITION

A. Current-Mode Approach for Supplying a DBD

Almost all of the DBDs can be represented using the model in Fig. 2 [23]–[26]. Because of its capacitive nature, to satisfy the causality criteria, this load must be supplied with a current-mode converter. This current must have a zero mean value; otherwise, the voltage across the dielectric barriers will reach uncontrolled values.

Another reason to supply the DBD with a current-mode converter, instead of a voltage-mode converter, remains in the desired “normal glow regime” of the gas obtainable with DBDs: the absolute value of the gas voltage v_{gas} is almost constant (V_{th} voltage). When this gas state is reached, as in [27], the only way to control and vary the power is by changing the current set point (as suggested by the arrows in the v_{gas} versus i_{gas} characteristic in Fig. 2).

B. Pulsed Current-Mode Converter

The current-mode approach has been developed and demonstrated with two different structures for an excimer lamp in [28]. Fig. 3 shows one of these topologies working in a discontinuous conduction current mode. In the top figure, the original concept is shown, where a unidirectional pulsed current source J , based on the buck–boost converter working in discontinuous current mode, supplies the lamp via a full bridge. This bridge inverts every half cycle the direction of the pulsed current source.

In the bottom figure, the final implementation is shown. The step-up transformer is used to reduce the lamp voltage (typ-

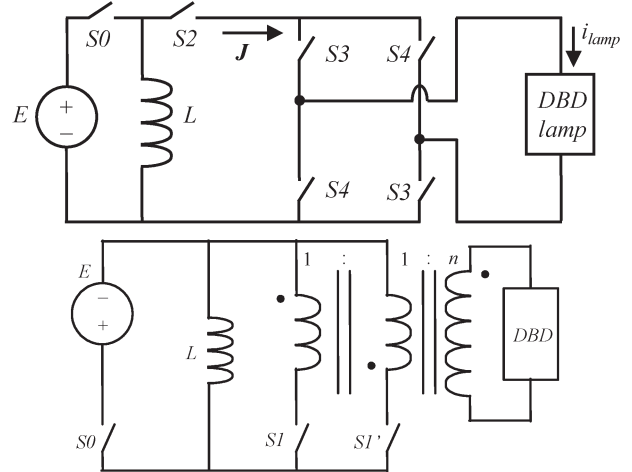


Fig. 3. Pulsed current-mode converter topology. (Top) Original concept and (bottom) implemented structure.

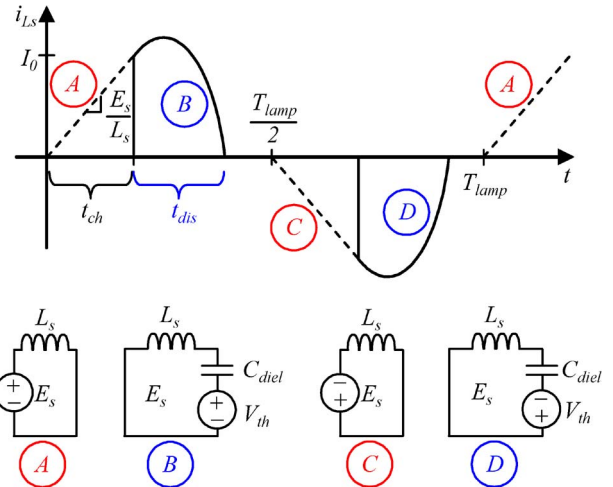


Fig. 4. Operating sequences of the pulsed current mode.

ically 7 kV) to values compatible with commercial semiconductors (switches S_0 , S_2 , S_3 , and S_4). Taking advantage of the transformer need, a two-primary-winding configuration is used in order to merge the full bridge to a two-switch and common-cathode structure, facilitating the gate driver construction. In the same manner, S_2 is combined during the half cycle with S_3 to produce S_1 and during the other half cycle with S_4 to produce S_1' . S_0 is relocated to obtain the final topology, which presents only three common-cathode switches.

The operating principle of this converter is shown in Fig. 4 (all elements are seen from the secondary of the transformer). During t_{ch} , while S_0 is on, the current in the inductance (L) linearly increases in the so-called charge phase A.

Then, S_1 is turned on, and S_0 is turned off. The energy previously stored in the inductance is now sent to the DBD, this last being represented by the dielectric capacitance C_{diel} and the constant voltage across the gas V_{th} . This time interval called discharge sequence B has a resonant behavior, associating the dielectric capacitance of the load and the inductance of the converter. Note that the magnetizing inductance of the transformer must be much higher than the L inductance in order to obtain the series resonant tank shown in Fig. 4 and

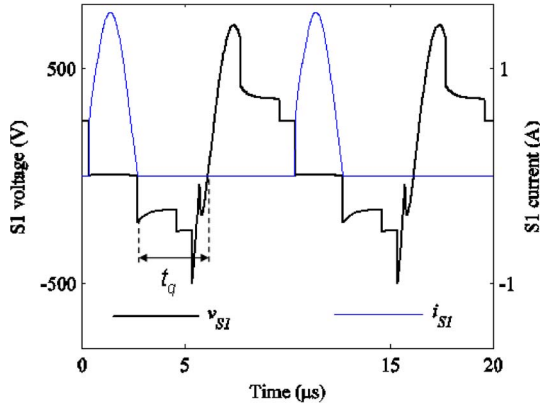


Fig. 5. Simulated waveforms for S1.

also the current source mode desired. When the decreasing current crosses the zero value, S1 turns off, indicating the end of the discharge sequence with a duration t_{dis} . This phase is followed by a zero-current sequence, which defines the half of the operating period. This blanking time provides one degree of freedom to adjust the DBD power, varying the operating frequency.

The second half of the period has a development similar to the first one; S1' is used instead of S1. Therefore, the current in the secondary will flow in the opposite direction. In order to invert the lamp current, a full-bridge topology (instead of a two-primary-winding transformer) can also be used.

Another method to adjust and control the DBD power, aside from the frequency change, is the variation of the energy stored in the inductance at the end of the charge sequence—see (1)—by means of the charge time t_{ch} or by adjustment of the magnitude of the E source

$$Energy\ at\ t_{ch} = \frac{1}{2} \cdot L \cdot \left(t_{ch} \cdot \frac{E}{L} \right)^2. \quad (1)$$

III. SPECIFICATIONS OF THE POWER SUPPLY SWITCHES

A. Nature of the Switches

The current-mode converter presented in the last section requires specific types of switches to work correctly. This can be stated with the simulation of the whole circuit in Fig. 3, using, in the first step, ideal switches managed according to the desired sequences in Fig. 4. For the case of the DBD lamp supply treated in this paper, as shown in Fig. 5, the waveforms for S1 have unidirectional current and bidirectional voltage. S1' and S0 have the same characteristics.

Concerning the commutations, the dynamic characteristic built from these waveforms and shown in Fig. 6 exhibits a controlled turn-on under positive voltage and spontaneous turnoff at null current: This is the behavior of a thyristor. Unidirectional voltage devices like insulated-gate bipolar transistors must be avoided because, immediately after turnoff, the switch voltage attains a highly negative value producing the destruction of such a device.

Nevertheless, commercial devices [17] are not suited for DBD lamp applications due to the required high-frequency

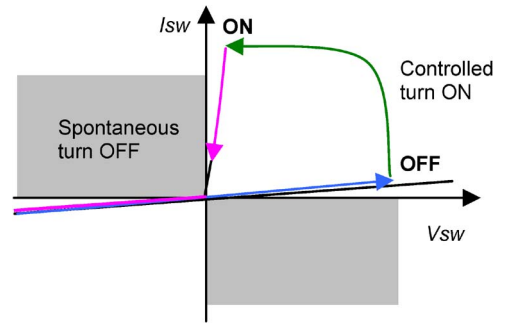


Fig. 6. I_{sw} versus V_{sw} static and dynamic characteristics.

TABLE I
CHARACTERISTICS OF THE HIGH-FREQUENCY SYNTHESIZED THYRISTOR

Symbol	Quantity	Desired values
V_{rmax}	max. reverse voltage	1000 V
V_{dmax}	max. direct voltage (off-state)	1000 V
I_{dmax}	max. on-state current	peak : 5 A
t_q	max. turn-off time	< 1 μ s
f_{max}	max. operating frequency	400 kHz
V_g	gating signal (turn-on)	TTL levels, isolated

range. The synthesis and implementation of high-speed thyristorlike devices are the main focus of this paper and are developed in the following parts. A similar synthesis approach to the one described in this paper has been already used for other switching functions [7], [8], [18].

B. Electrical Characteristic Definition

In this section, as well as for further experimental validations, the supply of a specific DBD excimer UV lamp (100 W) [7], [10], [28] is considered; a frequency range from 40 to 200 kHz is selected for UV emission control investigations. Concerning the switch specifications, the maximum values of voltage and current are selected during the design of the supply, using the degree of freedom brought by the choice of the step-up ratio of the transformer [29]. The chosen ratio enables the use of semiconductors in the range of 1000 V or less; using this ratio, numerical simulations or analytical analyses are carried out to define the expected characteristics of the high-speed synthesized thyristor (see Table I).

The management of the turnoff time (t_q) is very important since the voltage across the switch returns very quickly to positive values after the decreasing current crosses the zero value (see Fig. 5). If the switch has not been locked in the OFF state during this interval, it can produce undesired reconnection, losing the benefits of the zero-current-switching mode.

IV. SYNTHESIS OF THYRISTORLIKE SWITCHES

A. Principle

Fig. 7 shows the concept diagram of the proposed circuit to conform to the characteristics shown in Fig. 6.

A serial association of a diode with a transistor is used to obtain the desired static characteristic: It allows a controlled

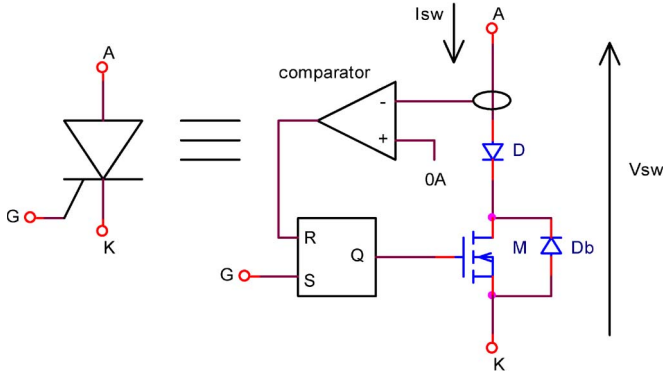


Fig. 7. Schematic overview of the synthesized thyristor.

turn-on and prohibits negative currents. A MOSFET is chosen because it provides capability to sustain high voltage (HV) in the OFF state, fast switching performance, and low on-resistance. When the decreasing current crosses the zero value and the diode naturally turns off, the transistor must also be turned off to maintain the entire switch locked in the OFF state in case the voltage returns to positive values.

The management of the switch state is a crucial issue to obtain the desired performances: The following sections are focused on the measurement and sign detection of I_{sw} current (Section IV-B), the management of the MOSFET gate (Section IV-C), and the self-powering stage (Section IV-D), a very useful feature for this device operating in a harsh environment.

B. Current-Sensing Methods and Sign Detection

At the circuit design step, the technique of sensing the I_{sw} current becomes the main concern [30]. When the application is running, the voltage V_{sw} reaches high positive and negative values, and very HV and current variations (dV_{sw}/dt and dI_{sw}/dt) are generated during switching. Fig. 8 shows an overview of the considered solutions which are compared, regarding these constraints.

Solution 1) Measurement of the voltage V_{ak} (sum of the voltages across M and D) provides information on the sign of the I_{sw} current. While this voltage exceeds a threshold voltage V_{th} (representing the sum of the voltages across M and D for a given positive current), the current I_{sw} is supposed to be positive. The main drawback of this approach is that, because of the large variation of the anode-to-cathode voltage, it is necessary to add a protection diode and an RC low-pass filter to send the signal to the comparator input. These additional components strongly limit the switching-frequency range.

Solution 2) This solution proposes the use of a senseFET associated with a sense resistor R_s in order to estimate the direction of the MOSFET drain current I_{sw} . Aside from the presence of reading errors when the sign of I_{sw} changes, it must be noticed that the choice of available manufac-

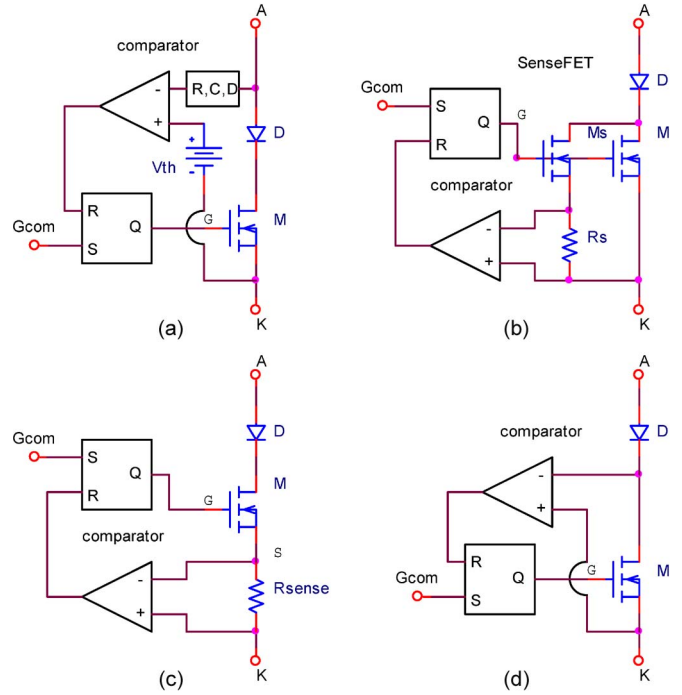


Fig. 8. Possible detection strategies. (a) Reading of V_{ak} . (b) Use of a senseFET. (c) Use of a sense resistance. (d) Reading of V_{ds} .

tured senseFETs is very limited. This approach can suit a very small number of applications with suitable specifications.

Solution 3) Introducing a low-value series sense resistor R_{sense} with the MOSFET provides a reliable reading of the I_{sw} current value after proper noise filtering. This resistor contributes to increasing the conduction losses of the switch. Moreover, unintended parasitics on the current I_{sw} lead to variations of the voltage V_{gs} and affect the control of the switch during the ON state.

Solution 4) This solution uses the fact that the MOSFET transistor M at the ON state can be considered as a low-value resistance with a quasi-constant value, as shown in the following:

$$V_{ds} = R_{dson} \cdot I_{sw}. \quad (2)$$

The reading of V_{ds} voltage is a direct image of the current value. The sign of this voltage directly indicates the direction of the I_{sw} current. This approach is similar to solution 3) without its drawbacks.

The design concept shown in Fig. 8(d) represents the architecture selected in our application for the current-sensing technique. The advantages of this architecture are summarized as follows.

- 1) The detection circuit does not alter the operation of the MOSFET M .
- 2) The reading of the I_{sw} current is achieved under a low-impedance condition.
- 3) A detection insensitive to the R_{dson} value is obtained because only the sign of the measurement is important.

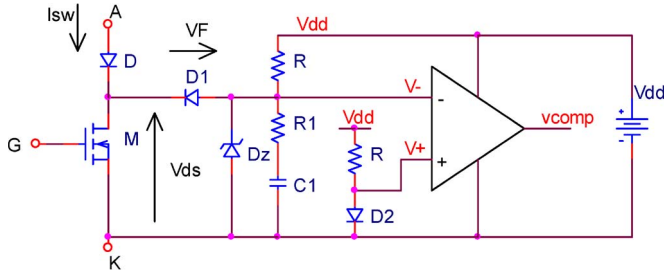


Fig. 9. Detection circuit for current I_{sw} zero crossing.

- 4) The input of the comparator is clamped to approximately -0.7 V for negative voltages owing to the presence of the power diode in association with the body diode of the MOSFET.

The implementation of the “comparator” function in Fig. 8(d) is now provided.

The V_{ds} voltage, which is proportional to the I_{sw} current [see (2)], is used for sensing this current, as long as M is in the ON state. This voltage has a low value and remains limited to a few volts. The zero-crossing detection for the current I_{sw} is achieved by means of the sign-detection circuit shown in Fig. 9. It compares the MOSFET voltage V_{ds} against the 0-V level.

When the transistor M is in the OFF state, the inverting input of the comparator must be protected. Consequently, the diode D_1 sustains, during this state, the voltage between the drain of M and the input of the comparator.

When the current I_{sw} reaches a zero value, V_{ds} is equal to zero, and the input voltage of the comparator is equal to V_F (the D_1 forward drop voltage). In order to correctly detect the transition to zero of the I_{sw} current, it is important to prepolarize the noninverting input of the comparator at the V_F voltage. For this reason, the diode D_2 is added and must match the D_1 diode. The R_1, C_1 branch evacuates the charges stored in D_1 during the off sequence and minimizes the delay in the measurement of V_{ds} between the $V-$ and cathode pins during turn-on.

C. Gate Control Circuit Implementation

The dynamic characteristic and the switching event management presented in Section III-A are obtained by means of the gate control circuit. Taking into account the details of the current-sensing solution, the latter implements a sequential strategy intended to improve the immunity of the device against perturbations. The operation of the gate control is shown in the time diagram in Fig. 10. At the time t_{start} , the turn-on order of the switch is sent. A pulse is provided to the input signal “ $vgcom$,” and the MOSFET gate command signal “ vg ” is set to “1.” The first rising edge, due to this switching event, is detected on the output “ $vcomp$ ” of the comparator. This undesired event must be masked, and a temporal filter, named “ $delay_1$,” is implemented for this purpose.

The converter which uses the synthesized switch is characterized by a current waveform which necessarily reaches the zero value. During this transition to zero of the current I_{sw} , the second rising edge on signal “ $vcomp$ ” occurs, and it will start the sequence of the MOSFET turnoff.

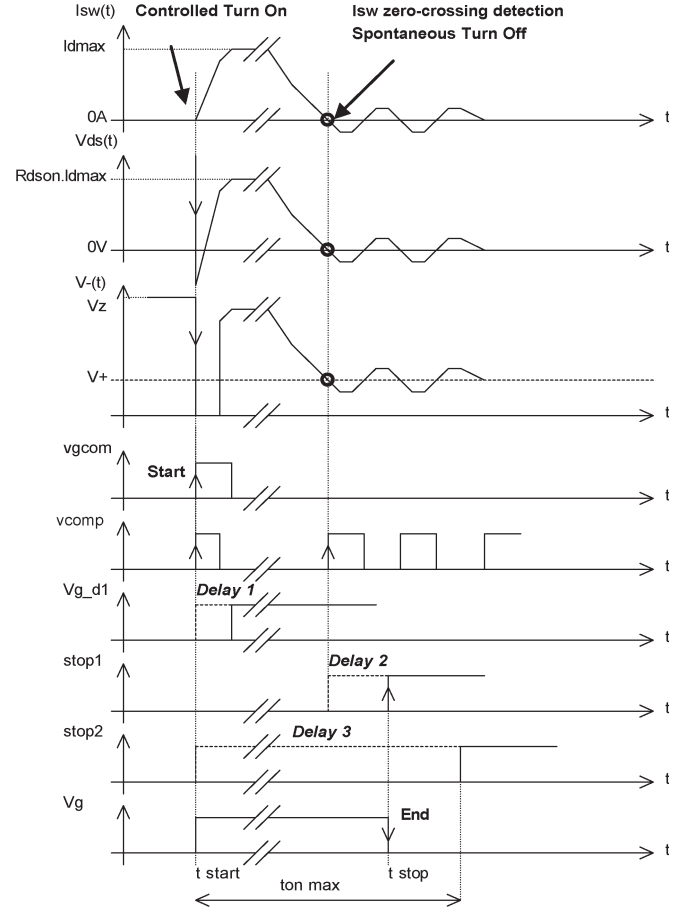


Fig. 10. Time diagram of signals of gate control circuit. “ $vgcom$ ” is command signal. “ vg ” is status of the MOS transistor.

After the second delay, named “ $delay_2$,” a stop signal called “ $stop_1$ ” is set to “1” and leads to the MOSFET turnoff. This delay is implemented to guarantee a correct diode D recovery time and to be sure that the HV diode is actually off.

For safety purposes, if no zero-crossing event is detected after a certain time (“ $delay_3$ ”), a signal “ $stop_2$ ” is set to “1.”

A general stop signal, named “ $stop$,” is used to force the MOSFET turnoff [see (3)] and to reset the control logic. It is important to remark, however, that a specific reset is needed during power-up of the system. A power-on-reset circuit is added and provides a “ por ” signal which is set to “1” during a short delay at start-up

$$stop = stop_1 \text{ OR } stop_2 \text{ OR } por. \quad (3)$$

For a strong integration purpose, the circuit dedicated to drive and control the gate of the MOSFET must be as simple and compact as possible. Fig. 11 shows the realization of this gate control circuit. Only two D-latch cells are necessary to detect the important events:

- 1) D-latch 1: M forced turn-on command given by “ $vgcom$,”
- 2) D-latch 2: detection of zero crossings of I_{sw} .

The three delays are introduced by means of RC cells which allow the easy tune of timers. It should be noted that it is important to reset those cells when a “ $stop$ ” signal occurs in

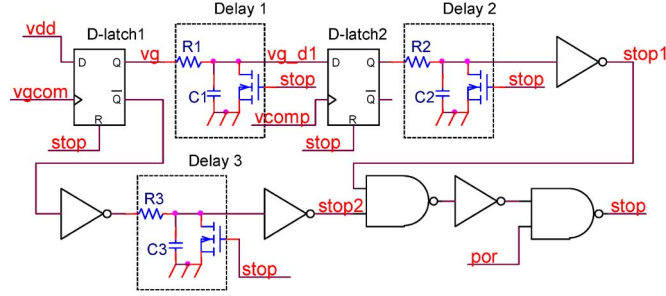


Fig. 11. Circuit of the MOSFET gate control.

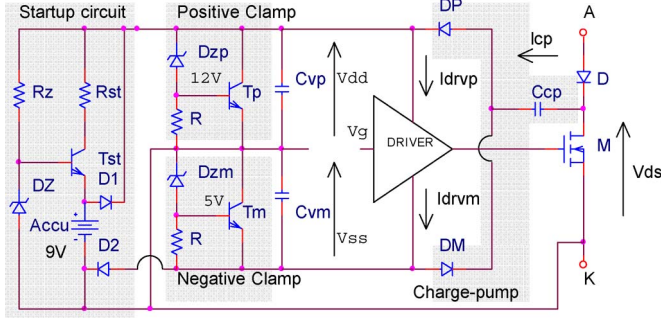


Fig. 12. Self-powered circuit description. The driver receives the vg signal, defined in Figs. 10 and 11.

order to avoid a memory effect for the following sequence. This reset is done by activating a transistor in parallel with each delay cell.

Other needed stages are added around the logic circuit.

- 1) Optoelectronic link used to send the TTL $vgcom$ signal: this isolated link allows the use of several synthesized thyristors in an HV environment with very fast switching abilities.
- 2) Level shifter used to adjust the vg signal to the required voltages at the gate of the MOSFET (+15 V/ - 5 V).
- 3) MOSFET driver.

D. Self-Powered Circuit

As this synthesized thyristor must behave like a three-terminal switch and bearing in mind that it could be used in the high side of a floating bridge configuration, which is a rather harsh environment, it is interesting to build in a self-powered circuit [19]–[22], [31]. This circuit supplies the MOSFET driver taking the energy from the main application.

1) *Self-Powered Circuit Principle*: The self-powered circuit is based on an ac/dc charge-pump converter. Indeed, it is possible to take advantage of the voltage across the MOSFET V_{ds} since it is a largely varying periodic waveform. From this voltage, positive and negative dc levels V_{dd} and V_{ss} are generated to supply the MOSFET driver. Fig. 12 shows the proposed electrical circuit.

As the V_{ds} signal is an alternate waveform, charges can be transferred to the circuit via the capacitance C_{cp} . Fig. 13 shows the resulting capacitance current waveform obtained for a given V_{ds} voltage behavior (similar to the simulation shown in Fig. 5). With a frequency F_{sw} and an amplitude ΔV_{ds} , the charges

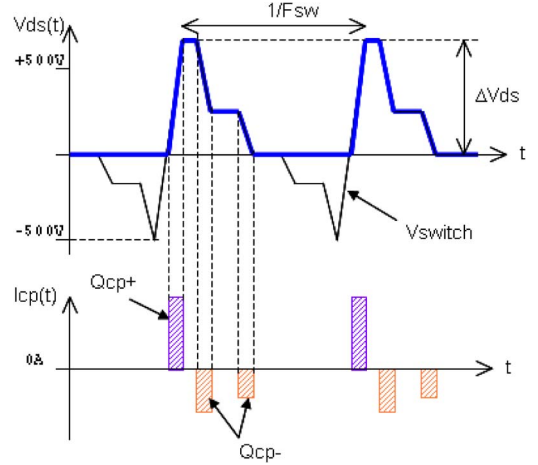


Fig. 13. Idealized V_{switch} voltage, associated V_{ds} waveform, and charge pump C_{cp} current waveform.

transferred during each switching period by means of the C_{cp} capacitance are given as follows:

$$Q_{cp+} = C_{cp} \cdot (\Delta V_{ds} - V_{dd}) \approx C_{cp} \cdot \Delta V_{ds} \quad (4)$$

$$Q_{cp-} = C_{cp} \cdot (\Delta V_{ds} - V_{ss}) \approx C_{cp} \cdot \Delta V_{ds}. \quad (5)$$

This results in positive and negative average currents

$$I_{cp+} = I_{cp-} = C_{cp} \cdot \Delta V_{ds} \cdot F_{sw}. \quad (6)$$

Knowing the average current I_{drv} of the driver, the value of the minimal capacitance $C_{cp\min}$ is computed, as given in the following:

$$C_{cp\min} = \frac{I_{drv}}{\Delta V_{ds} \cdot F_{sw}}. \quad (7)$$

Slightly higher capacitance values are chosen to guarantee the operation of the circuit. C_{vp} and C_{vm} capacitances are introduced as energy storage capacitors, providing a small voltage ripple. The following expressions are proposed to calculate these values:

$$C_{vp} = 10 \cdot \frac{C_{cp} \cdot \Delta V_{ds}}{V_{dd}} \quad (8)$$

$$C_{vm} = 10 \cdot \frac{C_{cp} \cdot \Delta V_{ds}}{|V_{ss}|}. \quad (9)$$

In order to limit the supply voltage of the drivers V_{dd} and V_{ss} , two active clamping circuits are introduced. Dzp , R , and Tp correspond to the positive limitation circuit, while Dzm , R , and Tm correspond to the negative one.

2) *Start-up Circuit*: During the start-up of the power converter, the voltages across all the synthesized thyristors are constant and so are their V_{ds} . In this condition, the charge pump is not able to extract energy from the power circuit. Hence, it is necessary to use a small battery to supply the driver for the first switching cycles. This battery is an accumulator and is recharged using the circuit shown in the left side in Fig. 12.

At start-up, while the accumulator is supplying the circuit, V_{dd} and V_{ss} are 8.4 and -0.6 V, respectively. When the charge pump begins working, V_{dd} goes higher than 8.4 V; then, D_1 and

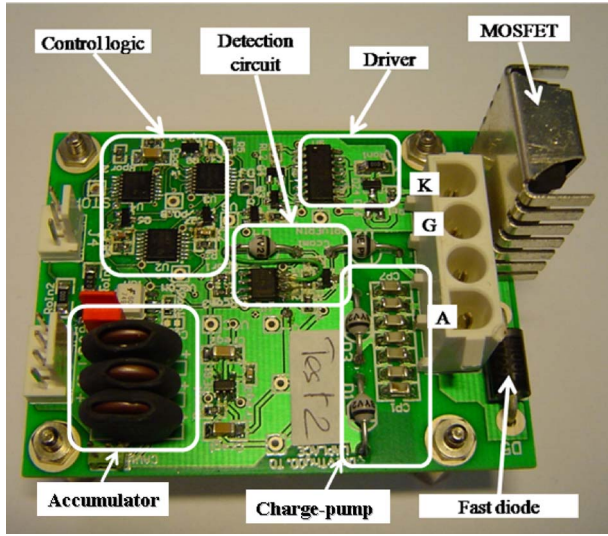


Fig. 14. High-frequency synthesized thyristor implementation.

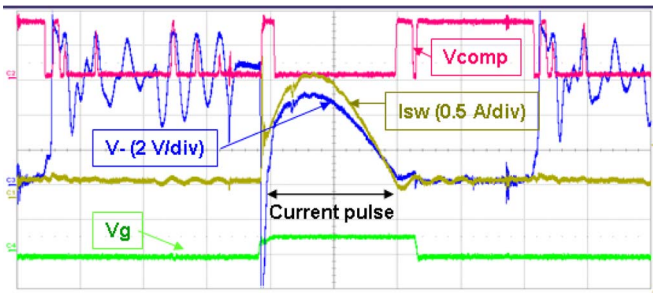


Fig. 15. Measurement of voltage $V-$ and detection of I_{sw} zero crossing. The current pulse I_{sw} is a magnified part of the i_L waveform (Fig. 18). Time base: $2 \mu\text{s}/\text{div}$.

D_2 turnoff and the charge of the accumulator start via the T_{st} transistor. The voltage of the D_z Zener diode is chosen slightly less than the battery voltage to stop the charge.

V. EXPERIMENTAL RESULTS

A. Synthesized Thyristor Implementation

A prototype of the high-speed synthesized thyristor, which can switch a peak current of 6 A, using surface-mount devices, has been realized on a $5 \times 4 \text{ cm}^2$ board, as shown in Fig. 14. MOSFET STW5NK100Z is used for the transistor M , and diode MUR4100 is used for the diode D . The entire circuit signals are referenced to the MOSFET source, and an implemented ground plane guarantees a good immunity to switching noise.

An experimental waveform of I_{sw} , during a conduction sequence, is shown in Fig. 15. In this figure, it can be seen that the $V-$ voltage reproduces with great accuracy the waveform of the I_{sw} current when M is at the ON state. System performances are directly linked to the accuracy and speed of the zero-crossing detection. The second rising edge presented by the “ $vcomp$ ” signal indicates this zero crossing with a very fast time response ($< 60 \text{ ns}$). In the zero-crossing detection circuit, a high-speed comparator LM319 is used to reach this performance.

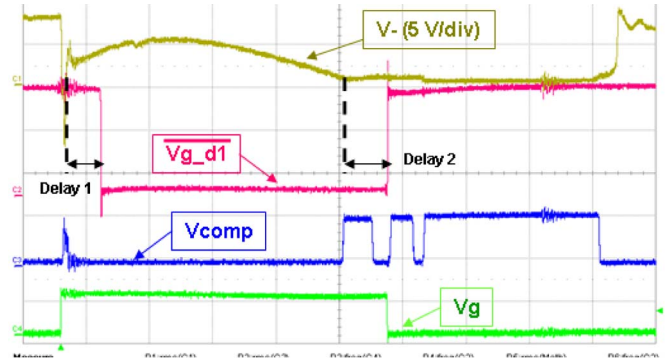


Fig. 16. Measurement of gate control circuit signals. Time base: $1 \mu\text{s}/\text{div}$.

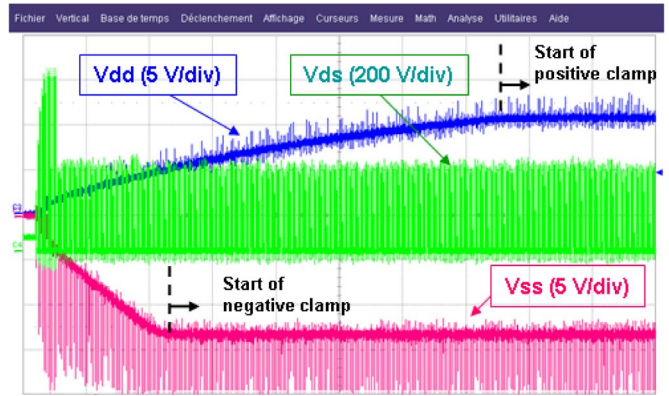


Fig. 17. Internal supply start-up behavior using self-powered circuit; waveforms of V_{dd} , V_{ss} , and V_{ds} . Time base: $500 \mu\text{s}/\text{div}$.

As can be seen, the signal $V-$ reproduces exactly the behavior of I_{sw} only after a delay of $1 \mu\text{s}$. This delay can be reduced by adjusting the values of $R1$ and $C1$ (Fig. 9).

Fig. 16 shows the main experimental signals of the gate control circuit. Signal vg_d1 is set to “1” 600 ns after M is turned on ($delay_1$). Therefore, the first rising edge of $vcomp$ is ignored.

When I_{sw} zero crossing occurs, the signal $stop$ is set to “1” after 800 ns ($delay_2$), and signal vg goes to “0.” As this signal vg indicates the state of the MOSFET gate, a switch-off order is provided.

Note that these signals are obtained in accordance with the expected principle shown in Fig. 10.

Fig. 17 shows the time behavior of the self-powered circuit. At system start-up, V_{dd} and V_{ss} voltages reach 10 V in 3.5 ms and -5 V in 1 ms, respectively. The values used for the capacitors are $C_{cp} = 100 \text{ pF}$ and $C_{vp} = C_{vm} = 2 \mu\text{F}$ for $F_{sw} = 100 \text{ kHz}$ and $\Delta V_{ds} = 500 \text{ V}$.

B. Current-Mode Converter

The power converter shown in Fig. 3 is implemented using three high-speed synthesized thyristors. The operating principle shown previously in Fig. 4 is satisfied, with a unidirectional current in the inductance and a bidirectional current in the DBD lamp. The main current waveforms are shown in Fig. 18.

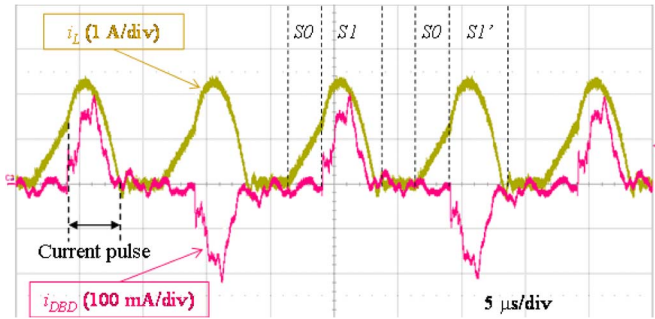


Fig. 18. DBD supplied with a current-mode converter, which uses three high-speed synthesized thyristors. Unidirectional signal is the inductance current. Bidirectional waveform corresponds to the DBD bidirectional current. Time base: 5 μ s/div.

VI. CONCLUSION

By using a fast MOSFET in series with an HV diode, the synthesis of a fast thyristor has been achieved. The high-speed performances of the circuit are obtained owing to the original principle of the transistor current sign detection. The drain-source voltage of the MOSFET provides a good estimation of its drain current value during the ON state. Directly driven by a compatible TTL signal via an optoelectronic link, this new “component” reproduces the characteristics of a thyristor for applications operating at several hundreds of kilohertz; additionally, the driver and the management circuit are supplied with a specific self-powered circuit which takes the necessary energy from the application circuit. These performances make this synthesized component particularly well suited for the control of the power transfer to capacitive loads, as DBD lamps.

The synthesized switch described in this paper has been used for the realization of a current-controlled converter, specially designed for the supply of DBD UV excilamps. This experimental validation, as well as the obtained performances, has confirmed the principles of this innovative solution and offers today new degrees of freedom for the control of the UV emission produced by DBD excimer lamps.

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