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A Review of Research on the Effect of Aging on the EMC of Integrated Circuits

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Abstract—Electromagnetic compatibility (EMC) is an essential requirement to electronic systems in which integrated circuits have a major influence. Intrinsic degradation mechanisms, which produces anticipated wear-out in deep submicron components threat not only the reliability of circuits, but also EMC performances. The need to predict and ensure long-term EMC has become a key challenge. This paper aims at presenting the last results on the long-term EMC topic. The paper clarifies the effect of device degradation mechanisms on EMC level drifts during lifetime and presents some attempts to predict these evolutions.

I. INTRODUCTION

Introducing new high performance and highly integrated electronic components and commercial off-the shelf (COTS) components in automotive, avionics and aerospace applications allows system manufacturers to reduce time to market delivery and manufacturing costs but forces them to analyze closely the reliability and life time with regard to the mission profiles of their applications. This trend has triggered off an increasing demand for conclusive statements about future lifetime and function of the product at early design stage, ranging from electromagnetic compatibility effects (EMC) to thermal management issues and thermo-mechanical reliability forecasts. EMC is a major requirement to electronic systems for years, in order to ensure low electromagnetic emission (EME) and susceptibility (EMS). In this way, electronic integrated circuits (ICs) are at the heart of EMC concerns as they may be both perturbing and perturbed elements.

During their lifetime, ICs may be affected by failure mechanisms mainly activated by harsh environmental conditions. Intrinsic degradation mechanisms, which produces anticipated wear-out in deep submicron components (e.g. features size 90nm and below), threat the reliability of circuits. Even if failure mechanisms may not compromise the circuit operation, IC intrinsic degradations can have a significant impact on EMC performances, as shown by recent research works. This issue is called "Long-Term EMC" [1].

This paper aims at presenting the last results on the long-term EMC topic, with a special focus on DSM components. The paper clarifies the effect of device degradation mechanisms on EME and EMS level drifts during lifetime. The paper present some attempts to predict these evolutions.

II. IDENTIFICATION OF CMOS DEVICE DEGRADATION MECHANISMS AFFECTING EMC

During their lifetime, CMOS devices are affected by intrinsic failure mechanisms, such as Electro Migration (EM), Hot Carrier Injection (HCI), Negative Bias Temperature Instability (NBTI), Time Dependent Dielectric Breakdown (TDDB), mainly activated by harsh environmental conditions such as high or low temperature and electrical overstress. Among them, HCI and NBTI are the major contributors to the device electrical performance degradation in advanced CMOS technologies, since they contribute to gate oxide layer degradation. The degree of degradation of a device and, hence, its lifetime depend on the stress level and duration (Table I). In return, these degradation at gate level may have a major roles in gradual changes of IC emission and immunity levels, since they affect electrical behavior of internal functions such as noise margins, jitters, current consumptions, delays.

TABLE I. IMPACT OF OXIDE DEFECTS BASED DEGRADATION MECHANISMS

	HCI	NBTI
<i>Transistor type</i>	<i>NMOS</i>	<i>PMOS</i>
Acceleration factors	High V _{ds} , low temperature	High V _{gs} , high temperature
Threshold voltage V _{TH}	Increase	Increase
Mobility μ	Decrease	Decrease
Drain current	Decrease	Decrease
Other	Substrate current increase	I _{off} current increase

III. EFFECT OF CIRCUIT AGING ON ELECTROMAGNETIC EMISSION

These last years, numerous experimental studies consisting in emission measurements combined with accelerated-aging conditions have been done on various type of ICs (small digital cores [2], oscillators [3], I/O buffers [4]) designed in CMOS 0.25 μ m, 90 nm and 65 nm technologies. Globally, the same conclusion has been drawn from all these experiments: applying electrical or thermal stress to ICs leads to a time dependent reduction of the power integrity issues, conducted and radiated EME, whatever its technology. The technology changes only the sensitivity to stress conditions.

The studies presented in [3] clarify the link between the intrinsic degradation mechanisms accelerated by electrical stresses in a CMOS 90 nm technology and the variation of electromagnetic noise produced by I/O buffers and digital blocks. A test chip containing NMOS and PMOS transistors with various sizes and digital structures is characterized under electrical stress conditions. Fig. 1-a shows the evolution of the threshold voltage of PMOS transistors with stress time for two different stress conditions which activate NBTI mechanism. The threshold voltage increases gradually with stress time according to power law. Then, these conditions are applied on a digital circuit and the power supply voltage fluctuations and the evolution of conducted EME is measured.

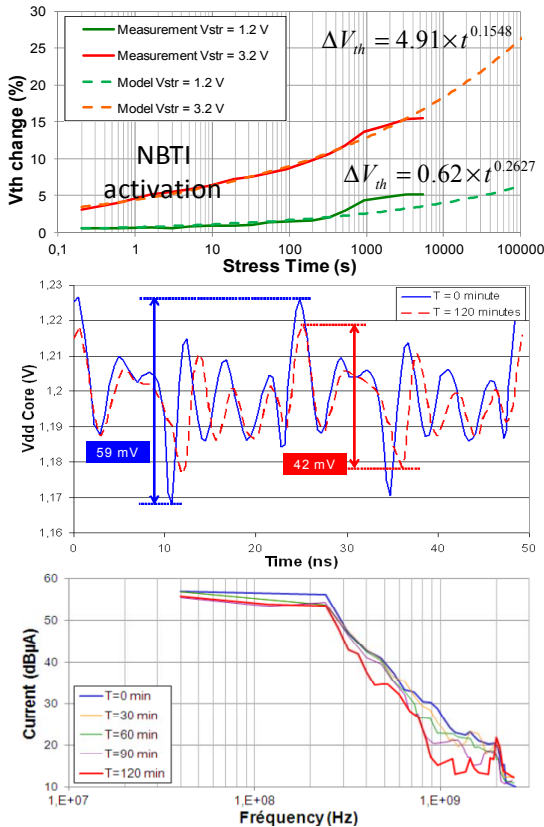


Fig. 1. (a) Link between NBTI (top) and power integrity and (b) conducted emission level; (c) evolutions of a CMOS 90 nm digital circuit [3]

Fig.1-b shows that the power supply drops due to the switching activity of the digital core are decreasing with stress time. The analysis of EME in frequency domain shown in Fig. 1-c shows that the spectral content of the conducted noise is reduced, especially in high frequency. The circuit remains operational during all the stress period and its average current consumption is not affected. Only the timing characteristics such as propagation delays through the digital core increase.

Experimental analysis coupled with CAD simulation helps to understand the mechanisms which lead to the general reduction of the EME. It is associated to the reduction of the amplitude and the temporal spreading of the dynamic current consumption of the IC. The acceleration of degradation mechanisms such as NBTI leads to decrease of transistor drive current and the increase of switching time, which have a direct

impact on EME. Predicting the drift of IC emission relies on an accurate modeling of the evolution of dynamic current consumption. In [5], an aging-aware EME model of the previous CMOS 90 nm digital circuit is built. From the IC netlist and the empirical relations between transistor parameters and electrical stress condition and durations extracted from measurements, an equivalent macromodel is constructed. Fig. 2 presents the simulation of the evolution of the conducted emission spectrum when the digital core is exposed to an electrical stress. The model is able to predict with a quite good accuracy the time-dependent reduction of the conducted emission spectrum up to 1 GHz. This result demonstrates that a simple and non confidential model ensures a reasonable estimation of the evolution of the EME.

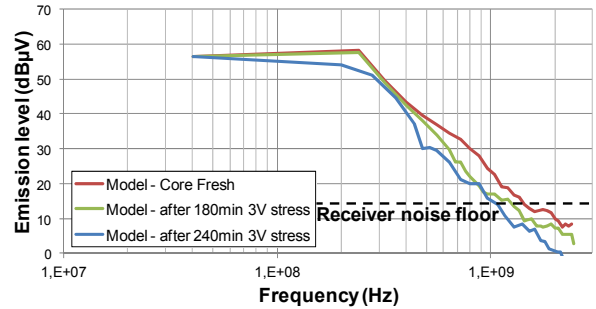


Fig. 2. Simulation of the evolution of the conducted emission of a CMOS 90 nm digital core exposed to a 3 V electrical stress [5]

Although these results are very positive for the control of EME at IC level, the impact of aging on EME should not be overlooked. Around the IC, passive devices such as capacitors, inductors or ferrites constitute efficient filtering elements of EME. However, their characteristics drift under high temperature and high voltage conditions leading to a significant increase of conducted and radiated EME over large frequency ranges, as shown in [6].

IV. EFFECT OF CIRCUIT AGING ON ELECTROMAGNETIC SUSCEPTIBILITY

Comparing to the conclusion drawn about the impact of aging on EME, the effect of aging on EMS is less straightforward. Numerous studies have been led these last years to clarify the impact of aging on DSM circuit susceptibility to electromagnetic interferences. Several types of functions have been tested such as digital circuits [7], I/O buffers, phase-locked loop [8], voltage regulator, bandgap voltage reference and operational amplifiers [9] designed in CMOS 0.25 µm, 90 nm, 65 nm. Both positive and negative variations of the susceptibility levels have been measured after aging accelerated by electrical or thermal stresses, depending on the nature and the design of the tested functions.

The following example is proposed to illustrate the potential effect of aging on EMS of ICs [9]. A low dropout (LDO) voltage regulator designed in CMOS 90 nm technology is electrically stressed by applying high bias voltage on its power supply. This function is sensitive to electromagnetic disturbance applied on its power supply, which produces DC offset on its output. Its susceptibility to electromagnetic

disturbances applied on its power supply is characterized according to stress time. Fig. 3 presents the evolution of EMS level after several stress period T equal to 24 hours. Although the regulator is still functional in nominal conditions, the susceptibility level is gradually reduced over a large frequency range.

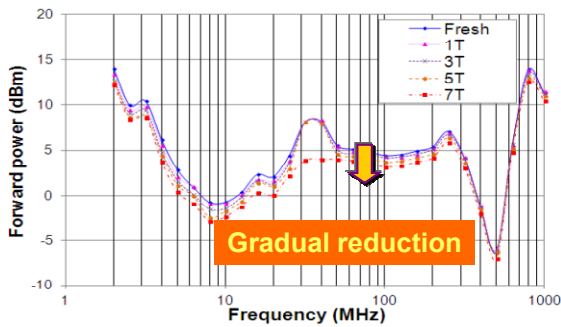


Fig. 3. Effect of electrical stress on conducted susceptibility of a CMOS 90 nm LDO regulator [9]

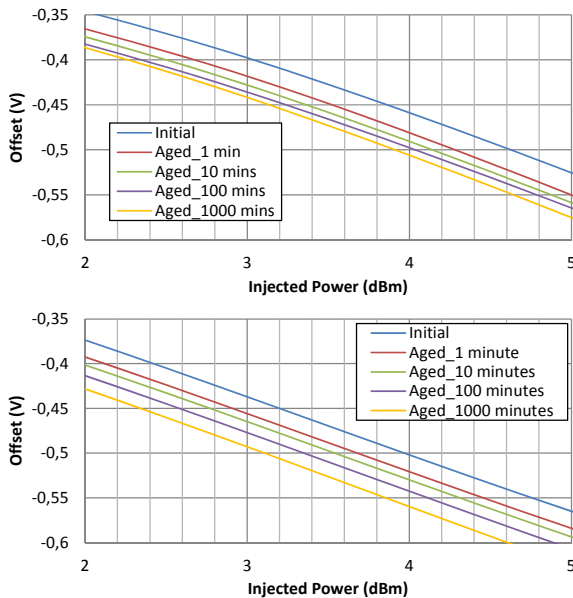


Fig. 4. Measurement (top) and simulation (bottom) of the opa offset voltage vs. disturbance amplitude and electrical stress time [13]

Experimental characterization of degradation mechanisms at transistor level and CAD simulations are necessary to understand the origin of the EMS increase. The increase of power supply voltage leads to an acceleration of NBTI in some PMOS transistors of the circuit, especially the bias transistor in an internal operational amplifier (opa) of the regulator. In [10], an aging-aware susceptibility model of a CMOS 90 nm opa mounted in voltage follower configuration is built. The opa is mounted in follower configuration. The circuit is also submitted to electrical stress conditions that accelerate NBTI on PMOS devices. The change of their threshold voltages has been characterized experimentally and its dependence according to stress voltage and duration is modeled by an empirical relation. The threshold voltage

variation with stress time is then included in the transistor netlist in order to simulate the evolution of the susceptibility level according to the stress time. Fig. 4 presents the measured and simulated evolution of opa output offset vs. the amplitude of a 200 MHz harmonic disturbance after various stress time. The simulation predicts correctly the increase of the offset voltage with stress time. The CAD-based analysis helps to understand the origin of the increase of the induced DC offset after aging. The increase of the threshold voltage due to NBTI leads to an increase of the slew rate of the opa and differential pair bias current. Although the opa remains functional in nominal conditions, it has a serious impact on the generation of DC offset due to electromagnetic disturbances.

V. CONCLUSION

The examples presented in the previous parts have shown that IC aging leads to a gradual drift of EME or EMS levels. Predicting the amount of variation is not straightforward since it depends on the function of the IC, the technology and the stress conditions. A major issue for manufacturers of embedded electronic systems, especially those which are intended to operate in harsh conditions, is the impact of the combined aging of all the embedded components of the electronic application. The questions that arise are: What are the risks of non compliance to EMC requirements? Are the margins sufficient or disproportionate to compensate aging effect on EMC level? The development of aging-aware equivalent IC model for EMC prediction constitutes a solution to this issue.

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