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# A Multi-Mode Signature Analyzer for Analog and Mixed Circuits

*M. Renovell<sup>1</sup> M. Lubaszewski<sup>2</sup> S. Mir<sup>3</sup> F. Azais<sup>1</sup> Y. Bertrand<sup>1</sup>*

*1: LIRMM-UM2 161 Rue Ada Université de Montpellier II 34392 Montpellier Cedex France Tel: (33)467418523*

*renovell@lirmm.fr*

*2: DELET/UFRGS Av Osvaldo Aranha esq. Sarmiento Leite 103 90035-190 Porto-Allegre Brazil Tel:(55)513163140*

*luba@iee.ufrgs.br*

*3: CNM(CSIC) Av R. Mercedes Universidad de Sevilla 41012 Sevilla Spain Tel:(34)54623811*

*mir@cnm.us.es*

## Abstract

In this paper a multi-mode signature analyser is proposed to be built into analog and mixed-signal integrated circuits. The analyser circuitry is based on analog integrators and can perform transient (with one integrator) and frequency (with two integrators) response compaction. The area overhead incurred can be very low, since the same signature analyser can be shared by several analog macros. Besides that, whenever integrators are available on-chip for functional purposes, they can be shared with the testing circuitry. Experiments carried on a Sallen-Key (transient response compaction) and on a biquad filter (frequency response compaction) showed that a very high coverage of catastrophic and parametric faults can be obtained by using the proposed multi-mode signature analyser.

## Keywords

VLSI Integrated Circuit. Test. Analog and Mixed Signal Circuit. BIST.

## 1. INTRODUCTION

With the advances on analog-digital integrated circuits, faster and more complex test equipments are required to meet ever more severe test specifications. An attractive alternative to simplify the test equipment is to move some or all of the tester functions onto the chip itself. The use of Built-In-Self-Test for high volume production of mixed signal ICs is desirable to reduce the cost per chip during production-time testing by the manufacturers. In addition, it helps to perform diagnosis in the field.

In the past few years, many published papers have been concerned with the definition of DFT techniques, but few papers are concerned with the implementation of self-test capabilities [Alqutayri, 92-Vazquez, 95]. The

implementation of self-test capabilities implies the use of either on-chip Test Pattern Generators (TPGs) or Output Response Analyzers (ORAs) or both. In case of analog or mixed integrated circuits, two types of Output Response Analyzers can be defined: Analyzers dedicated to multi-frequency response compaction called multi-frequency ORA and analyzers dedicated to transient response compaction called transient ORA.

In a mixed circuit, the response compaction can be performed either on a digital signal after analog to digital conversion [Nagi, 94] or directly on the analog signal. This paper deals with purely analog module that does not require analog to digital conversion. So, considering purely analog modules, only one proposition of frequential ORA has been published [Lubaszewski, 96]. And in the same way, only one proposition of transient ORA has been published [Renovell, 96]. The objective of this paper is to propose a purely analog Multi-Mode Signature Analyzer (MMSA) able to perform both multi-frequency and transient output response compaction. The ability of performing on-chip both multi-frequency and transient response compaction allows to take advantage of the complementarity of the two test approaches.

## 2. THE MULTI-MODE SIGNATURE ANALYZER

The analog Multi-Mode Signature Analyzer we propose is based on the use of two cascaded follower-integrators which can implement the transparent function or the integration function. Each follower-integrator is built from a configurable op-amp that has been proposed simultaneously by different authors [Renovell,95 - Vazquez, 95] . The basic principle of the configurable op-amp is given in figure 1.

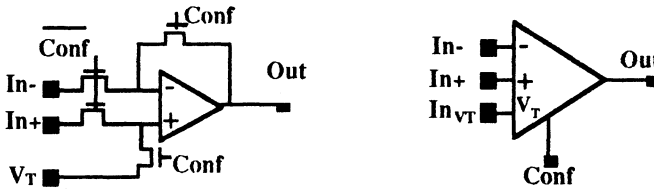


Figure 1 The configurable OPAMP

Considering a classical op-amp, a fully transparent module can be obtained by adding 4 switch-transistors in transparent mode  $Conf=1$ . Figure 1 gives the symbolic representation of the configurable op-amp with the additional input  $V_T$  and the control input  $Conf$ . The configurable op-amp can be used to build a follower-integrator. The basic principle of the follower-integrator is given in figure 2 using a switch capacitor implementation. When the control input  $Conf=1$ , the op-amp by-pass the passive R and C components and operates as a follower. When  $Conf=0$ , the op-amp ignores the  $V_T$  input and operates as an integrator.

It is well known that the input offset of operational amplifiers can lead to the output saturation of pure integrators. In case the error induced by the offset cannot

to be tolerated, we have chosen to embed an autozeroing circuitry [Gregorian,86] to cancel the offset. Then each integration stage can be modified according to the scheme given in figure 2. For simplicity, the module is represented without offset cancellation in the following sections.

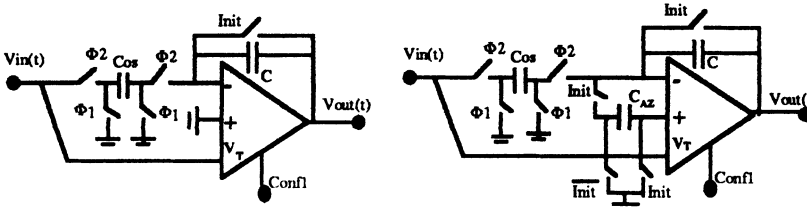


Figure 2 The follower-integrator module

By cascading two follower-integrators, we obtain the Multi-Mode Signature Analyzer as illustrated in figure 3. The different modes of operation are controlled by vector (Conf1,Conf2). When the configuration vector (Conf1,Conf2)=00 is used, the Multi-Mode Signature Analyzer performs a double integration and implements a multi-frequency ORA. When the configuration vector (Conf1,Conf2) = 01 or 10 is used, the Multi-Mode Signature Analyzer performs a single integration and implements a transient ORA. The detail of these modes are given in the following sections. Finally, when the configuration vector (Conf1,Conf2) = 11 is used, the Multi-Mode Signature Analyzer does not perform any integration and implements an analog SCAN register controlled by switches S1 and S2.

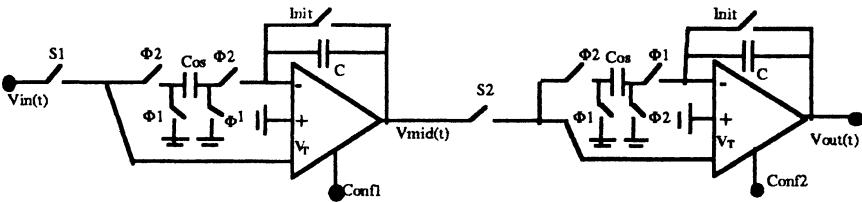


Figure 3 The Multi-Mode Signature Analyzer

### 3. THE MULTI-FREQUENCY RESPONSE ANALYZER

#### 3.1. Principle and Implementation

A multi-frequency ORA is obtained if the configuration vector (Conf1,Conf2)=00 is selected in the multi-mode signature analyzer with S1=S2=1. A signature is obtained by computing the time for the output of the second integrator to reach a predefined reference voltage ( $V_{ref}$ ). Assuming  $V_{in} = -V_0 \sin(\omega t + \phi)$  and  $V_C|_{t=0} = 0$ , it

can be shown that  $V_{mid} = -\frac{V_0}{\omega \tau} [\cos \phi - \cos(\omega \tau + \phi)]$  (1) and

$$V_{out} = \frac{V_0}{(\omega \tau)^2} [-\sin(\omega \tau + \phi) + \omega \tau \cdot \cos \phi + \sin \phi] \quad (2) \text{ where } \tau = RC = \frac{C}{f_{ck} \cdot C_{os}}$$

Considering no phase shift in the circuit under test ( $\varphi=0$ ), (2) becomes:

$$V_{out} = \frac{V_o}{(\omega\tau)^2} [a\tau - \sin(a\tau)] \quad (3)$$

Figure 4 shows the integration of a signal with  $V_0=1V$  and  $f=500Hz$ , with a time constant  $\tau=8.10^{-4}s$ . Due to the initial condition  $V_C|_{t=0}=0$ , the first integration results in a signal shifted above analog ground according to (1). Since  $\varphi=0$ , the second integration gives an increasing (monotonically) value for  $V_{out}$ .

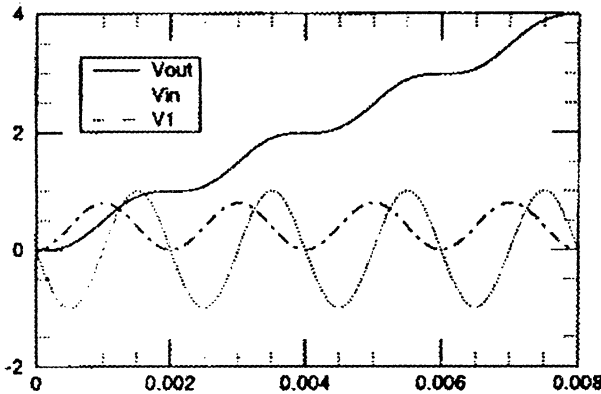


Figure 4 Double-integration effects for  $V_0=1V$ ,  $f=0.5kHz$  and  $\tau=0.8ms$ .

### 3.2. Fault coverage

Significant signal deviations result in general in different time signatures. Nevertheless, for smaller frequencies and larger input voltages, the time signature may be approximately the same for a significant frequency window, leading to a limited coverage of parametric (soft) deviations. This loss in fault coverage can be alleviated by considering larger time constants. However, increasing  $\tau$ , although it increases soft fault detection, increases also testing time (time required to reach  $V_{ref}$ ). Secondly, it also increases the probability of false rejection. Table 1 summarizes the influence of  $\tau$  in the valid input space, in fault detection, false rejection and testing time.

	Test Time	Parametric Deviation Detection	Valid Input Space	False Rejection
$\tau \uparrow$	$\uparrow$	$\uparrow$	$\downarrow$	$\uparrow$
$\tau \downarrow$	$\downarrow$	$\downarrow$	$\uparrow$	$\downarrow$

Table 1 The effects of  $\tau$  changes.

Considering two signals  $f_1(t)$  and  $f_2(t)$  of the valid input space, signature aliasing occurs when  $f_1(t)$  and  $f_2(t)$  result in approximately the same time signature:

$$\frac{1}{\tau^2} \int \int_0^n f_1(t).dt = V_{rf}, \quad \frac{1}{\tau^2} \int \int_0^n f_2(t).dt = V_{rf}, \quad (4) \quad t_1 \gg t_2$$

From equation [3] and neglecting the  $\sin(\omega_i t_i)$  terms, equation (4) implies:

$$\frac{V_{o1}}{\omega_1} t_1 \cong \frac{V_{o2}}{\omega_2} t_2 \Rightarrow \frac{V_{o1}}{f_1} \cong \frac{V_{o2}}{f_2} \quad (5)$$

Considering a linear aliasing behaviour as in equation (5), the aliasing can be illustrated by means of figure 5. Given a signal  $(V, f)$  in the input space, this signal is accepted to deviate in voltage/frequency an amount  $dV/df$  with respect to the nominal value. Considering a frequency deviation as in the case of signal  $(V, f)$  in figure 5, all signals within the highlighted cone should then leave the same signature. A deviation in voltage is illustrated for signal  $(V', f')$  in figure 5. Depending on the location of the signal in the input space, the aliasing cone will be larger for one type of deviation than the other.

Giving then a correct signal  $(V, f)$  with its corresponding signature, the probability that a faulty signal gives the same signature is the probability of the faulty signal falling within the aliasing cones. Considering that the faulty signal has the same probability of being anywhere in the input space, this can be calculated as follows.

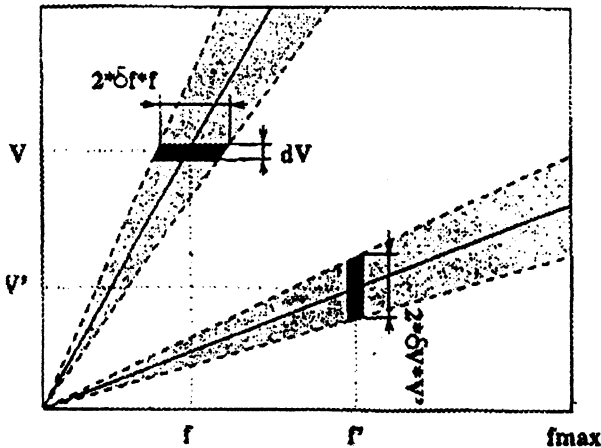


Figure 5 Aliasing probability computation.

In the case of the frequency deviation cone for  $(V, f)$ , the probability of aliasing is given by:

$$P_{alias\ worst\ case1} = \frac{\int_0^{V_{max}} 2 \cdot \delta f \cdot f \cdot dV}{f_{max} \cdot V_{max}} = \frac{\int_0^{V_{max}} 2 \cdot \delta f \cdot V \cdot \frac{f_{max}}{V_{max}} dV}{f_{max} \cdot V_{max}}, \quad P_{alias\ worst\ case1} = \frac{2 \cdot \delta f \cdot V_{max}^2}{V_{max}^2 \cdot 2} = \delta f.$$

In the case of the voltage deviation cone for  $(V', f')$ , the probability of aliasing gives:

$$P_{\text{alias worst case}} = \frac{\int_0^f 2 \cdot \delta V \cdot V \cdot df}{f_{\text{max}} \cdot V_{\text{max}}} = \frac{2 \cdot \delta V}{f_{\text{max}}} \frac{f_{\text{max}}^2}{2} = \delta V.$$

Depending on the location of the signal, the size of its aliasing cone will be different, but figure 5 illustrates the worst cases for frequency and voltage deviations. For any signal, the worst case aliasing probability is then given by:

$$P_{\text{aliasing worst case}} = \max(\delta f, \delta V) \quad (6)$$

Then, assuming that deviations of  $\pm 5\%$  are accepted for the nominal frequency and nominal voltage, the probability of aliasing in the worst case given by equation (6) will be 0.05. Finally, let us consider faults in the signature analyzer structure. In order to analyse the mutual influence of  $t$ ,  $w$  and  $\tau$ , let us isolate  $t$  in equation (3) for  $V_{\text{out}}=V_{\text{ref}}$  and derive the resulting expression with respect to  $\tau$ . Then,

neglecting the term  $\sin(wt)$ , we obtain: 
$$\frac{\delta t}{\delta \tau} = 2 \frac{V_{\text{ref}}}{V_0} \omega \tau \quad (7)$$

According to (7), the time signature  $t$  is more sensitive to  $\tau$  variations for large values of  $w$  (that justifies neglecting  $\sin(wt)$ ) and large values of  $\tau$ . Then, in order to ensure a good coverage of the signature analyzer faults, very low frequencies should be avoided.

### 3.3. Experimental Results

A discrete version of the switched-capacitor multifrequency signature analyser was used for testing the biquad filter of figure 6. The signature analyser was implemented in protoboard with  $C_{\text{os}}=2.2\text{nF}$  and  $C=22\text{nF}$ . The power supplies were set at +5V and -5V.

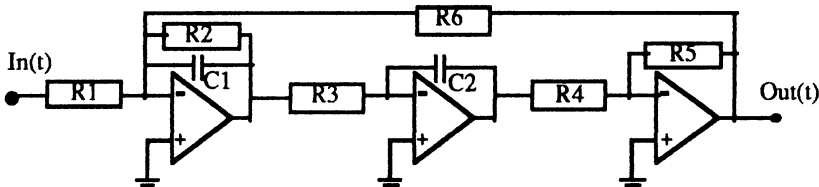


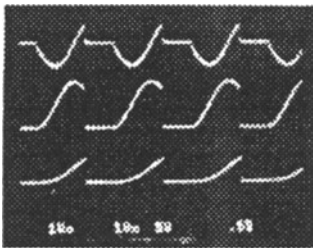
Figure 6 The circuit under test.

Two frequencies were applied to the circuit under test,  $f_1=721\text{Hz}$  and  $f_2=1442\text{Hz}$ . The fault set considered includes large deviations (-50% and +100%) of passive components. In order to reproduce in practice the simulation conditions of figure 4, signature analysis starts when, following a falling pass-by-zero of the test signal, the precomputed delay for the fault-free signal to reach analog ground elapses. The consideration of this delay is not required in normal test application. The signature computation ends when the analyser comparator signals that a threshold voltage  $V_{\text{ref}}=+4\text{V}$  was reached. Then the integration capacitors (C) are reset (Init=1 in both integration stages), the signature analyser input is disconnected from the filter output, and the analyser input is grounded. This procedure is performed cyclically in order to provide the oscilloscope with periodic waveforms. Figures 7(a and b) show,

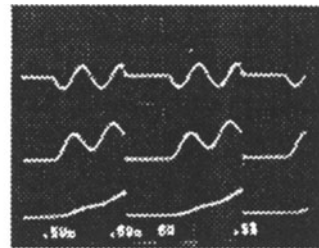
from top to bottom, the signals at the input of the analyser ( $V_{in}$ ) and at the outputs of the first ( $V_{mid}$ ) and the second integrator ( $V_{out}$ ), obtained for the fault-free biquad at 721Hz and 1442Hz respectively.

The experiments with the faulty filter consisted firstly in injecting component deviations of +100% and -50% ( $2.C_1$ ,  $C_1/2$ ,  $2.R_1$ , and  $R_1/2$ ) into the circuit and in computing time signatures. A 100% coverage is achieved for these passive component faults. The results obtained for the faults  $R_1/2$  and  $C_1/2$  are presented in figures 7(c and d). Fault  $R_1/2$  is detected at 721Hz and remains undetected at 1442Hz; fault  $C_1/2$  is detected at 1442Hz and remains undetected at 721Hz. From the analysis of the signals  $V_{in}$  (top),  $V_{mid}$  (middle) and  $V_{out}$  (bottom), it is clear that different signatures are obtained for phase and amplitude deviations.

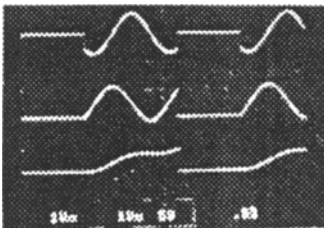
Secondly, although the precomputed frequencies originally did not consider the detection of small component deviations, deviations of  $\pm 20\%$  from the nominal values of resistors and capacitors were considered in our experiments. The fault coverage decreased slightly, especially due to components to which the filter output voltage is less sensitive for the frequencies applied. This is the case of capacitor  $C_1$ . If other nodes are observed and/or other test frequencies are applied, better sensitivity figures may be obtained. Finally, all faults injected into the signature analyser (switch shorts and opens, and capacitor deviations) were also detected.



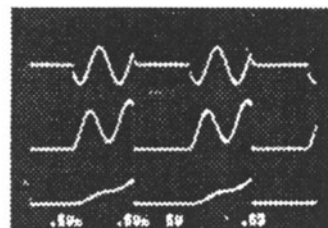
(a) fault-free biquad at 721Hz



(b) fault-free biquad at 1442Hz



(c) faulty biquad ( $R_1/2$ ) at 721Hz



(d) faulty biquad ( $C_1/2$ ) at 1442Hz

**Figure 7** Filter test results:  $V_{in}$  (top),  $V_{mid}$  (middle) and  $V_{out}$  (bottom).



## 4. THE TRANSIENT RESPONSE ANALYZER

### 4.1. Principle and Implementation

A transient ORA is obtained if the configuration vector (Conf1,Conf2)= 01 or 10 is selected in the multi-mode signature analyzer. When the Multi-Mode Signature Analyzer is configured with vector 01, the first stage corresponds to an integrator and the second one to a follower. The integrator implements the transient response compaction function, the follower is not absolutely required. However, the follower can be used after compaction to memorize the Analog Signature. The two switches in figure 3 controlled by S1 and Init are used for initialization and integration time control purposes.

The proposed transient ORA can be considered as an analog counterpart to the cumulative addition technique used by digital signature analyzers [Rajski, 92]. In integration mode (S1=1 and Init =0), the integration function is performed with a time constant RC. If the integration mode is held for a time interval [0; T<sub>i</sub>], the output value at the end of the integration time V<sub>out</sub>(T<sub>i</sub>) is equal to:

$$DS = O_1 + O_2 + \dots + O_n \Rightarrow AS = V_{out}(T_i) = - (1/RC) \int V_{in}(t) dt$$

### 4.2. Fault Coverage

To validate the implementation of the Multi-Mode Signature Analyzer in transient response compaction mode, the second order Sallen—Key filter of figure 8 has been studied. The validation is performed by SPICE simulations using a filter implementation with passive components in order to simulate hard faults on the passive components. Using a catastrophic fault model including 4 faults per MOS transistor (gate—drain and gate—source shorts, opens on drain and source contacts) together with 2 faults per passive component (short and open on resistances and capacitances), we determine the fault coverage of the filter. This fault coverage is calculated processing either the transient response O(t) during the test interval, or the analog signature AS delivered by the analyzer at the end of the test time. The input test stimulus is a pulse signal. This type of test stimulus has been identified as very efficient and is widely used for test purpose [Evans,90 - Alqutayri,92].

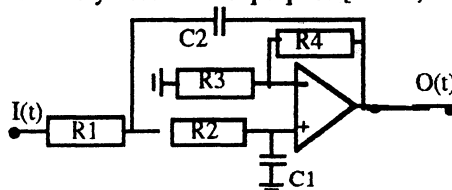


Figure 8 Second Order Sallen-Key Filter

Under these conditions, using a classical tolerance of 10% around the nominal response of the filter, 41 of 48 faults are detected when processing the transient

response. This off-chip time-domain analysis gives a fault coverage  $FC_{ref}$  equal to:  $FC_{ref} = 85.4\%$ .

In a second step, the fault coverage is established using the analog signature analyzer. The analyzer input is directly connected to the output node of the filter. Fault detection is then determined by a single comparison between the signature generated for faulty circuits and the pre-determined fault-free one, taking into account the same tolerance of 10%. Simulation results demonstrate that 40 of 48 faults are detected, that corresponds to a fault coverage  $FC_{AS}$  equal to:  $FC_{AS} = 83.3\%$ . Comparison between time-domain and signature analysis results shows that among the 41 faults normally detected when processing the transient response  $O(t)$ , 40 faults are detected when observing the analog signature AS. So, for this example, the aliasing problem occurs for only one fault of the list. This result points out that the continuous integration function can be considered as an efficient analog compression technique and that the proposed implementation of the analyzer perfectly works.

### 4.3. Improvement

On the basis of the analog signature analyzer presented above, we define a multiple-input module. Indeed, the analyzer is based on the classical opamp integrator and this integrator exists in both single and multiple-input versions. So, it is easy to define a multiple-input signature analyzer implementation, as described in figure 9. During the integration mode ( $S1=1$  and  $Init=0$ ), all the input signals  $V_{in1}, V_{in2}, \dots, V_{in_n}$  are integrated and the output signal  $V_{out}(t)$  is expressed by the following equation:  $AS = V_{out}(T_i) = - \sum (1/R_i C) \int V_{in_i}(t) dt$

The area overhead induced by the replacement of a single-input analyzer by a multiple-input one is very low: it is sufficient to add one resistor and one switch per additional input, a single opamp and a single capacitor being required to perform the integration.

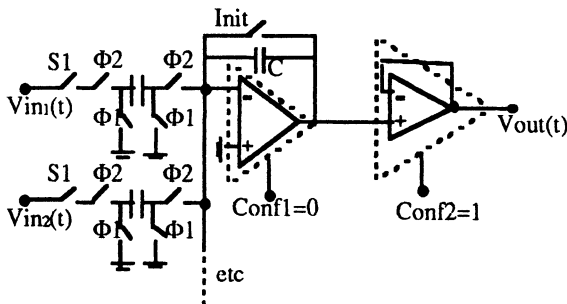


Figure 9 Multiple-Input Analog Signature Analyzer

This multiple-input signature analyzer can be considered as the analog counterpart to the digital Multiple-Input Shift Register (MISR). Analog circuits often present

few output pins, and frequently a single output pin (for example when dedicated to filtering applications). Considering a single output circuit, the interest of the Multiple-Input Analyzer consists in the observation of additional internal nodes. In fact, in this situation the multiple—input analyzer adds some extra observation points in the circuit, thus increasing the global observability. Observability is commonly accepted as one of the most important attribute of the testability, and so, by increasing the observability, we make the circuit more testable.

To illustrate this idea, we study the fault coverage achieved for the previous Sallen—Key filter using a 2—input signature analyzer. One input of the module is used to process the filter output node and the other constitutes the additional observation point. Obviously, this point has to be judiciously chosen to be able to get an increase in fault coverage. Starting with the remark that all the non—detected faults are faults inside the opamp, the additional observation point is chosen as an internal node of the opamp. So, the two analyzer inputs are connected to (i) the output node of the filter and (ii) the output node of the opamp differential stage. The SPICE simulations show that the new fault coverage  $FC_{AS^*}$  is equal to:  $FC_{AS^*} = 97.9\%$ .

Keeping in mind that the reference fault coverage achieved by an off—chip time—domain analysis is equal to  $FC_{ref}=85.4\%$ , we note a very significant increase when using the multiple—input analyzer. It has to be emphasized that usually, when using signature analysis techniques, the problem is to minimize the number of error masking phenomena in order to obtain a fault coverage as close as possible to the fault coverage achieved by an external test. With the multiple—input analog analyzer, not only we can partially overcome aliasing problems by introducing redundancy but also, we permit an improvement of the fault coverage. This solution consequently goes beyond the classical objectives of signature analysis techniques.

## 5. CONCLUSIONS

Similarly to the digital world, in the analog domain the off-chip analysis of output test responses requires a test equipment capable of extracting a high volume of data from the circuit under test and capable of properly processing these data. This kind of equipment is in general very expensive and takes a relatively long time to extract and process the test data. Those costs can be drastically reduced if a built-in output response analyser is used to perform test data compaction on-chip. Then a simple comparison of the computed analog signature to a reference value can provide a go/no-go indication outside the chip.

In this paper a multi-mode signature analyser is proposed to be built into analog and mixed-signal integrated circuits. The analyser circuitry is based on analog integrators and can perform transient (with one integrator) and frequency (with two integrators) response compaction. The area overhead incurred can be very low, since the same signature analyser can be shared by several analog macros. Besides that,

whenever integrators are available on-chip for functional purposes, they can be shared with the testing circuitry.

Experiments carried on a Sallen-Key (transient response compaction) and on a biquad filter (frequency response compaction) showed that a very high coverage of catastrophic and parametric faults can be obtained by using the proposed multi-mode signature analyser. It was also pointed out that existing aliasing problems can be alleviated by enhancing the observability of the circuit under test using the same signature analyser. In addition, the effects of the operational amplifiers offset on the integration stages were shown to be cancelled by an autozeroing circuitry.

Given the results above, one can conclude that the testability of analog and mixed-signal circuits can be greatly improved by using the multi-mode signature analyser proposed in this paper. This improvement can be achieved at a rather low cost when compared to the prices of commercially available test equipments.

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## 7. BIOGRAPHY

M. Renovell is a full CNRS researcher at LIRMM (Laboratoire d'Informatique Robotique et Microélectronique de Montpellier, France). His topics of interest are fault modelling and test of mixed signal circuits.

M. Lubaszewski is a professor at UFRGS (Federal University of Rio Grande de Sul) in Porto-Allegre (Brazil). His topics of interest are in test of analog and mixed signal circuits.

S. Mir is assistant professor at CNM (Centro Nacional de Microelectronica) in Sevilla (Spain). His topics of interest are design and test of analog and mixed signal circuits.

F Azais is a full CNRS (French National Council for Scientific Research) researcher at LIRMM (Laboratoire d'Informatique Robotique et Microélectronique de Montpellier, France). His topics of interest are in test of mixed signal circuits.

Y. Bertrand is professor at LIRMM (Laboratoire d'Informatique Robotique et Microélectronique de Montpellier, France). His topics of interest are fault modelling, test of sequential circuits and test of mixed signal circuits.