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BEOL-investigation on selfheating and SOA of SiGe HBT

**R. D'Esposito, S. Fregonese,
T. Zimmer**

Outline

- **SiGe HBTs for THz applications**
 - **Thermal issues in state of the art SiGe HBTs**
- Technologies under study: IFX B11HFC and ST B55
- Characterization of BEOL impact in single finger HBTs (IFX B11HFC)
- Physical modeling of the BEOL impact (IFX B11HFC)
- Impact of BEOL and transistor layout in multifinger HBTs (ST B55)
- Conclusions & future perspectives

Temperature issues in SiGe HBTs

High speed performances till sub-THz range

DTI
(poor thermal conductivity)

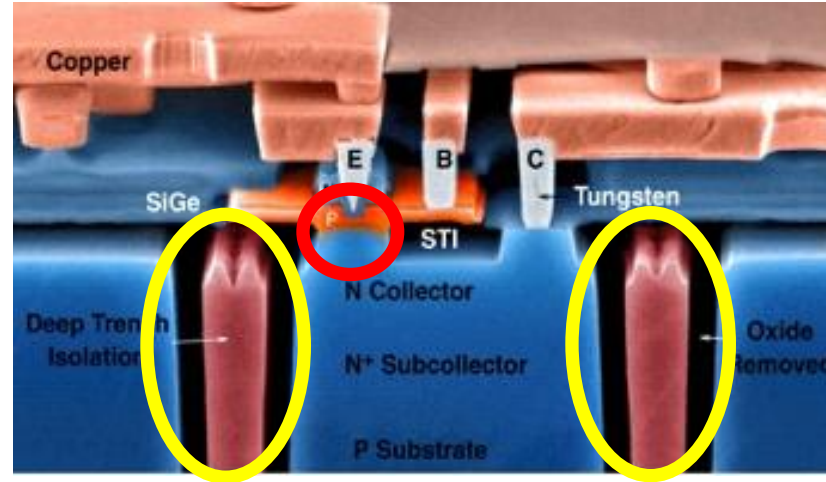
aggressive shrink of the active part

high current densities
high internal electric fields at the BC junction

can be modeled as a heat source

Serious thermal issues due to self-heating

- shift and deterioration of the DC and AC characteristics
- eventually device failure
- **positive electro-thermal feedback => electro-thermal loop**



<http://users.ece.gatech.edu/cressler/>

Scaling and high integration consequences

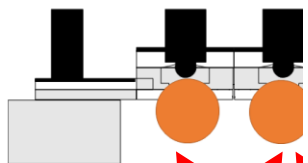
Device level:

multifingered architectures

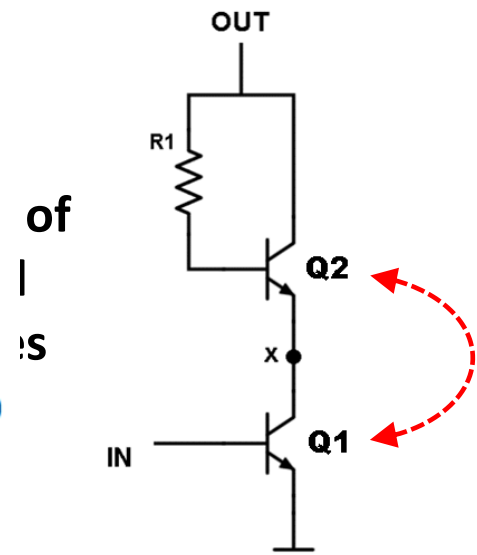
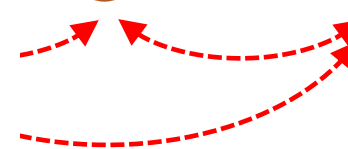
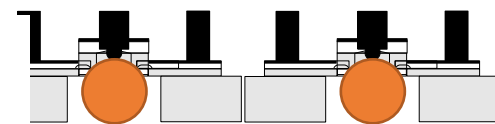
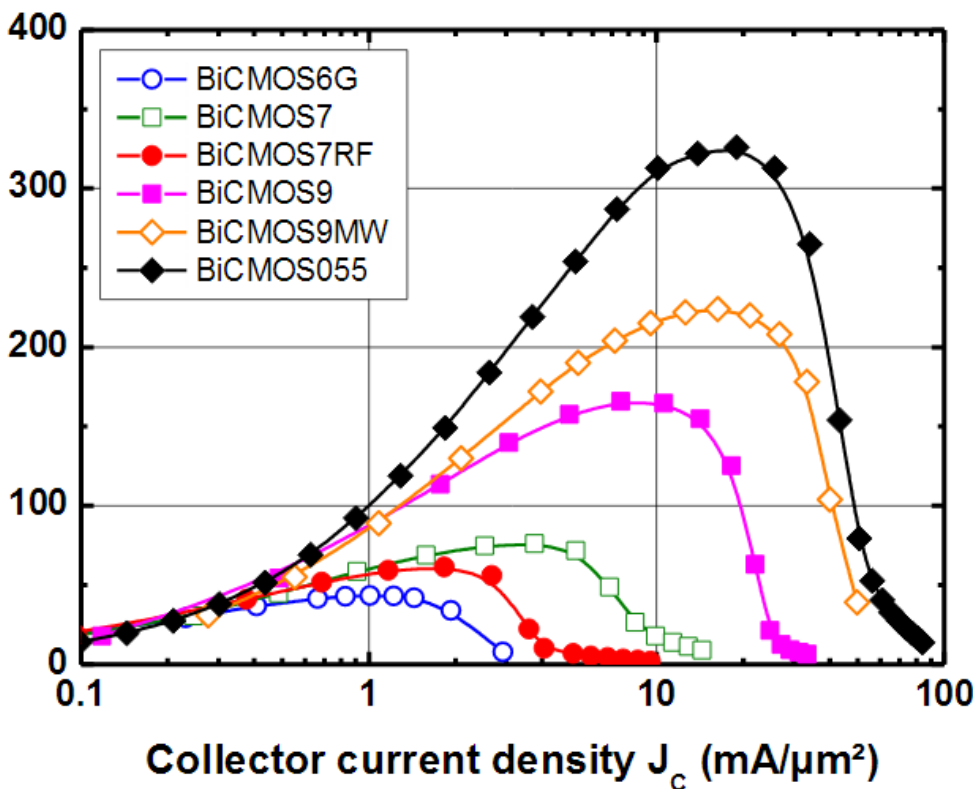
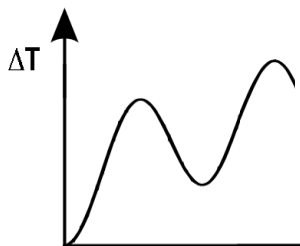
Scaling increases performances, but leads to higher J_c and thus to higher power densities

Circuit level:

higher density of components

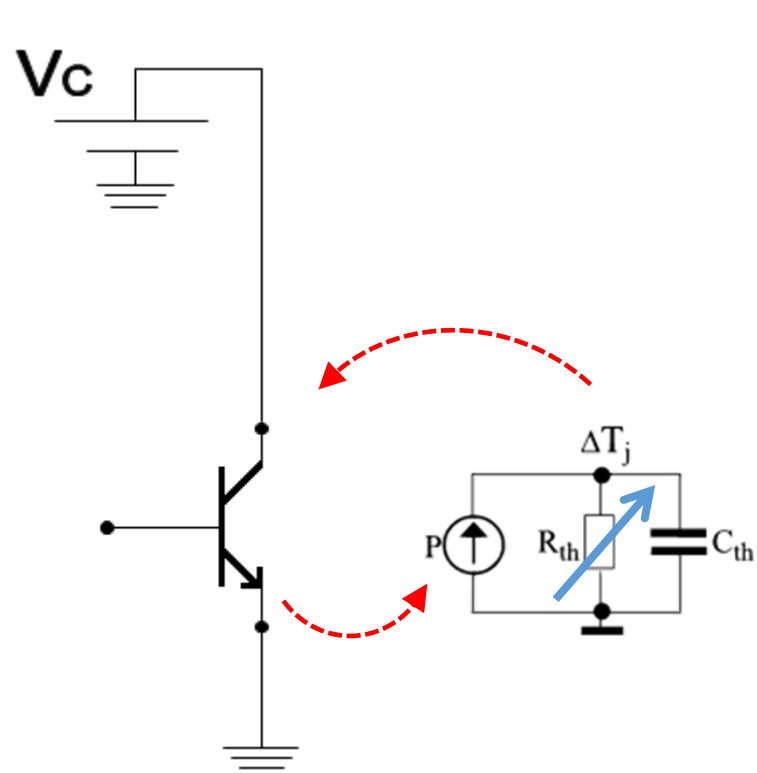


INTRA-DEVICE thermal coupling

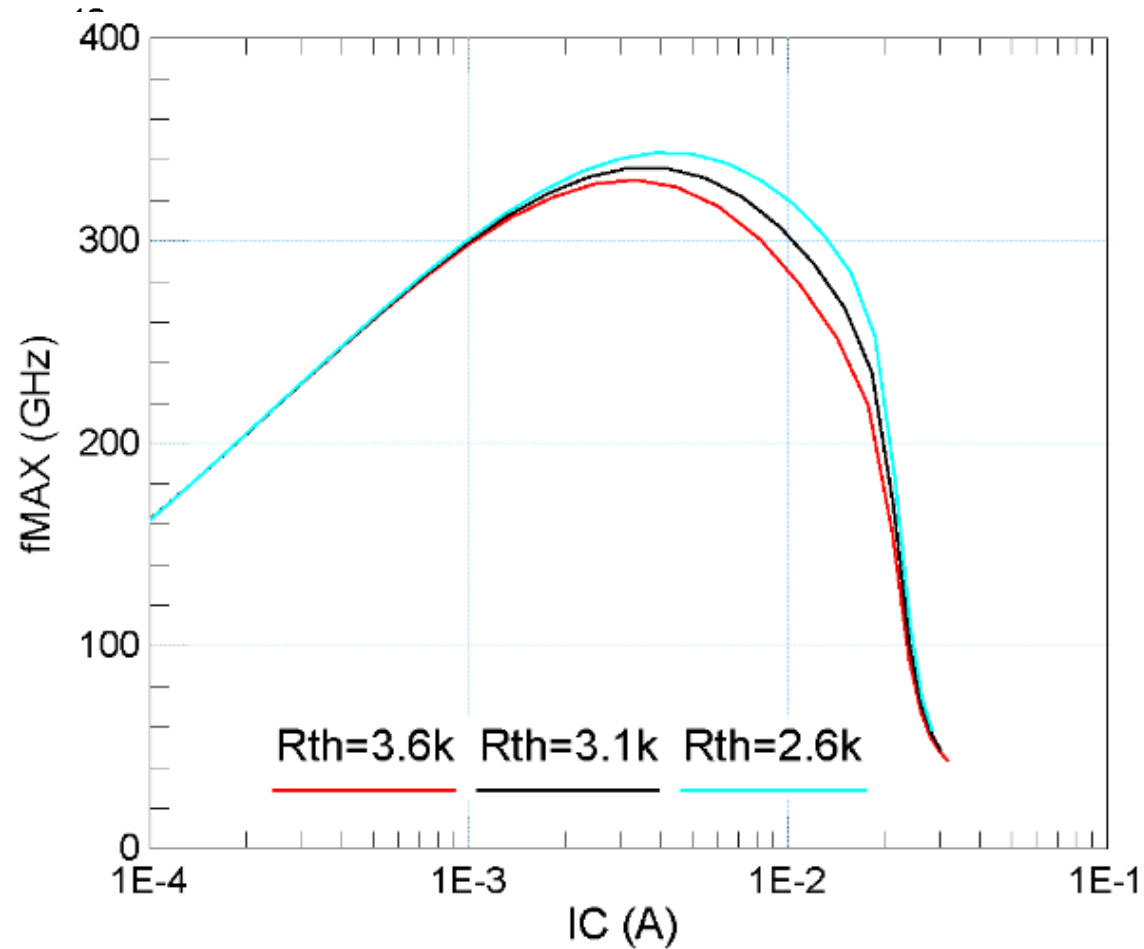


of
I
S

Effect of SH on device behavior: HiCuM simulations



A high value of R_{th} has a negative impact on the DC behavior: it leads to IC instability



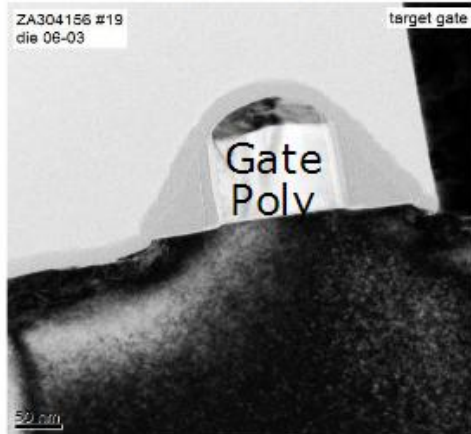
A high R_{th} decreases the f_T and f_{MAX} figures of merit

Outline

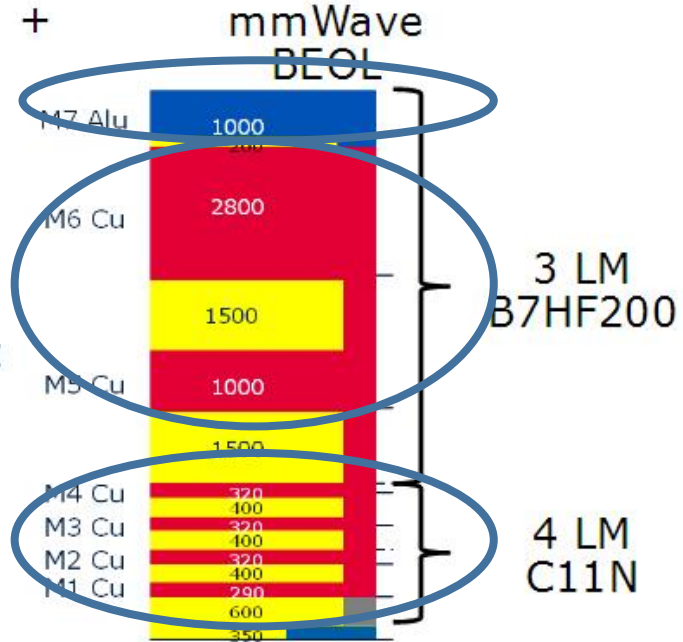
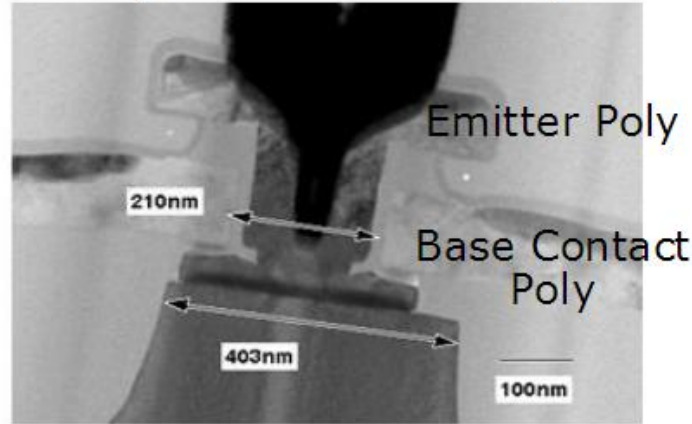
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Technologies under study: IFX B11HFC

130nm MOSFETs
(C11)



+ Scaled SiGe HBTs
(DOTFIVE SiGe HBT)

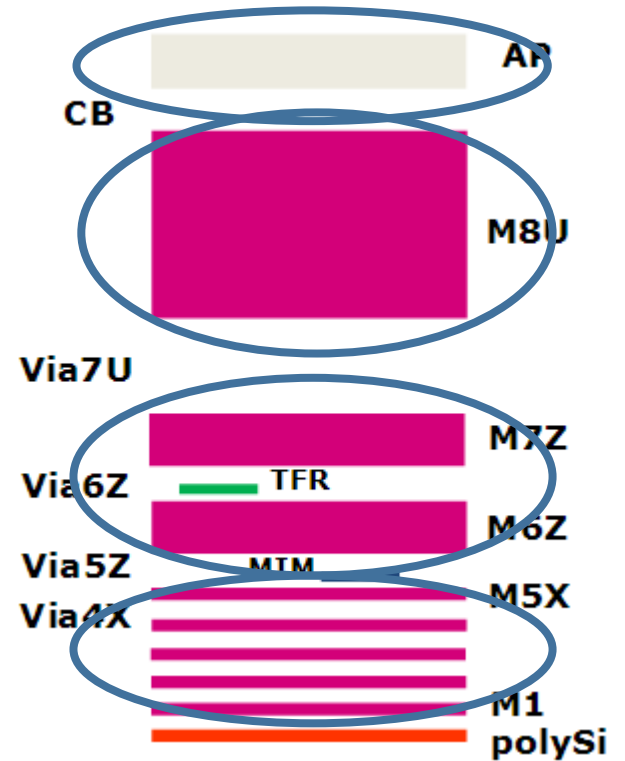
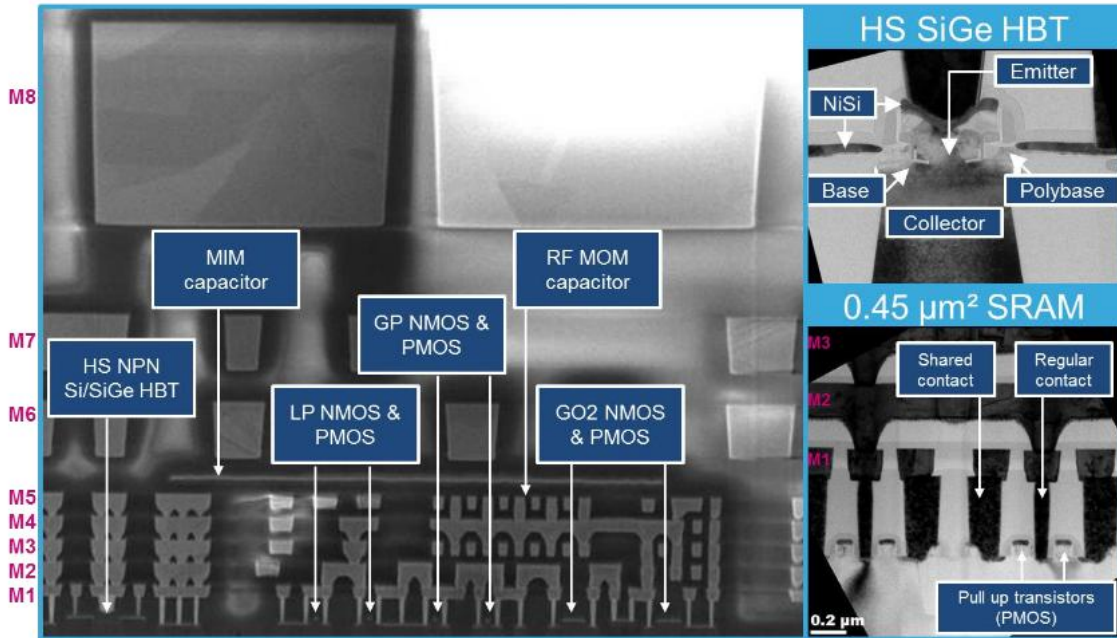


feature size	f_T	f_{MAX}	BV_{CBO}	BV_{CEO}
130nm	250GHz	370GHz	5.5V	1.5V

7 BEOL metals

- 4 thin Cu
- 2 thick Cu
- 1 Alu for pads

Technologies under study: ST B55



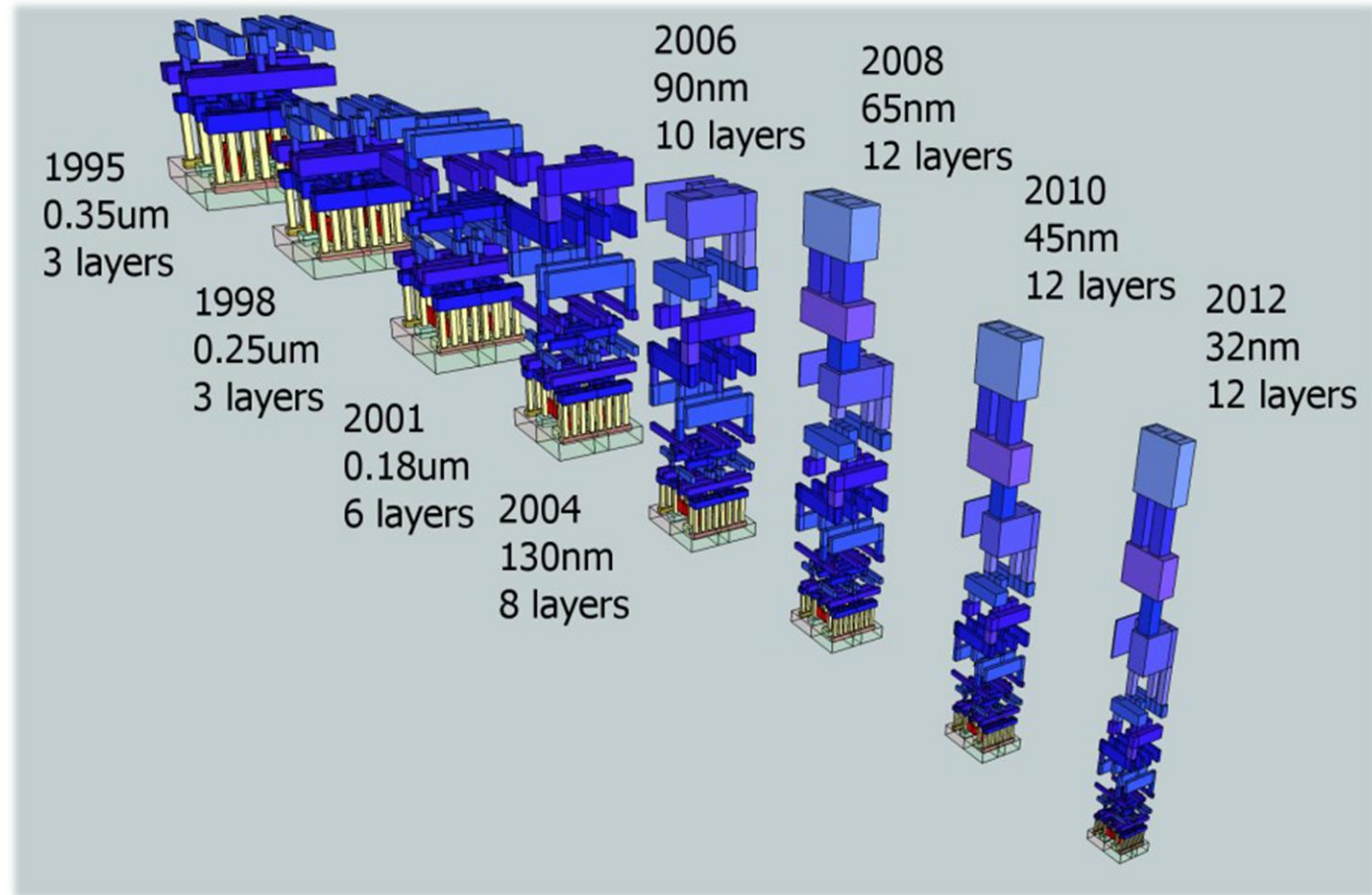
9 BEOL metals

- 5 thin Cu
- 2 medium Cu
- 1 thick Cu
- 1 Alu for pads

feature size	f_T	f_{MAX}	BV_{CBO}	BV_{CEO}
55nm	320GHz	370GHz	5.2V	1.5V

BEOL metallization evolution

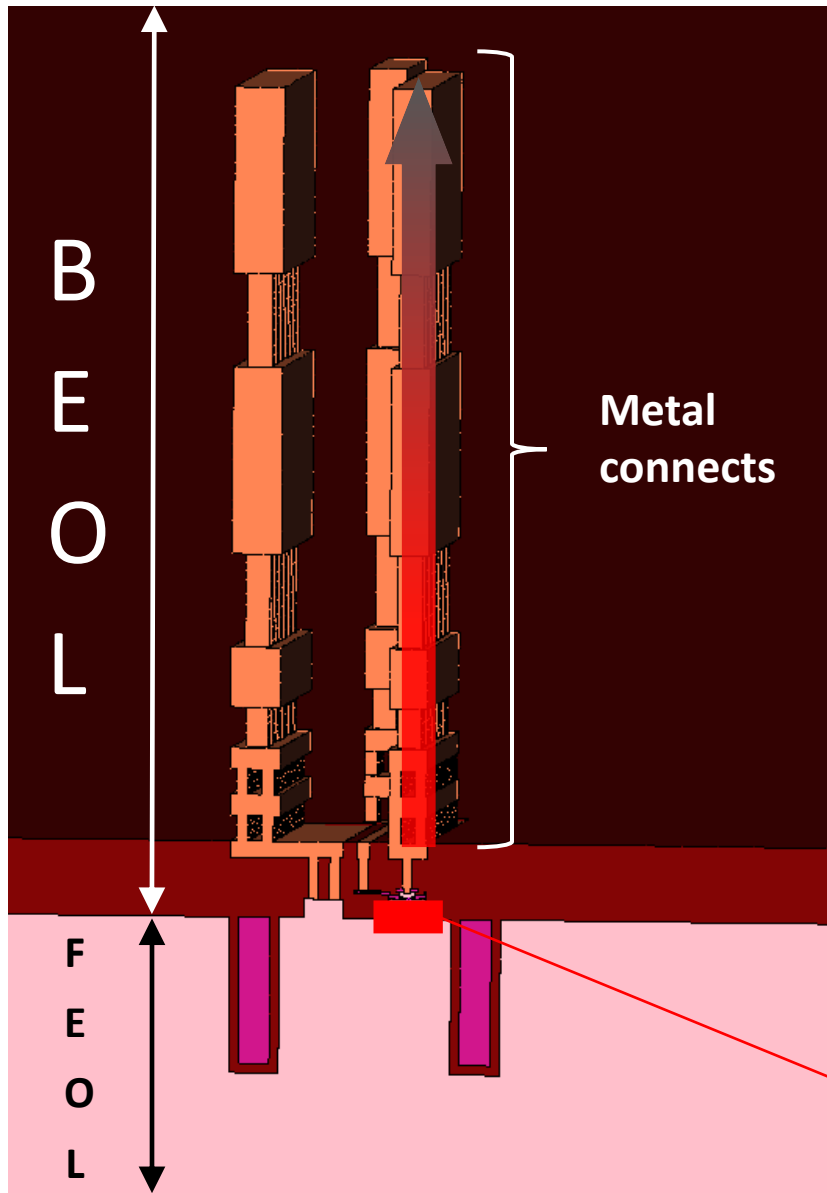
Evolution over time of a CMOS technology node



Akira Tsuchiya (Kyoto University, Japan)

- The dimensions of the active part of the transistors decreases
- The complexity of the BEOL increases

Scenario of the thermal impact of the BEOL



Thermal conductivity

FEOL Si → **1.54** W/cm K

BEOL SiO₂ → **0.014** W/cm K

BEOL Cu → **3.85** W/cm K

- Can the heat generated at the BC junction be dissipated through the metal stacks above it?
- How much the impact of the added metals on the behaviour of the component?
- Is it possible to model this effect to take it into account into circuit simulator?

HEAT SOURCE: BC junction

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Test structures to evaluate BEOL impact

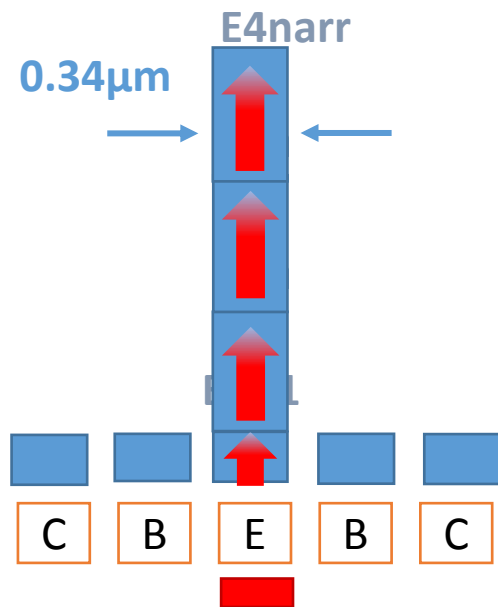
narr test set:

Minimum volume of metal added

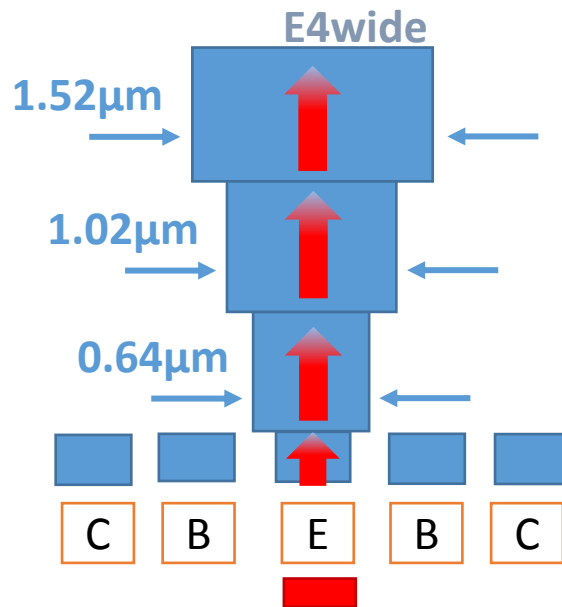
The metal dummies do not change the electrical connections: emitter is grounded at metal-1 level

wide test set:

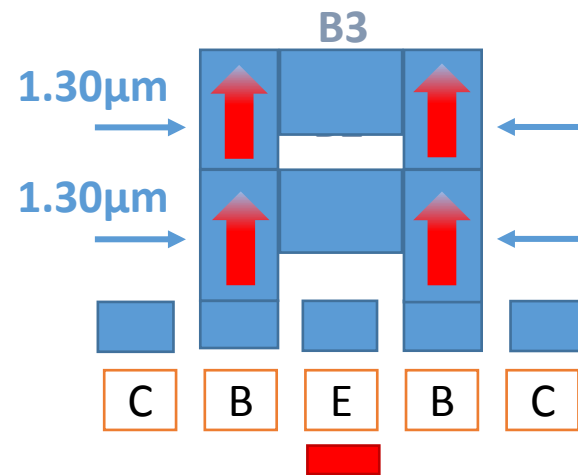
More volume of metal added



B1E1: reference test structure



Metal added upon the base contacts



Test structures for evaluation of the BEOL impact

$$A_E = (0,34 \times 5) \mu\text{m}^2$$

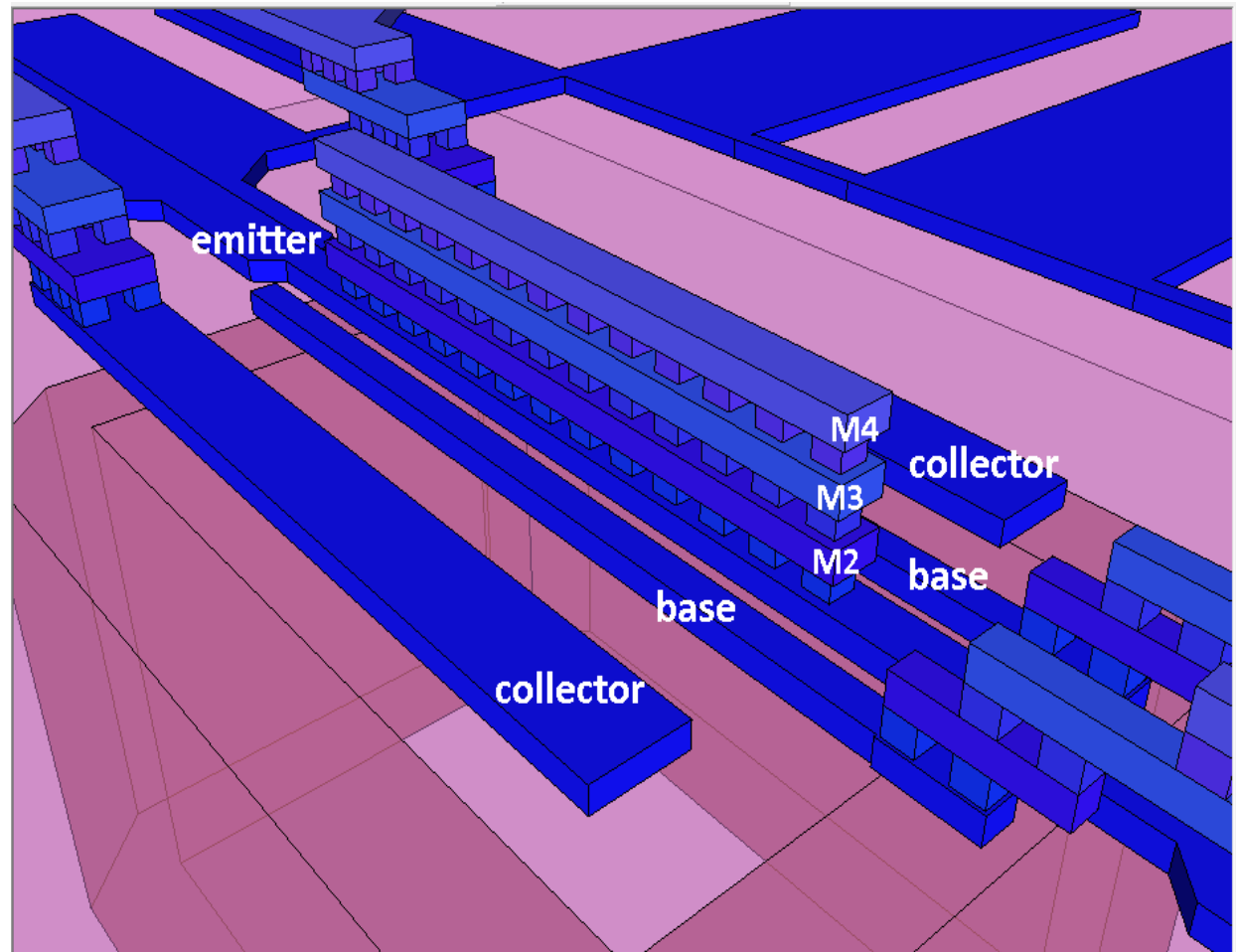
- E2narr
- E3narr
- E4narr



- E2wide
- E3wide
- E4wide

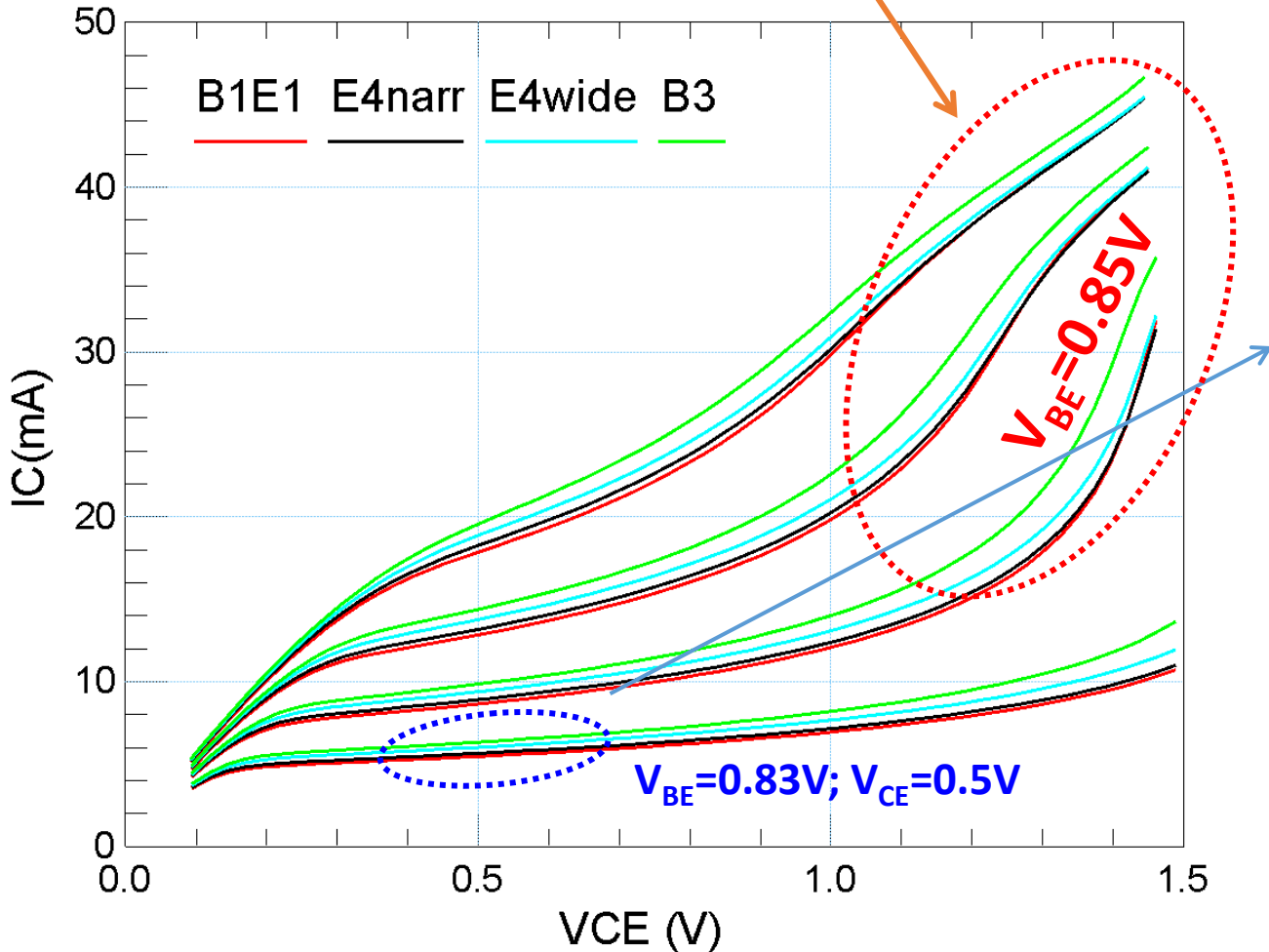


- B2
- B3



Output curves

Test structure	R_{th} [K/W]	ΔR_{th} %
B1E1	3300	0.0%
E4narr	3240	1.9%
E4wide	3160	4.4%
B3	3210	2.8%

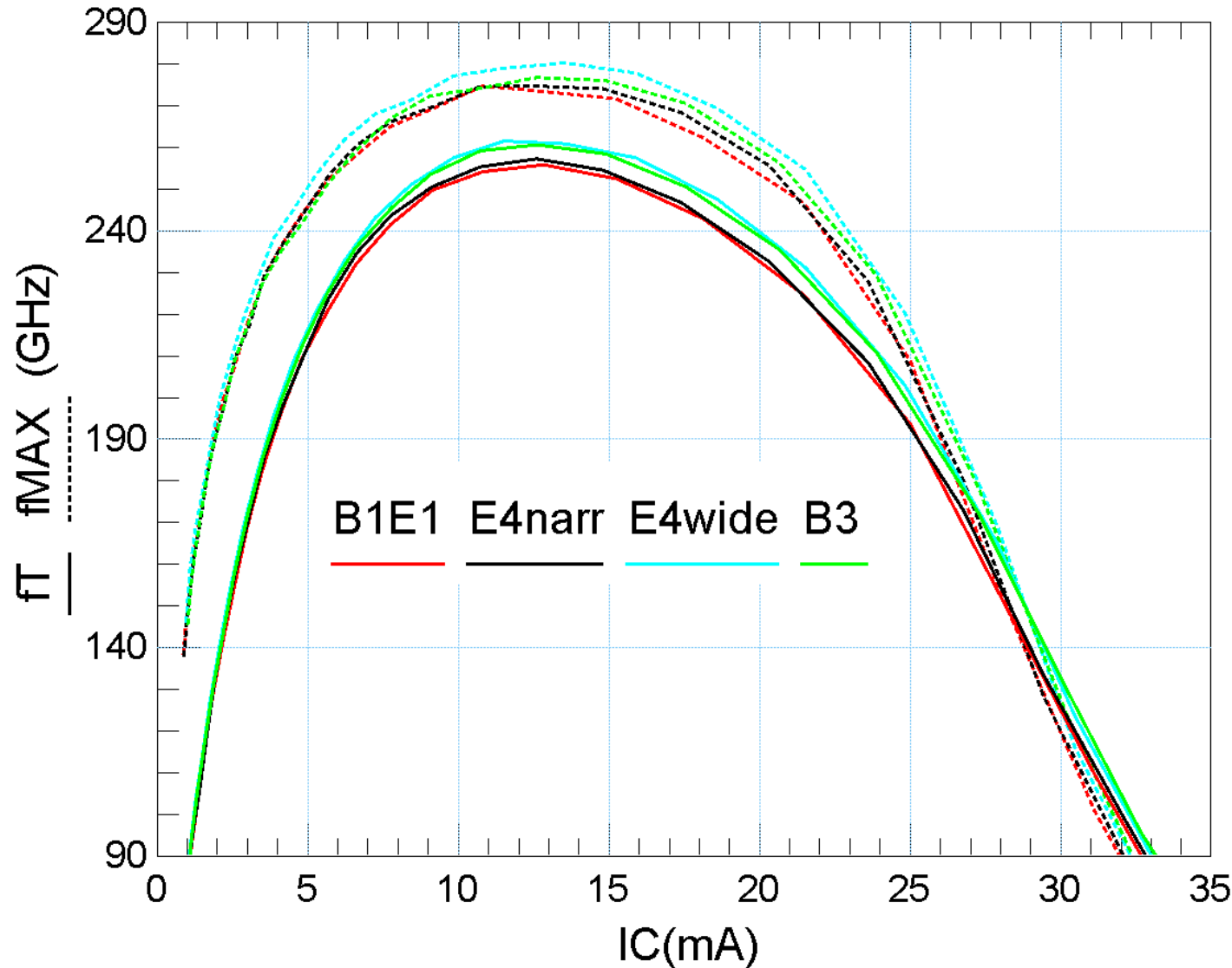


Test structure	ΔI_C %
B1E1	0.0%
E2narr	1.8%
E3narr	2.5%
E4narr	3.4%
E2wide	5.5%
E3wide	9.0%
E4wide	10.0%
B2	10.2%
B3	15.8%

ΔI_C % increases if the volume of metal increases; if metal is added to base contacts effect is stronger

Measured f_T and f_{MAX} figures of merit

de-embedding using the same OPEN and SHORT structures



$V_{CE}=1.5V$

No deterioration in the small signal RF figures of merit is measured

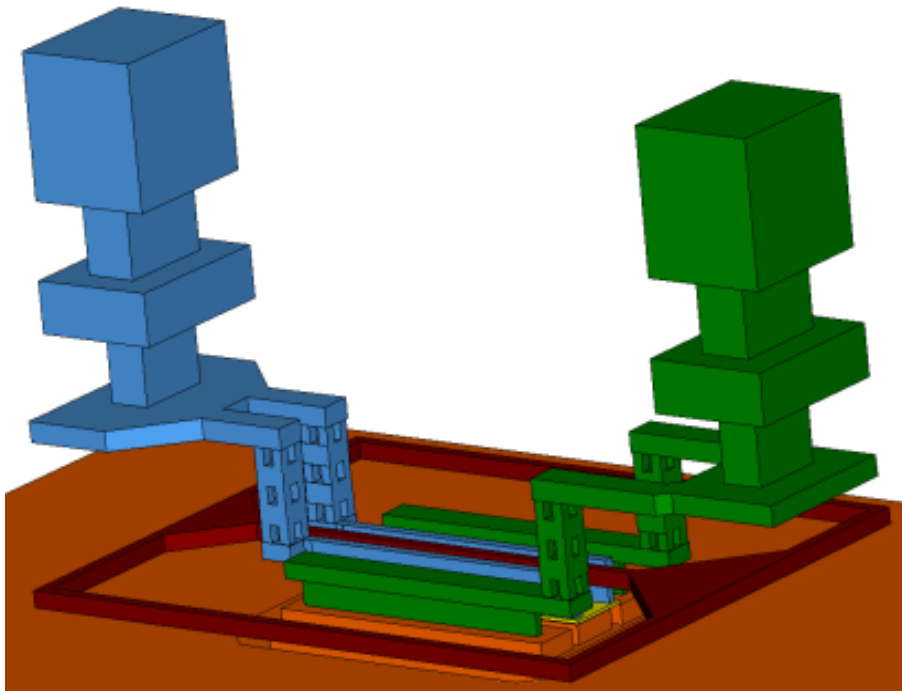
A sensible increment of f_T and f_{MAX} can be observed

Outline

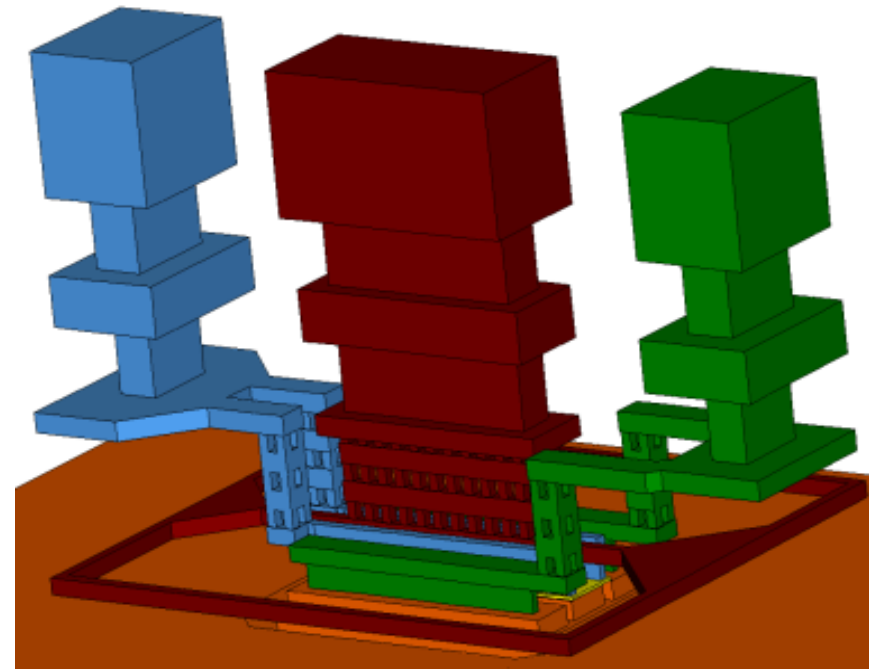
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Test structures for compact modeling of the BEOL impact

$$A_E = (0,22 \times 5) \mu\text{m}^2$$



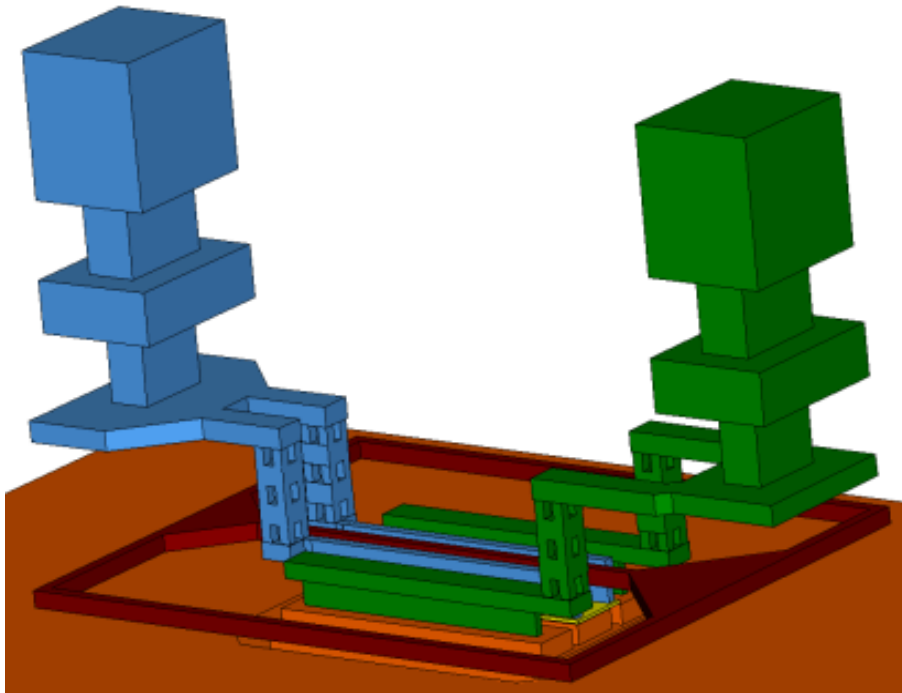
M1 test structure



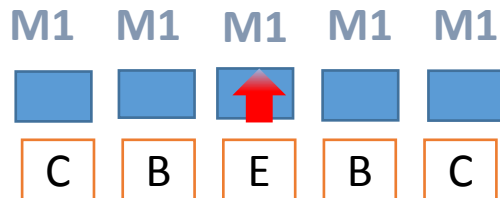
M6 test structure

Electrical connections are unaltered among the two structures

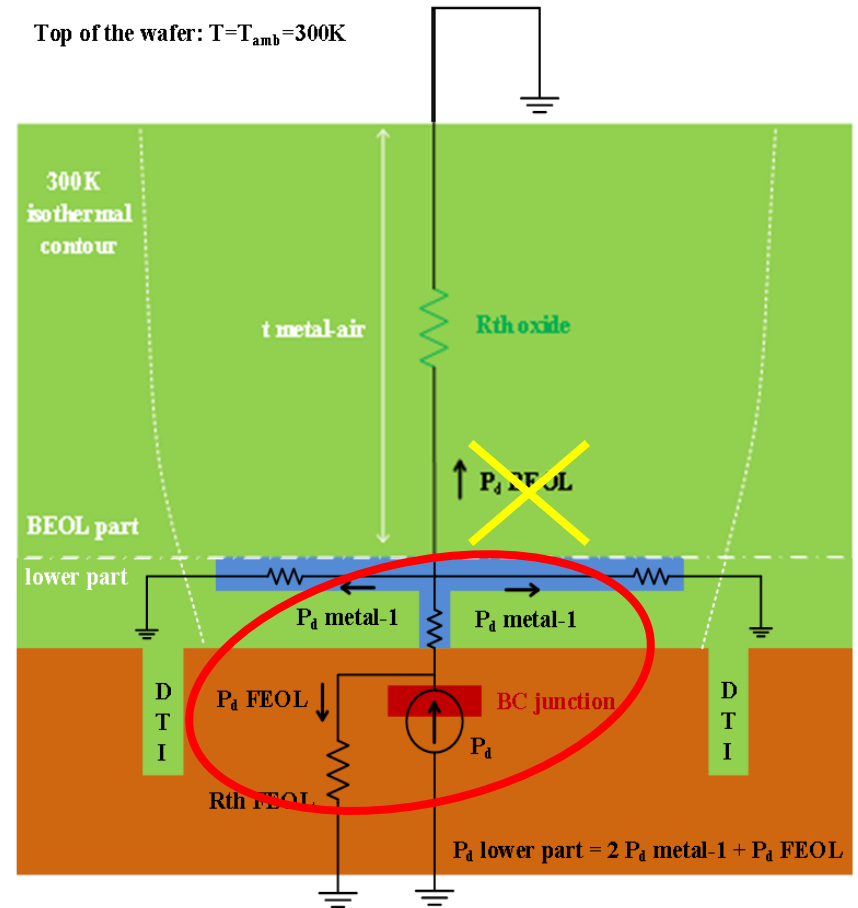
M1 test structure and schematic representation of the Rth



M1 test structure

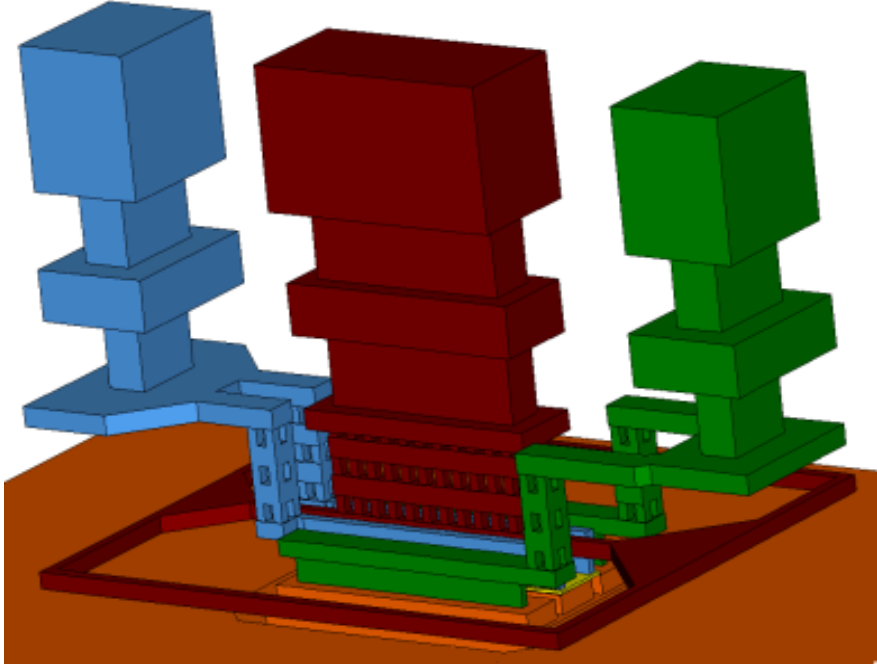


HEAT SOURCE: BC junction



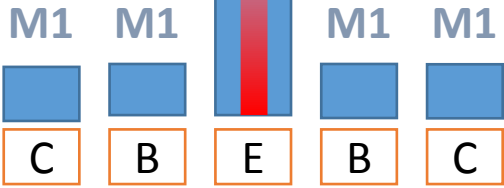
- R_{th} of the BEOL part is just given by oxide (very high value, P_d^{BEOL} is negligible)
- Total P_d can be approximated by just the P_d of the lower part

M6 test structure and schematic representation of the Rth



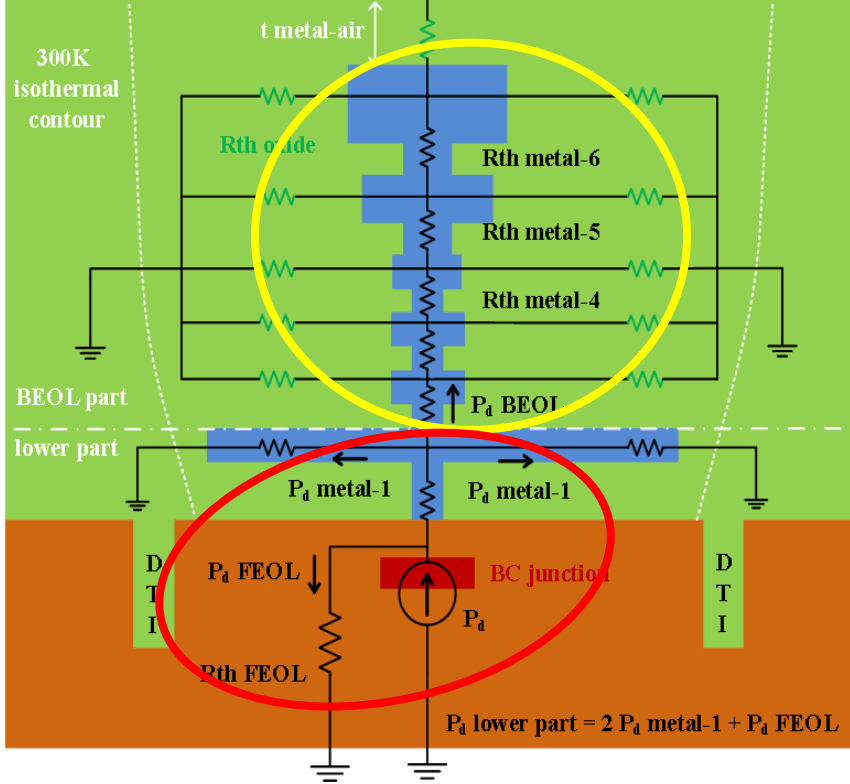
M6

M6 test structure



HEAT SOURCE: BC junction

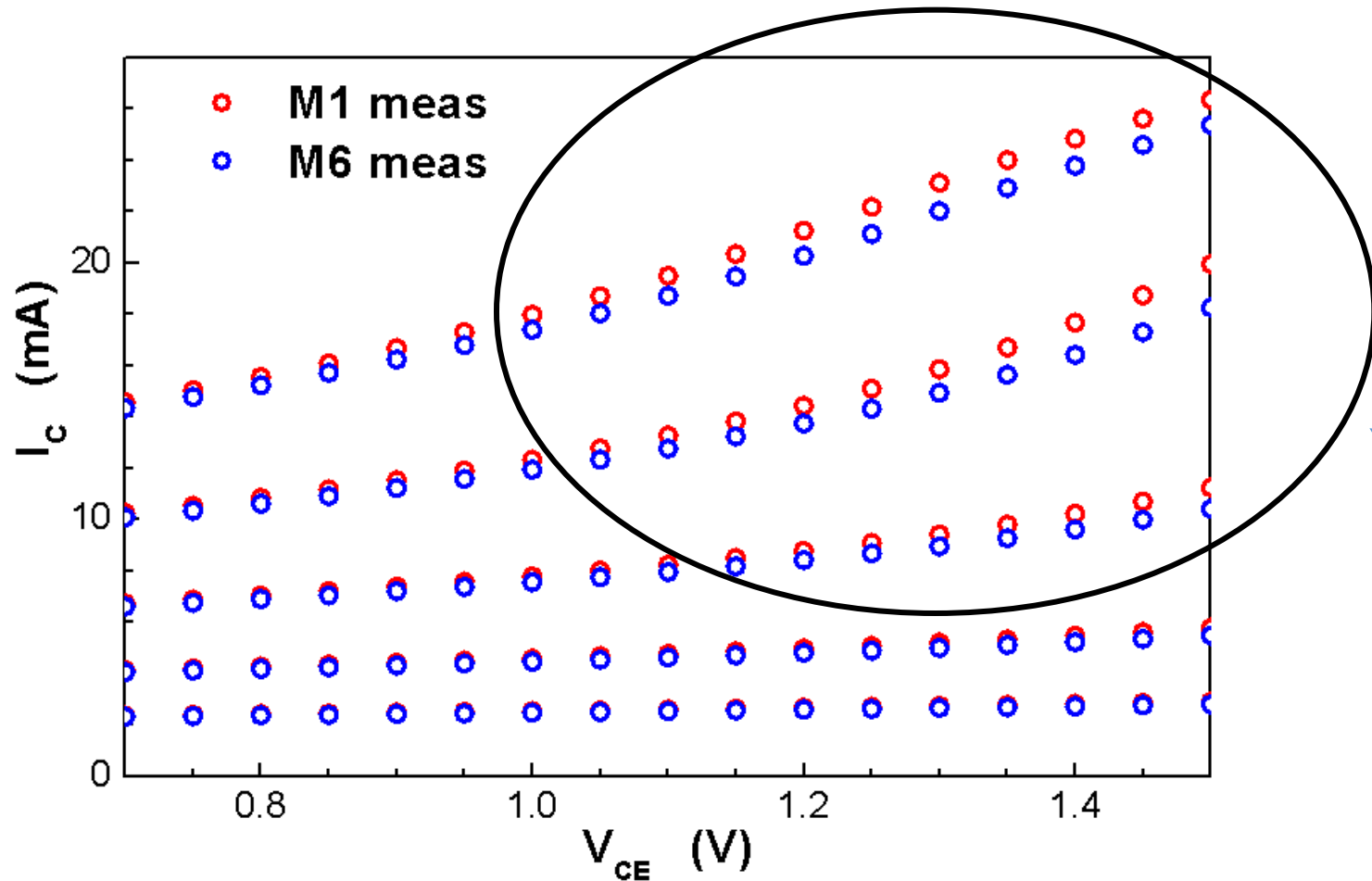
Top of the wafer: $T=T_{amb}=300K$



Back of the wafer: $T=T_{chuck}=300K$

- metallization reduces the overall Rth of the BEOL part and **helps vehicle P_d BEOL upwards**
- Total P_d is now split in 2 branches: one flows in the lower part and the other in the BEOL part

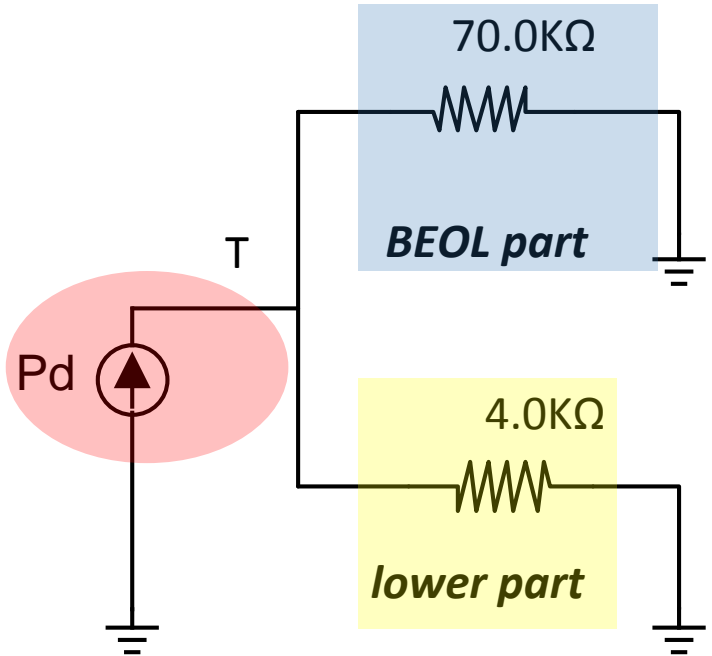
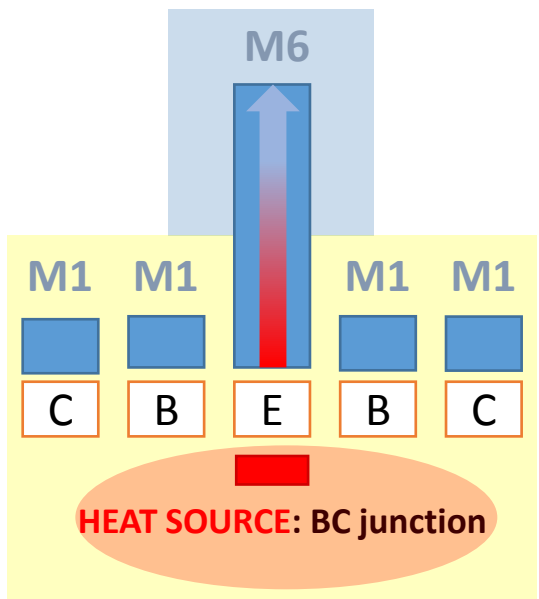
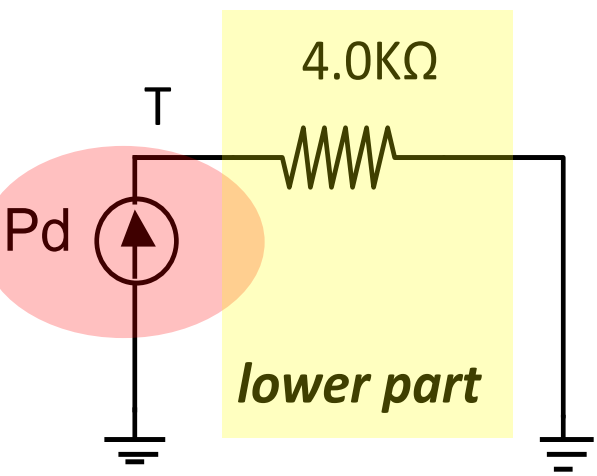
DC measurements on M1 and M6 (output curves)



DC current lowers for **M6** in the high power dissipation region ($V_{be} \sim 900\text{mV}$) due to lower R_{th} ($\sim 10\%$ variation)

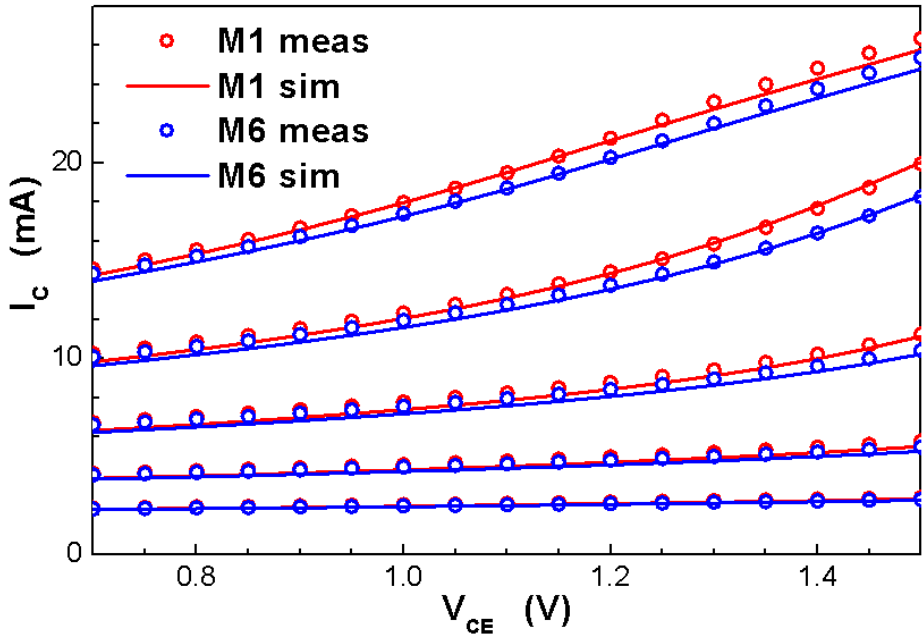
=> **better thermal stability**

DC measurements and thermal network simulated in HiCuM



M1 test structure

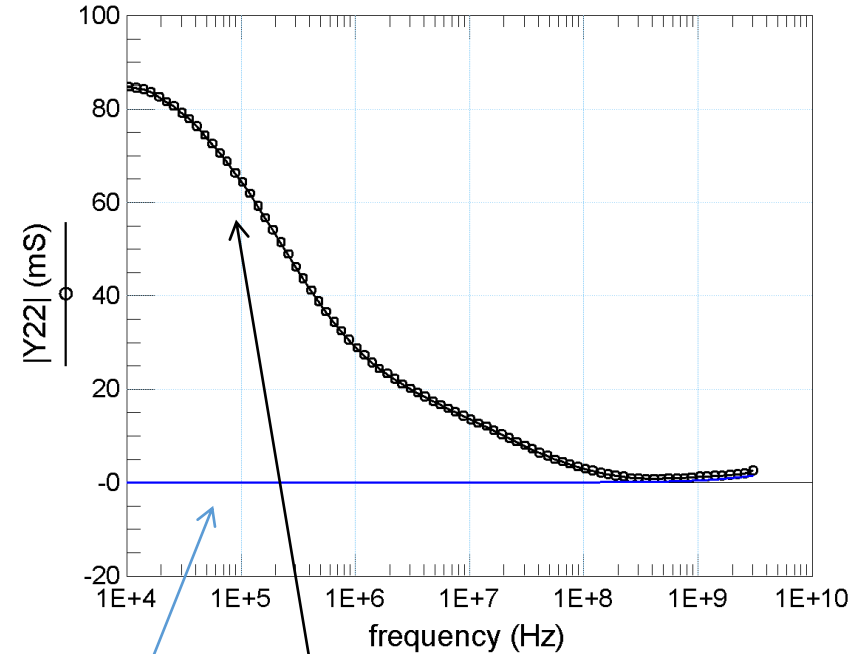
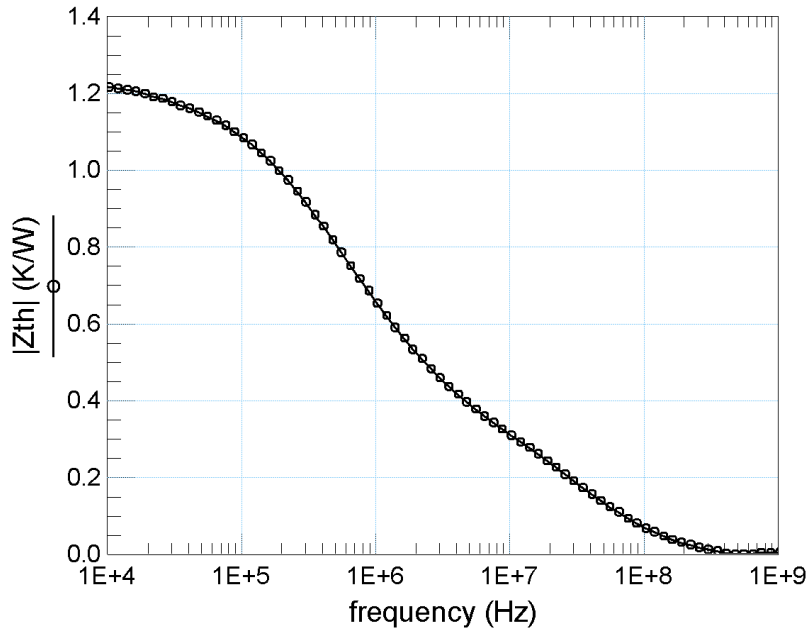
Rth for **M1 test structure** is **verified** with dedicated on-wafer measurements



M6 test structure

- Equivalent Rth drops from 4.0k to 3.78k (-5.5%)

Zth extraction using low frequency S-parameters measurements

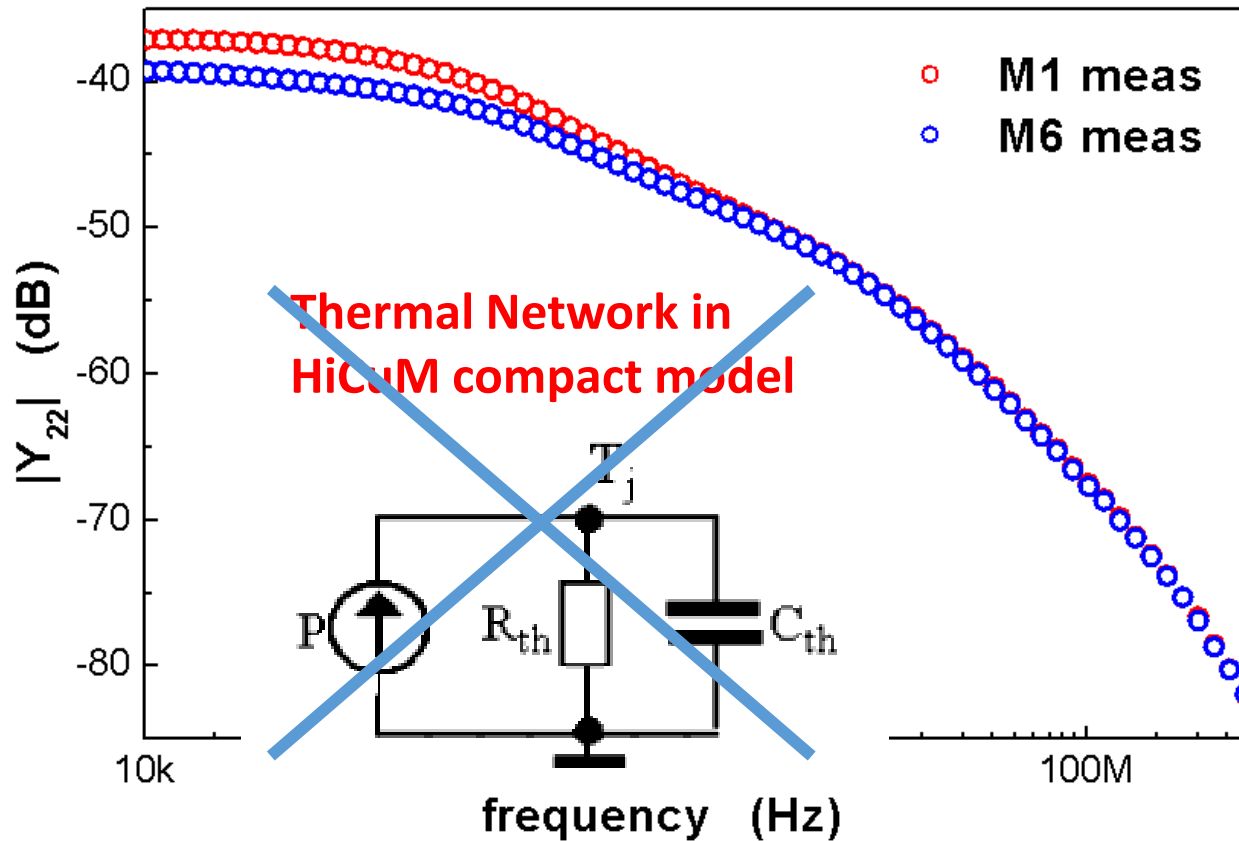


$$Z_{TH} = \frac{Y_{22_meas} - Y_{22_iso}}{\frac{dI_c}{dT_j} \left(I_c + V_{ce} Y_{22_meas} + V_{be} Y_{12_iso} \right)}$$

Y_{22} is sensible to dynamic self heating and used for Zth calculation

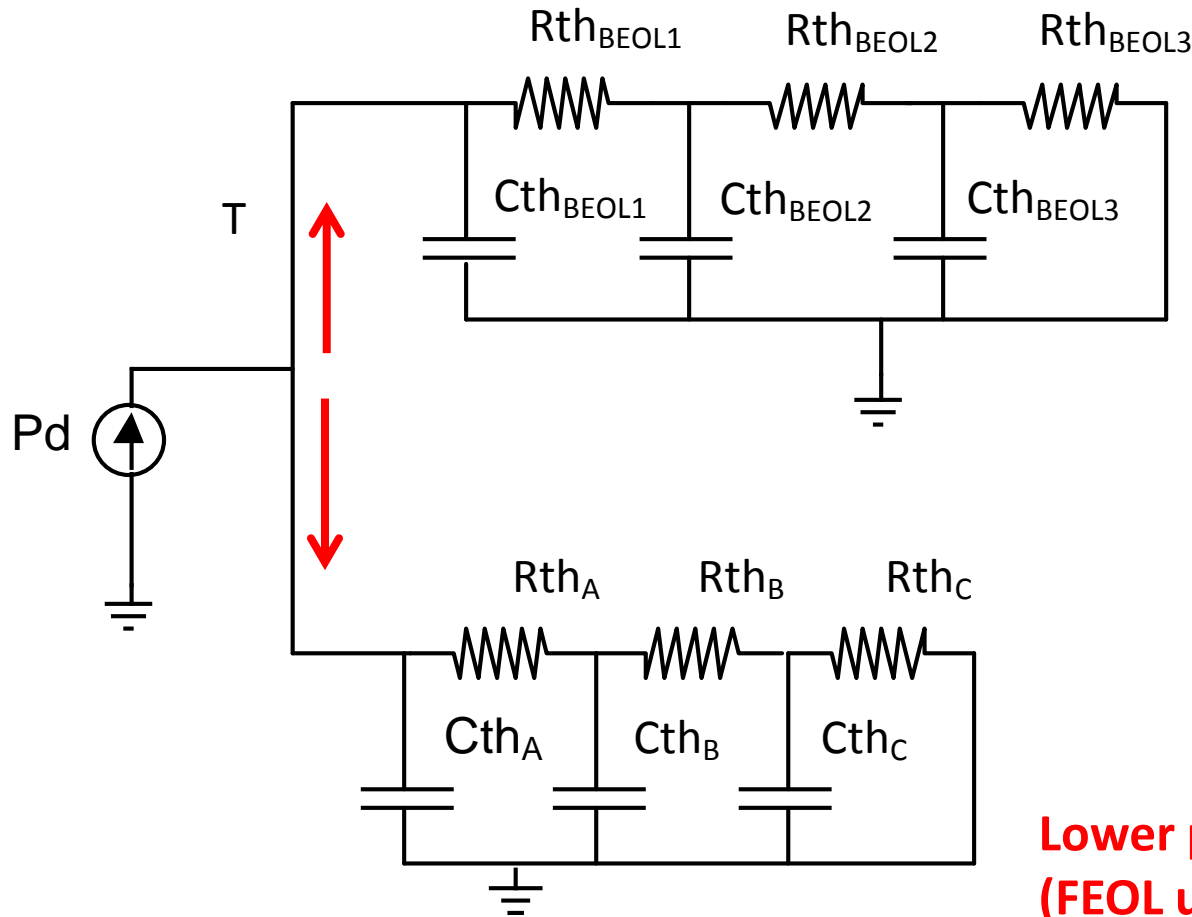
Y_{22} that would be theoretically measured if there were no self-heating effects in the component

Low frequency Y_{22} measurements



- Adding metal dummies in the BEOL changes the Y_{22} in the range DC \rightarrow 2~6MHz
- Thermal diffusion is a distributed phenomenon: an infinite number of RC poles is theoretically needed
- Measured Y_{22} in the range 10kHz \rightarrow 500MHz shows **three main slopes**

Proposed thermal network to take into account distributed Zth



BEOL
thermal network

$$Rth_{jn} = k_r^n R_j$$

$$Cth_{jn} = k_c^n C_j$$

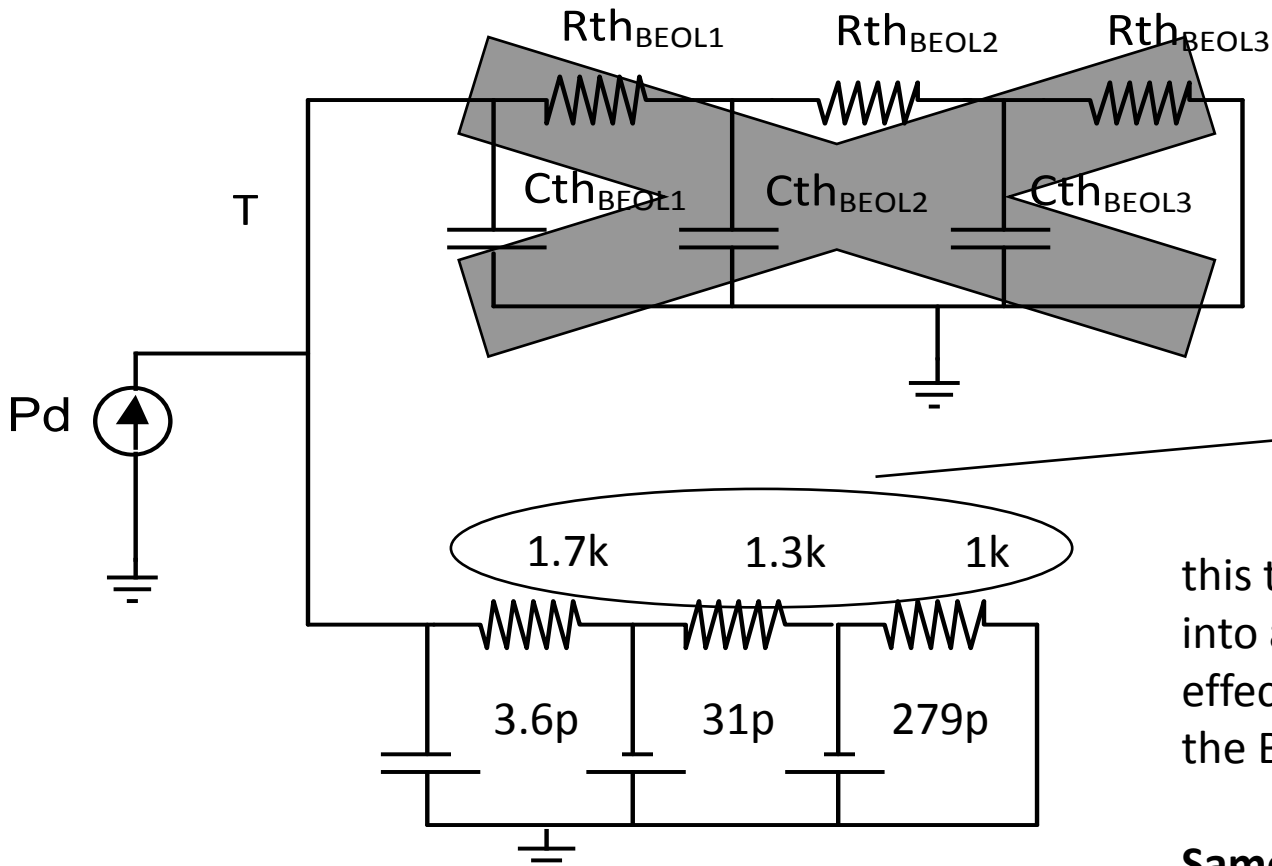
$$k_r < 1$$

$$k_c > 1$$

Lower part thermal network
(FEOL up to metal-1)

D'Esposito, S. Fregonese, A. Chakravorty and T. Zimmer, "Dedicated test-structures for investigation of the thermal impact of the BEOL in advanced SiGe HBTs in time and frequency domain" ICMTS 2016

Thermal model for the M1 test structure

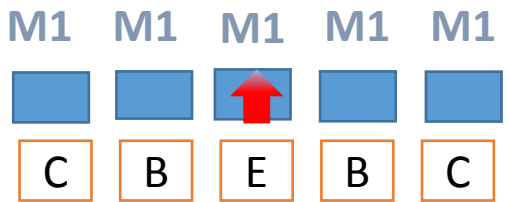


BEOL part is neglected for the M1 test structure

4k

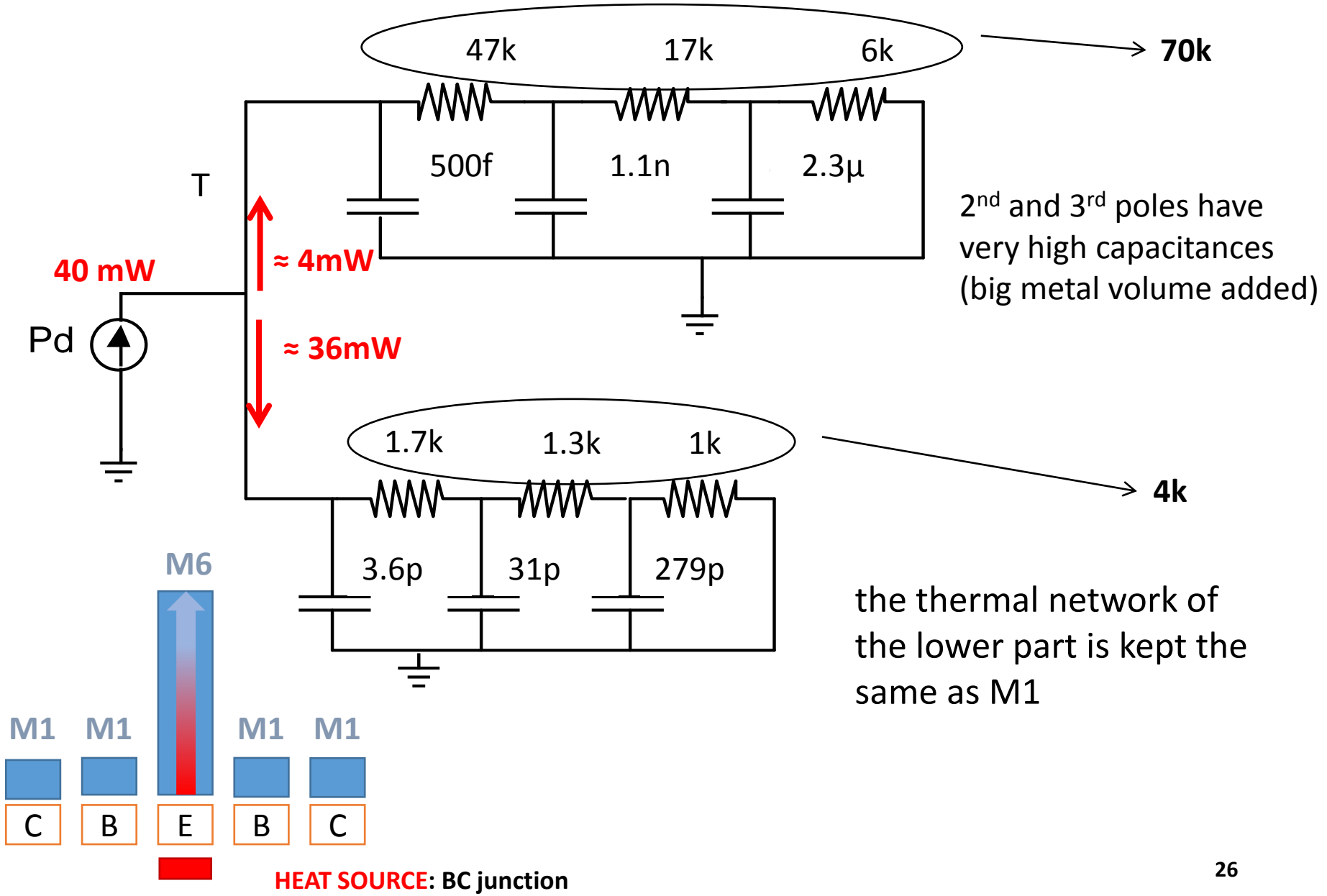
this thermal network takes into account the thermal effect of the FEOL and of the BEOL till metal 1

Same Rth than DC case is used, but cut into 3 parts

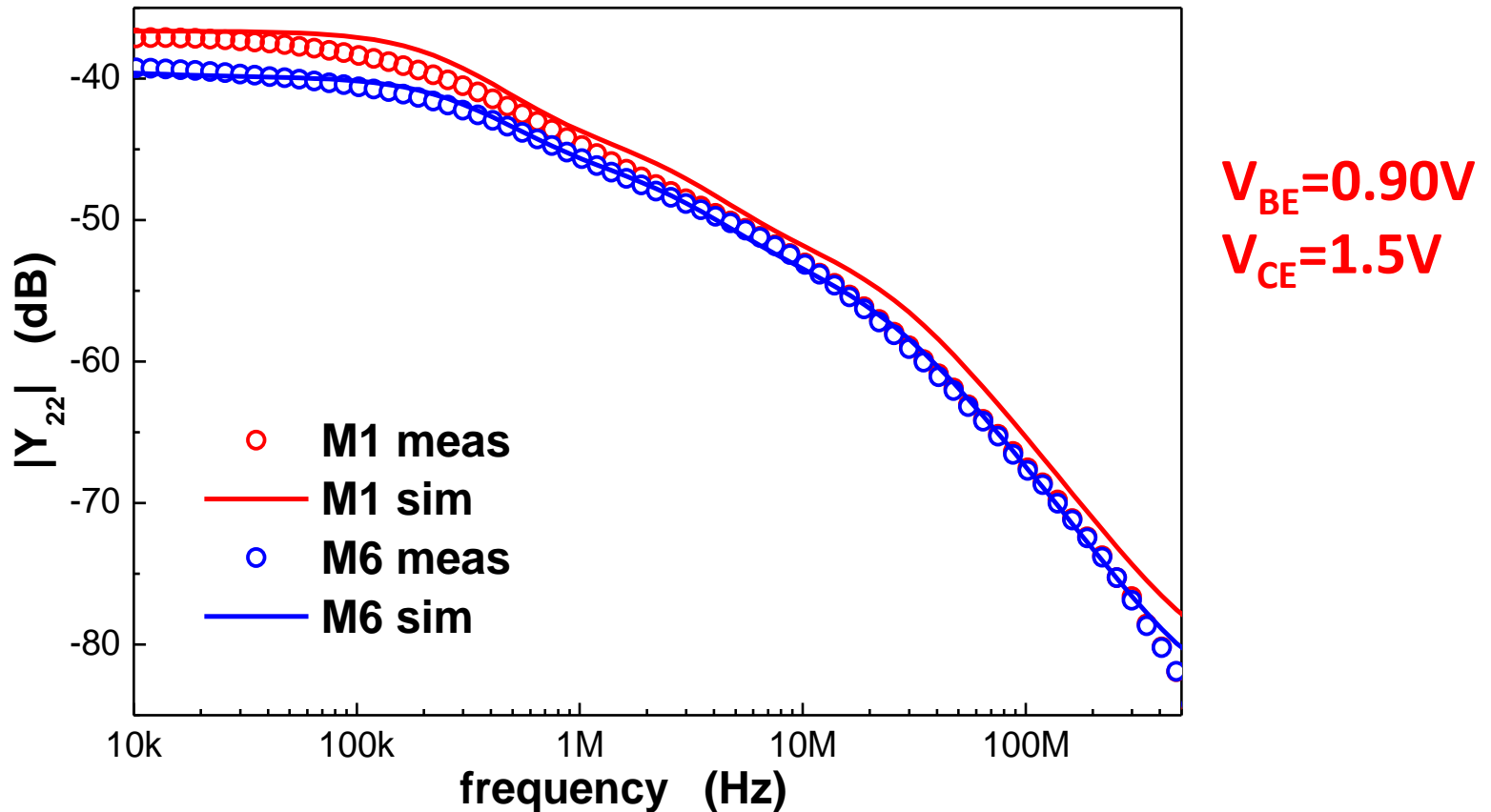


HEAT SOURCE: BC junction

Thermal model for the M6 test structure



Y_{22} parameter simulated in HiCuM



- The Y_{22} versus frequency is fit nicely for the 2 test structures under study using the proposed thermal networks

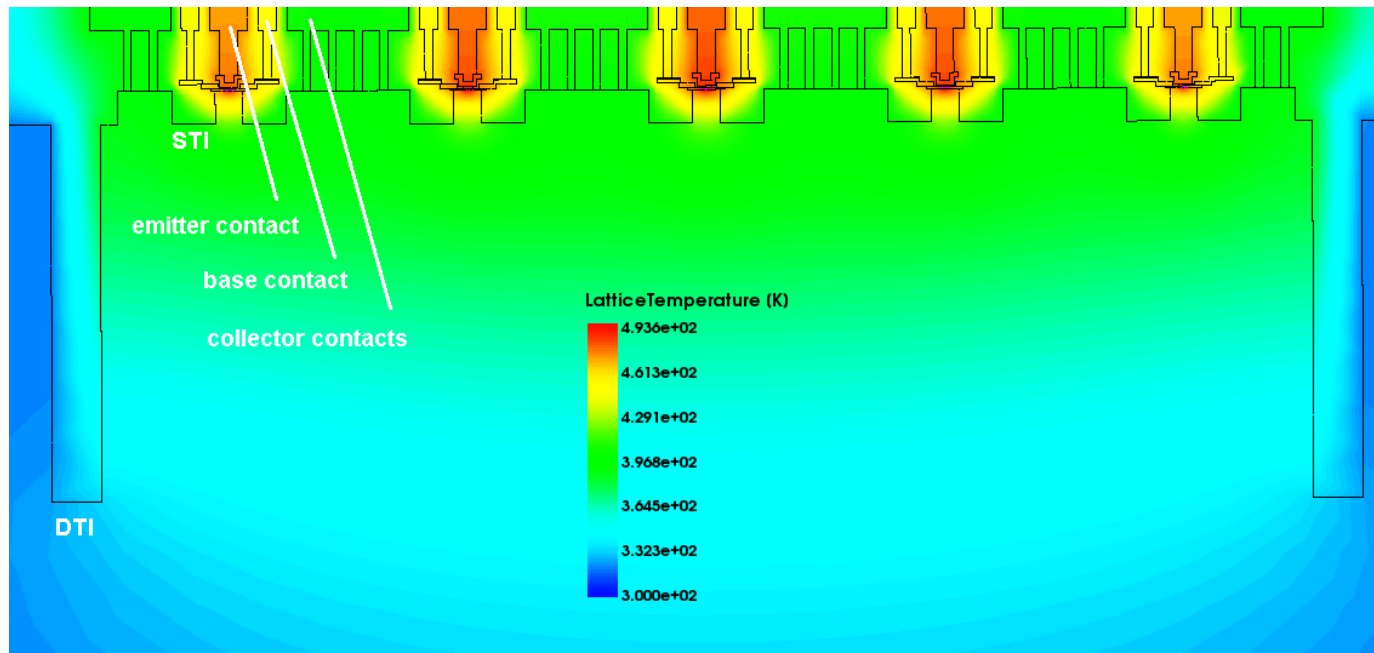
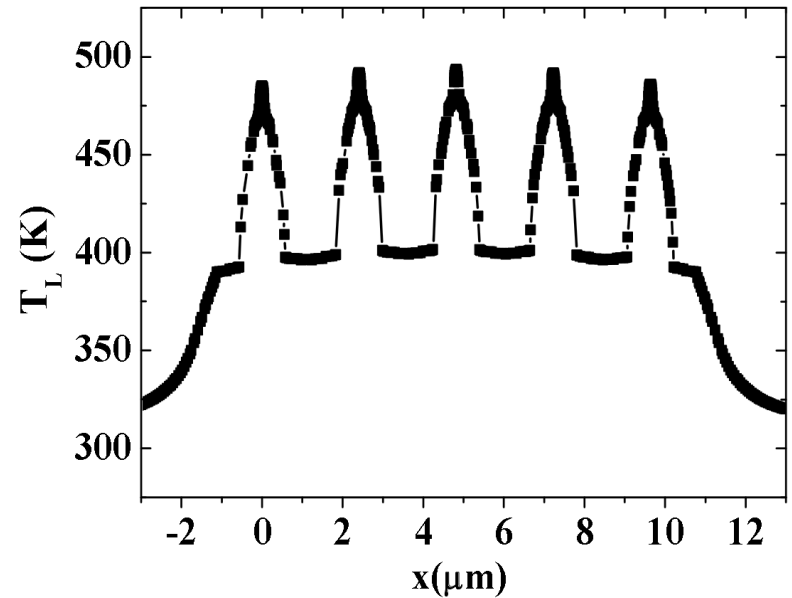
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Thermal unbalances in multifinger devices (ST B55)

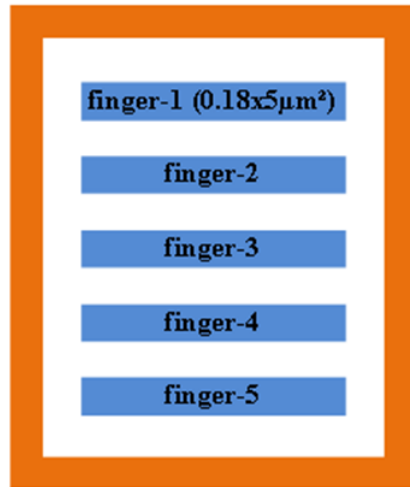
Thermal coupling in multifinger HBTs:

- 1) unbalanced temperature distribution
- 2) hotspot formation
- 3) current hogging
- 4) device instability
- 5) device failure

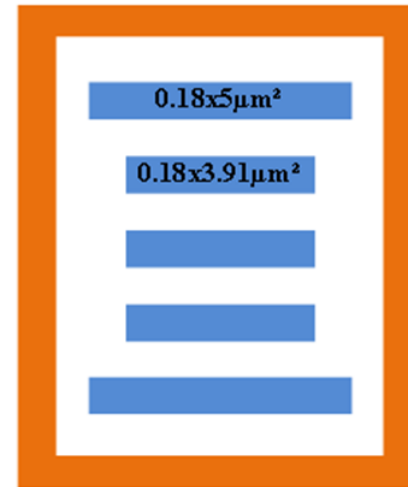


Proposed alternative finger layouts: HL structures

Reference structure:
VM3
(active part is unaltered)



(a) VM test structures
DTI enclosed area = $71,78\mu\text{m}^2$
 $A_E = 4,5\mu\text{m}^2$

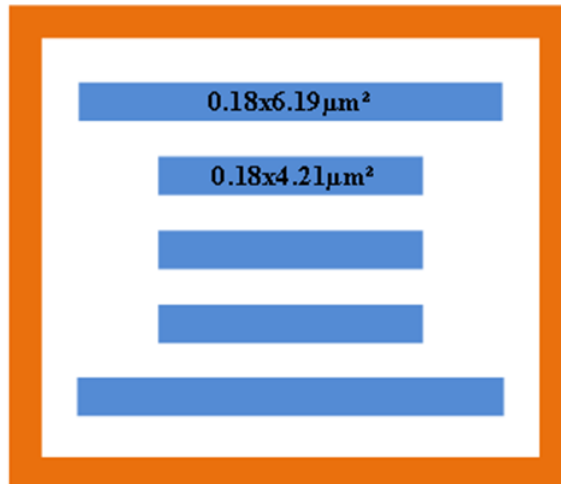


(c) HL2 test structure
DTI enclosed area = $71,78\mu\text{m}^2$
 $A_E = 3,91\mu\text{m}^2$

Non-uniform finger length
HL2

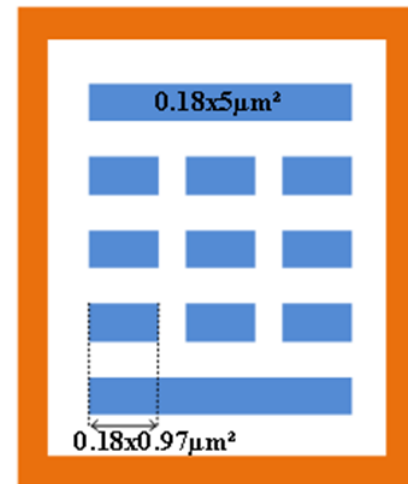
Lower power dissipated on the central fingers

Increased cross section surface for power dissipation



(b) HL1 test structure
DTI enclosed area = $86,83\mu\text{m}^2$
 $A_E = 4,5\mu\text{m}^2$

Enlarged DTI
HL1



(d) HL3 test structure
DTI enclosed area = $71,78\mu\text{m}^2$
 $A_E = 3,91\mu\text{m}^2$

Emitter segmentation
HL3

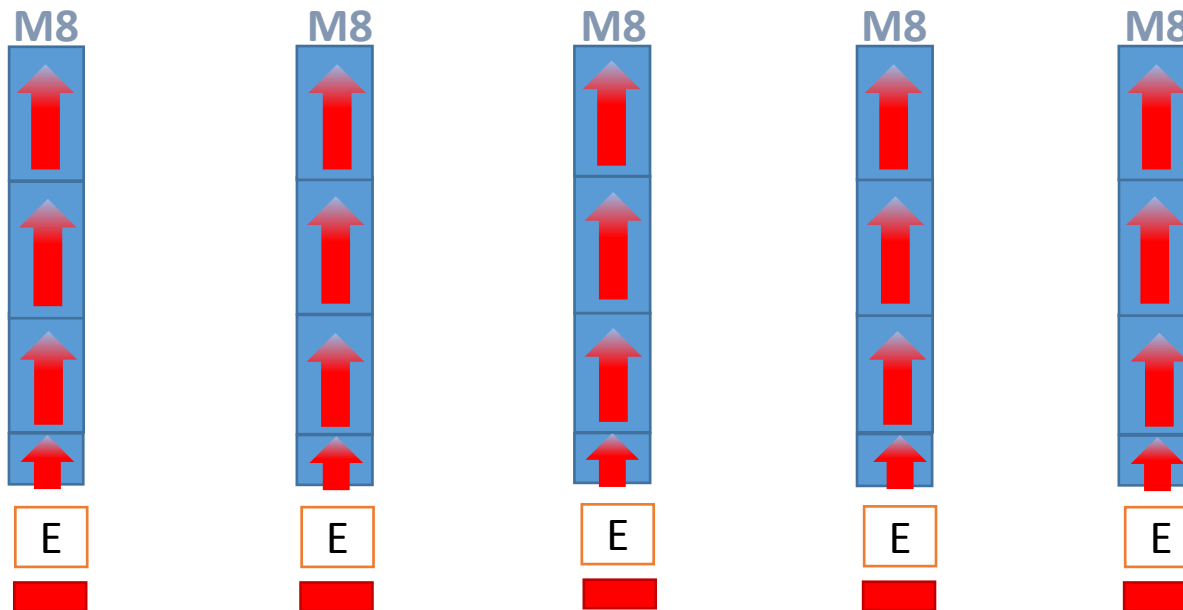
VM structures to evaluate the BEOL impact in multifingers

VM8 dummies till metal-8

VM6 dummies till metal-6

VM3 reference test structure

VM1 just metal-1 is present



The active part of the transistor is not modified, just heat spreaders are added

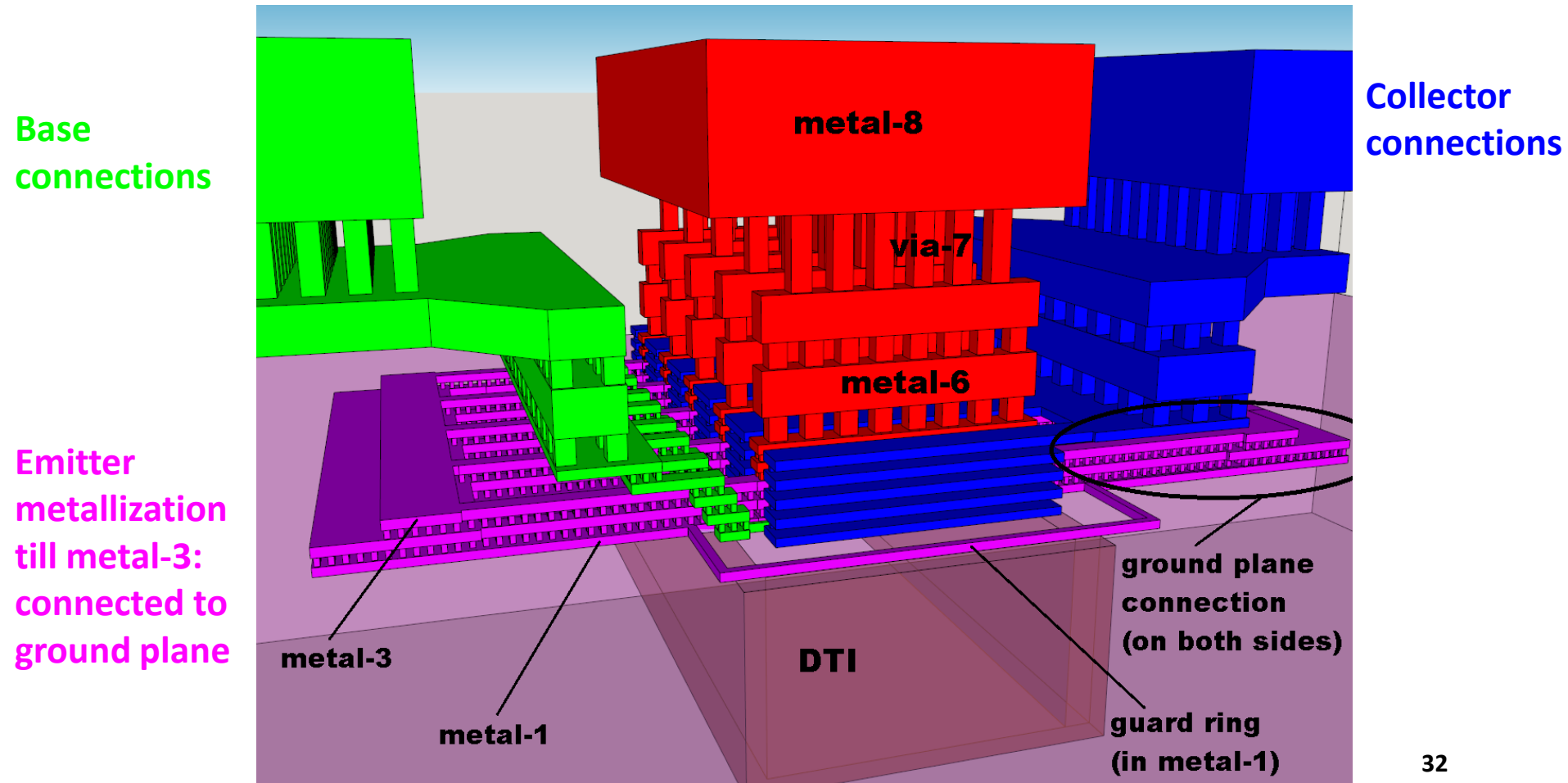
Electrical connections are unaltered among the different transistor structures

3D representation of the BEOL test structures

5xCBEBEBC architecture

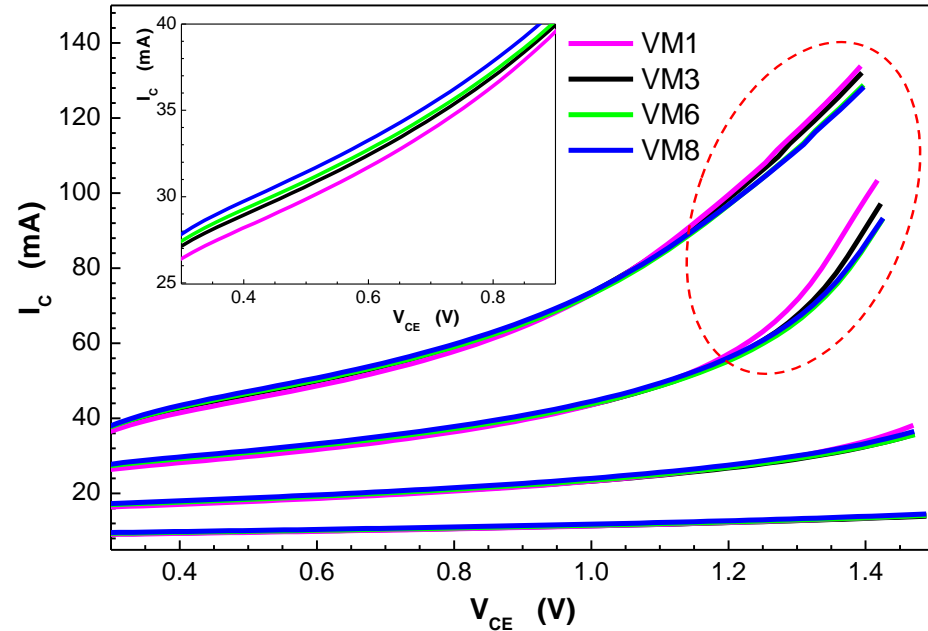
VM8 test structure

Metal dummies connected upon emitter contacts (VM8)

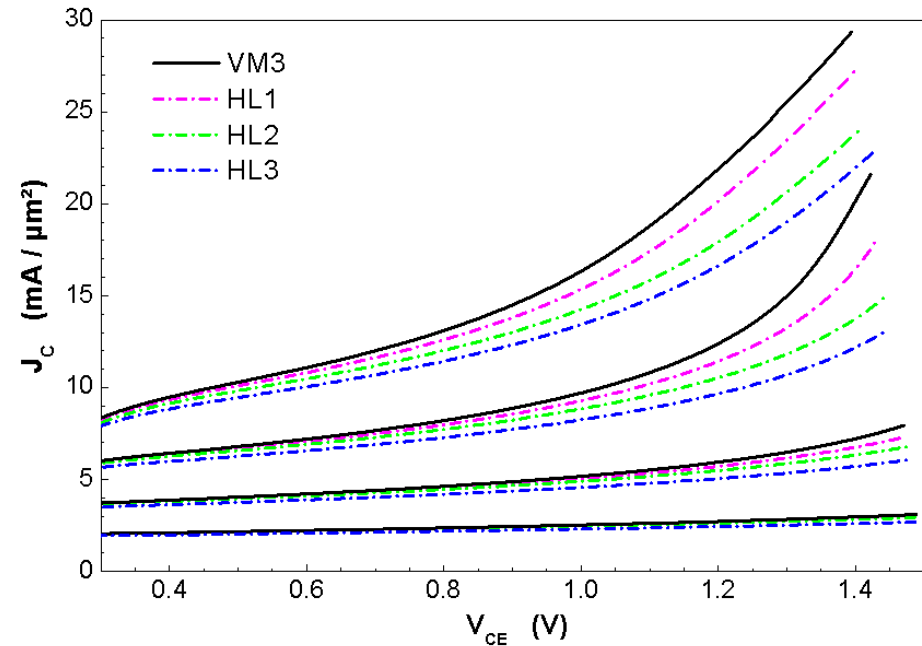


Output curves

VM test structures



HL test structures



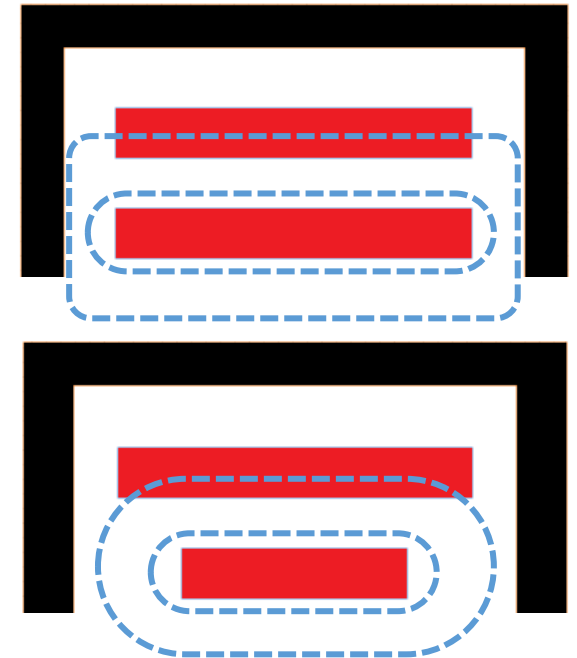
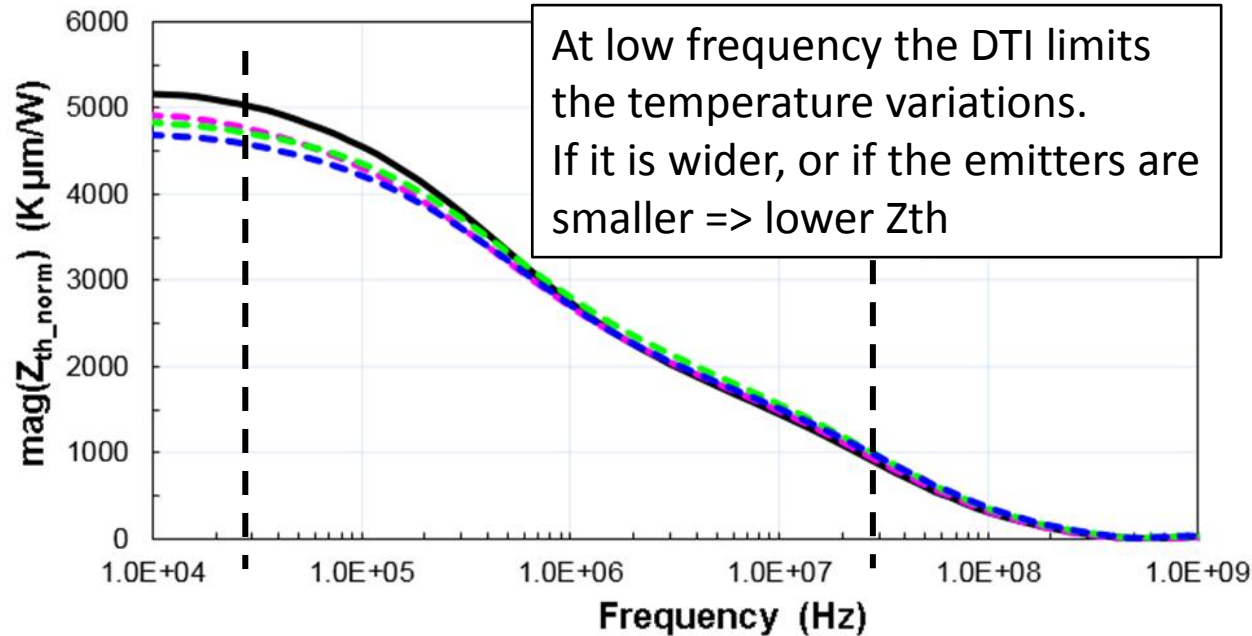
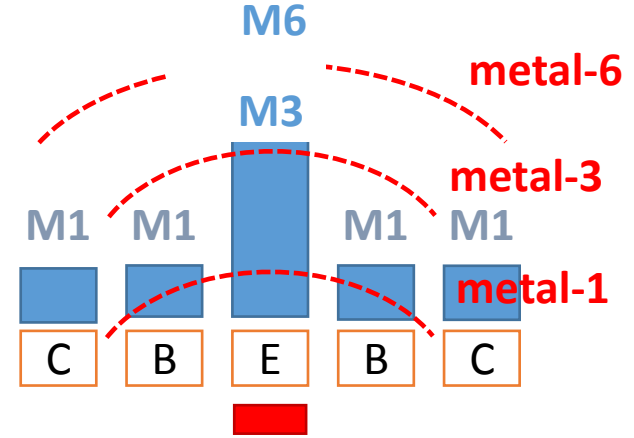
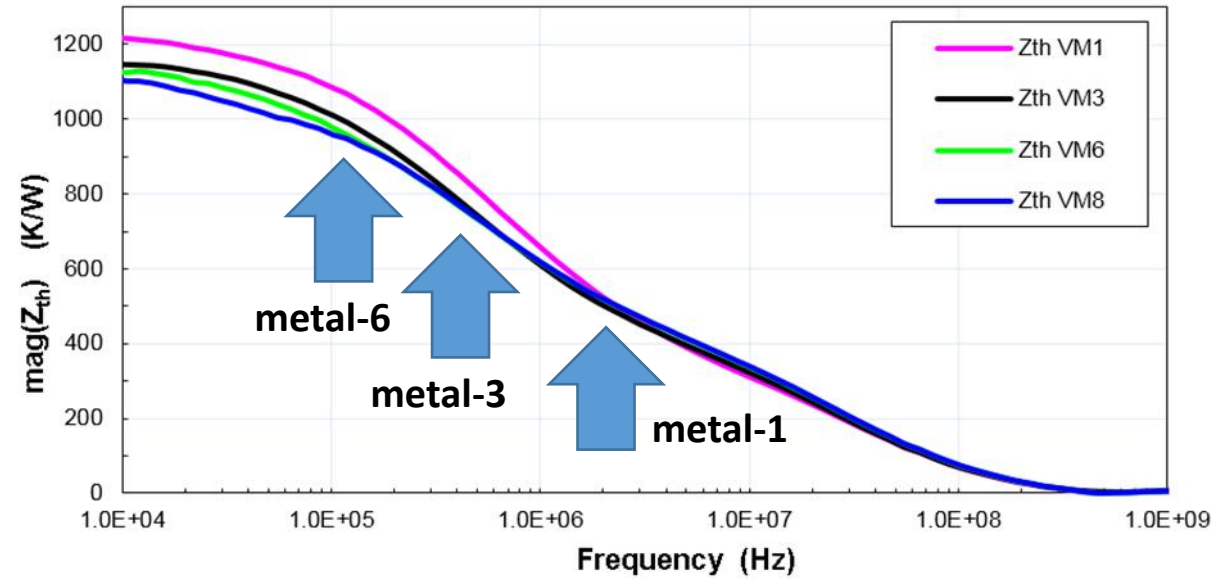
Adding metal heatspreaders above the emitters lowers the slope of I_C in the high P_{diss} region

The increase of the DTI enclosed area allows an even lower slope

The slope of J_C is even lower for the devices with reduced A_E

Emitter segmentation yields the best electro-thermal performances

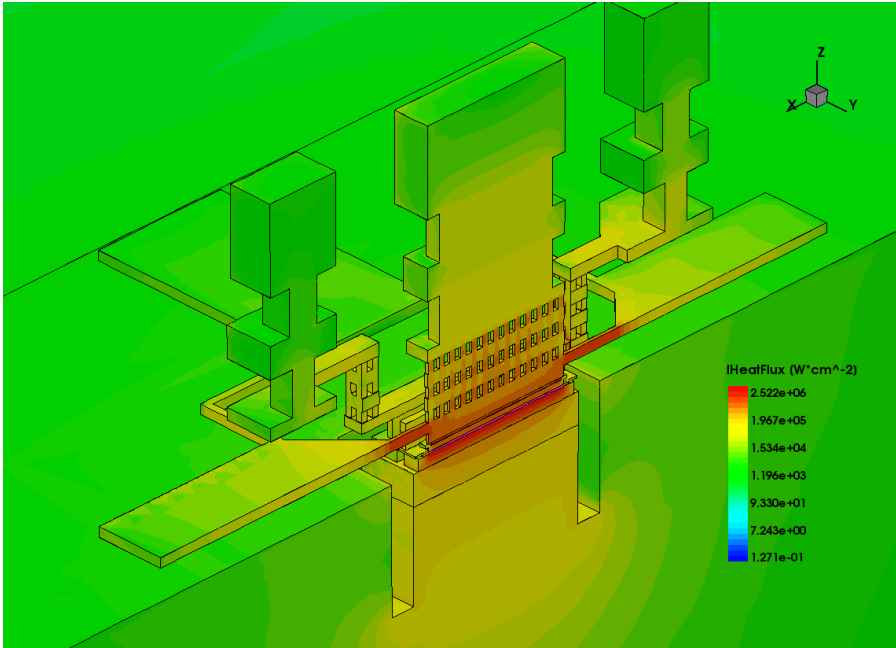
Thermal impedance



Outline

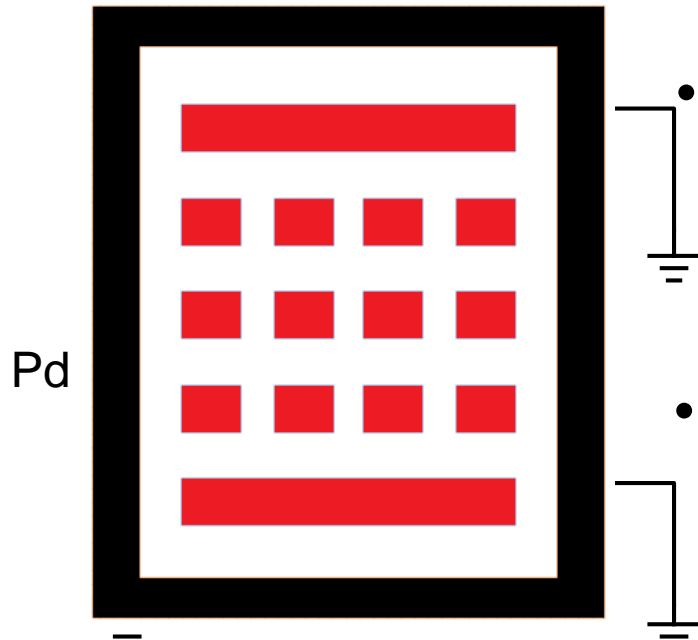
- SiGe HBTs for THz applications
 - Thermal issues in state of the art SiGe HBTs
- Technologies under study: IFX B11HFC and ST B55
- Characterization of BEOL impact in single finger HBTs (IFX B11HFC)
- Physical modeling of the BEOL impact (IFX B11HFC)
- Impact of BEOL and transistor layout in multifinger HBTs (ST B55)
- **Conclusions & future perspectives**

Conclusions: BEOL impact



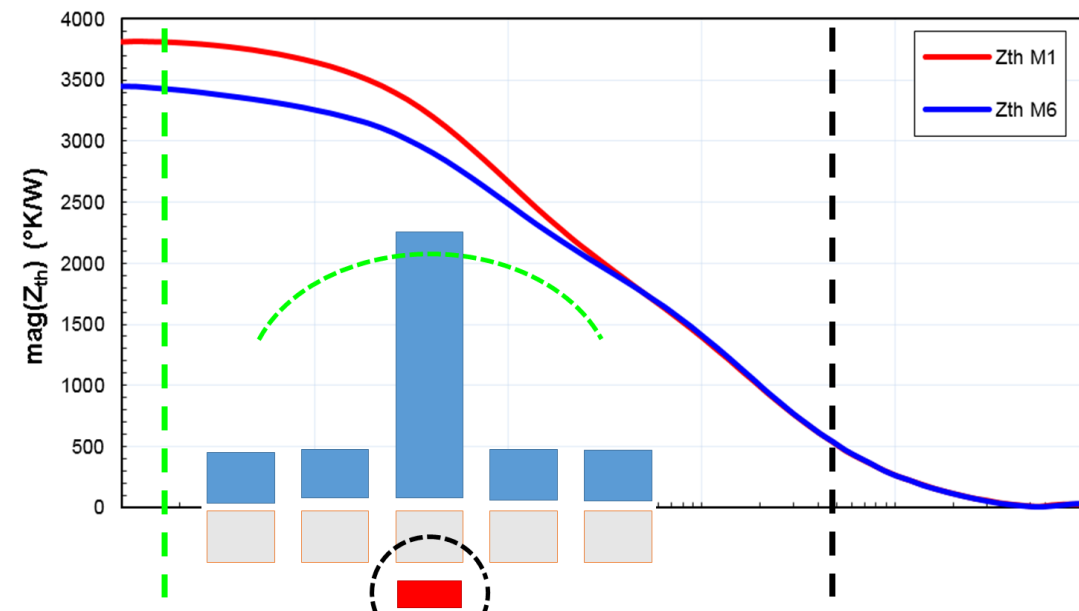
- Mechanical stress
- Decrease of R_{th}
- Stabilizing effect for I_C
- Better RF performances
- The metallization helps to evacuate the heat generated by the transistor
- The metal volume slows down the thermal response and keeps the temperature more stable
- These effect can be modeled on a physical base and simulated

Conclusions: layout modifications



- Modifications in the transistor layout have a stronger electro-thermal impact (DTI enlargement, emitter segmentation)

- In AC the temperature sinusoidal variations penetrate the transistor till different depths according to the frequency



- Changes in the transistor layout mostly induce Z_{th} variations at very low frequencies

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Thank you for
your attention!