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Using CAD Tool for Substrate Parasitic Modeling in Smart Power Technology

Hao Zou, Yasser Moursy, Ramy Iskander, Alexander Steinmair, Heimo Gensinger, Ehrenfried Seebacher, Jean-Paul Chaput and Marie-Minerve Lou rat

Abstract—Smart Power integrated circuits receive an increasing attraction recently, especially in automotive industry. Substrate noise coupling is one of the major causes of failure in this kind of integrated circuits that requires circuit redesign and increases the overall cost. An exhaustive failure analysis is needed to identify failures due to substrate coupling. In this paper, we present a post-layout extraction and simulation methodology for substrate parasitic modeling. Based on this methodology, we have developed a dedicated Computer-Aided-Design tool that is used for substrate extraction from layout patterns. The extraction employs a meshing algorithm for substrate parasitic generation. To validate the substrate model, the process of benchmarking uses industrial design structures in $0.35\mu\text{m}$ high-voltage-CMOS technology. Two test cases in transient simulation are considered in this work. The first one is a common used current mirror circuit. Our tool predicts the interference of substrate currents to this basic circuit. The second test case is an industrial design test-chip where parasitic coupling is investigated in a standard automotive test. Eventually, by using the proposed CAD tool, it becomes possible to simulate the behaviors of substrate noise at early phase before fabrication.

Index Terms—Smart Power ICs, parasitic noise, substrate modeling, CAD, meshing strategy.

I. INTRODUCTION

Modern trend of microelectronics is to integrate more functionalities on a single chip, along with reducing the cost and the total number of external components. This integration increases the reliability and reduces the electromagnetic interference (EMI) of the overall system. The same idea is used in Smart Power integrated circuit (ICs) where high voltage (HV) power devices and low voltage (LV) analog and digital devices co-exist on the same silicon substrate [1].

In a typical Smart Power IC, the power stage is commonly used to drive inductive loads, e.g. motor. During the power stage switching, the drain voltage of output transistor instantly goes below ground or above supply voltage that injects substrate currents. The induced substrate currents lead to a local shift of substrate potential that can reach hundreds of millivolts. As a consequence, it realizes the coupling between surrounding devices with possible activation of parasitic lateral NPN (N-well to P-substrate to N-well) bipolar junction transistors (BJT). The induced substrate current paths are considerably long and layout dependent.

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Unlike the traditional IC in LV technology, the Smart Power ICs have to withstand harsh environmental conditions like high operating temperatures. Due to high chip temperature arising from power domains, the substrate noise increases and the impact of substrate coupling becomes even worse. As technology improves, HV devices continue to get larger to deliver more power, in the meantime LV digital devices are shrinking to provide higher frequency and less power consumption. Therefore, it can be quite challenging to ensure immunity against parasitic coupling. The coupled noise from power stage is disturbing the normal functionalities and compromising the system performances. Moreover, the possible activation of parasitic BJTs may cause destructive effects such as triggering the latch-up.

Failures due to coupling of substrate lateral NPN BJTs cause several circuit redesigns. Addressing such failures is becoming of interest since these failures are still reported in tests after fabrication. On the one hand, conventional IC design ignores the minority carriers related effects, however, such effects due to carriers (majority and minority) injection and propagation in substrate are significant in Smart Power ICs. On the other hand, the impact of minority carriers cannot be modeled in conventional way, since standard compact model cannot maintain the minority carriers propagation between devices.

Technology Computer-Aided-Design (TCAD) [2] tools are considered the only way to investigate the minority carriers related effects. This physical device simulator solves the 2D or 3D equations based on the finite elements method (FEM). They have reliable results, yet considerably time demanding. Investigations to substrate parasitic lateral NPN BJTs using TCAD simulators were performed in [3][4]. They show reliable results with agreement to measurements. However, the method is not applicable since it is time demanding (several hours), and using custom layout reduction.

In 2010, a methodology for substrate parasitic modeling was introduced [5]. The idea relies on modeling the substrate with a network of enhanced parasitic models. Different from standard parasitic models, these models take into account the effects related to minority carriers. Besides the models, the geometry of layout is the key to model correctly the behaviors of substrate noise. Based on this idea, we extend the method by developing an automatic layout extraction tool. In this paper, the main idea will be introduced accompanied by several industrial test cases.

This paper is organized as follows: In section II, we recall the methodology of substrate parasitic modeling for Smart

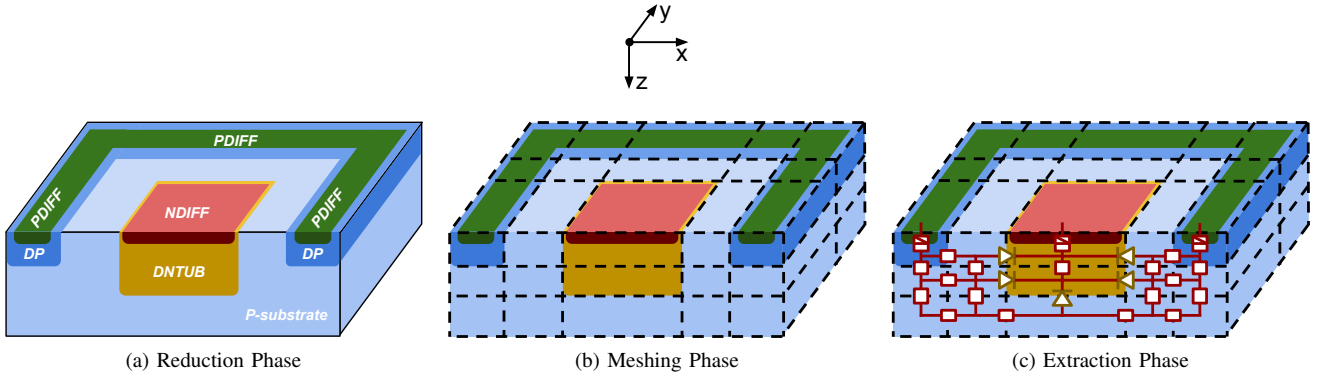


Fig. 1. Modeling approach for substrate parasitic extraction in case of simple diode.

Power technology. Section III introduces our design flow with dedicated layout-extraction methodology. To validate our substrate model, process of model benchmarking in terms of parasitic diode and bipolar are discussed in section IV. In section V, we apply our method to two cases study. Finally, the conclusions are drawn in section VI.

II. MODELING METHODOLOGY

In the context of European Project AUTOMICS [6] with 7th framework entitled “Pragmatic Solution for Parasitic-Immune Design of Electronics ICs for automotive”, we aim at proposing a new pragmatic, focused and well-structured solution for modeling of parasitic coupling in automotive ICs [7][8].

The idea relies on constructing automatically a 3-D network that takes into account both majority and minority carriers propagation in substrate. This substrate network is composed of enhanced parasitic models [9][10] (i.e. EPFL diodes, resistor and homojunction) with extracted geometrical features from layout [11]. Those enhanced models are compact spice models (written in Verilog-A), which have two additional terminals introducing minority carriers’ concentration and gradient. At those terminal, the minority carriers concentrations are saved as voltage and their gradient are saved as current [12]. Therefore, bipolar effects can be simply modeled by two back-to-back (NPN) or front-to-front (PNP) diodes. By doing this, the substrate lateral NPN BJTs can be extracted and simulated [13]. As a feature of our modeling methodology, this substrate network can be back annotated to circuit schematic, which is impossible by using TCAD simulations. As a consequence, the behaviors of substrate currents can be observed by fast simulation at early phase before fabrication of first prototype [14][15][16].

III. LAYOUT-BASED EXTRACTION METHODOLOGY

In the following, our approach of post-layout extraction is introduced. The flow in Figure 2 describes the overall idea: our extraction flow consists of 2 parts: a) *extraction of substrate network*. An extraction engine is developed based on *OpenAccess* [17], and encapsulated in a CAD tool. The CAD tool is integrated in Cadence design environment of ams AG Hitkit Process Design Kit (PDK). The idea of substrate modeling and parasitic extraction can be simply illustrated as in Figure 1, and will be explained in the following paragraphs. b) *extraction of*

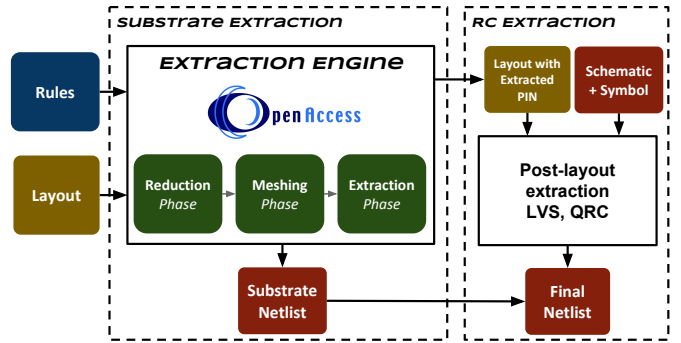


Fig. 2. Overall flow of post-layout extraction.

RC and netlist back-annotation. To back-annotate the substrate network with standard post-layout schematic, we extract pins at the interfaces of the substrate. Then these pins are extracted as short-vias between metal wires and substrate network. To extract the substrate parasitic, our methodology follows 3 steps:

A. Reduction Phase

The region of interest that we consider in our methodology is underneath transistor diffusion areas. In the one hand, we consider wells: e.g. deep N-well (DNTUB) and deep P-well (DPTUB) in ams AG 0.35 μm HV-CMOS technology process, and implants: e.g. N-implant (NDIFF) and P-implant (PDIFF). On the other hand, all the others: e.g. metal layers and via that do not contribute to the substrate parasitics are ignored in our methodology. Hence, specific rules are used to define the masks involved in a target technology process. The rules are formed in Extensible Markup Language (XML), thus written in XML file. Therefore, in our approach, we start by reducing layers from the original layout, and deriving a reduced version of layout that is used for further extraction.

B. Meshing Phase

Meshing of substrate region is based on lumped elements (i.e. cubes) in 3-D. Each element, has a different size, and models a lumped region in substrate. To complete the meshing in 3-D, we consider three steps: 1). Substrate layering; 2). 2-D surface meshing; 3). 2-D mesh refinement.

TABLE I
LAYER RELATION TABLE.

Index	Thickness (μm)	Wells and/or Implants
0	d_{DP}	NDIFF, PDIFF, DNTUB, DPTUB
1	$d_{DN} - d_{DP}$	DNTUB
2	$20 - d_{DN}$	N/A

1) *Substrate Layering*: For vertical meshing along z-axis, substrate will be divided into several stacked layers, or slices. The total number of slices is derived from the wells, thus their thickness are derived from the junction depths. For example, if we consider a substrate region of $20\mu\text{m}$ thickness, DNTUB and DPTUB are layers in our case (Figure 1 (b)). Eventually 3 slices are derived from vertical meshing. The “cut” through PN junction (DNTUB to P-substrate) and “cut” through DPTUB and P-substrate result in three slices: the slice on “top” includes DNTUB and DPTUB wells (Figure 3b); the slice in the “middle” includes only DNTUB (Figure 3c); and then the slice at “bottom” is only P-substrate region (Figure 3d). Table I records the relevant informations for meshing, such as thickness (second column) and involved wells or implants (third column) at each slice. Besides, N-type and P-type diffusions are considered as the contacts on the surface of “top” slice (Figure 3a).

2) *2-D Surface Meshing*: Once the substrate is layered, meshing on 2-D surface (x-y axis) is developed at each slice. Since wells have different junction depths, meshing on 2-D are different at each slice as well (see Figure 3). In our methodology, meshing on 2-D is based on points instead of shapes (e.g. rectangle or polygon is a combination of ordered points). The cost for computation and memory used increases as IC layout becomes more complex. Before meshing, we start to collect the vertices from the layers, and saved as:

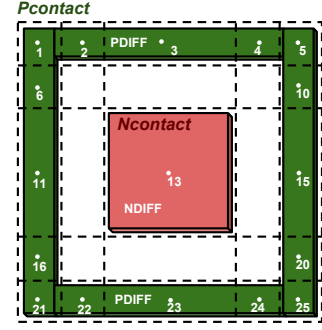
$$S = \{v1, v2, \dots, vn\}$$

where n is the total number of collected vertices, each one being a 2-D point, i.e. $v_j = (x_j, y_j)$. If one 2-D point can describe a location on the surface, then two 2-D points describe a line segment corresponding to a junction boundary. The extension of this line segment to the edges results in a mesh line (black line in figure). The projection of these vertices on x-axis is called $Xarray$, and the ones on y-axis is called $Yarray$. In our case, they can be expressed as:

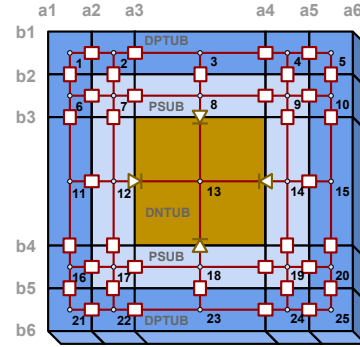
$$Xarray = \{a_1, a_2, a_3, \dots, a_p\}$$

$$Yarray = \{b_1, b_2, b_3, \dots, b_q\}$$

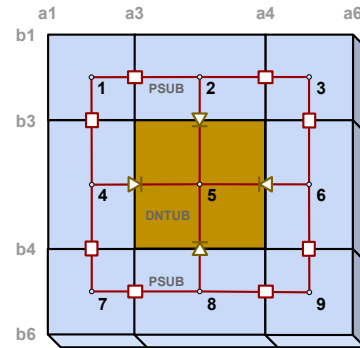
where p is the total number of coordinates in x-axis, and q is the one in y-axis. These two arrays build the coordinate system of resulting meshing. For each element in meshing, its depth equals to slice thickness (Table I), and its size on 2-D surface is defined by diagonal opposed corners, i.e. the lower left (LL) and upper right (UR) points. Eventually, the



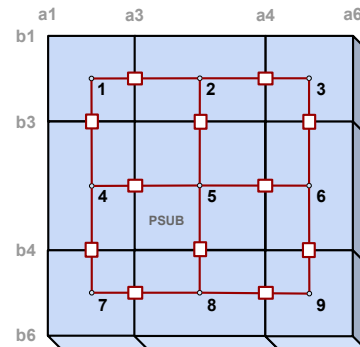
(a) N and P diffusions



(b) top layer (index=0)



(c) middle layer (index=1)



(d) bottom layer (index=2)

Fig. 3. 2D-meshing at each slice: (b) “top”, (c) “middle”, (d) “bottom”, and (a) N+/P+ diffusions on the surface of “top”. $\{a_1, a_2, \dots\}$ are coordinates at x-axis, and $\{b_1, b_2, \dots\}$ are coordinates at y-axis. Lines in black represent the mesh lines. Lines in red represent ideal connections in the future netlist. Component symbols in yellow and red are DNPS diodes and resistors in P-substrate respectively.

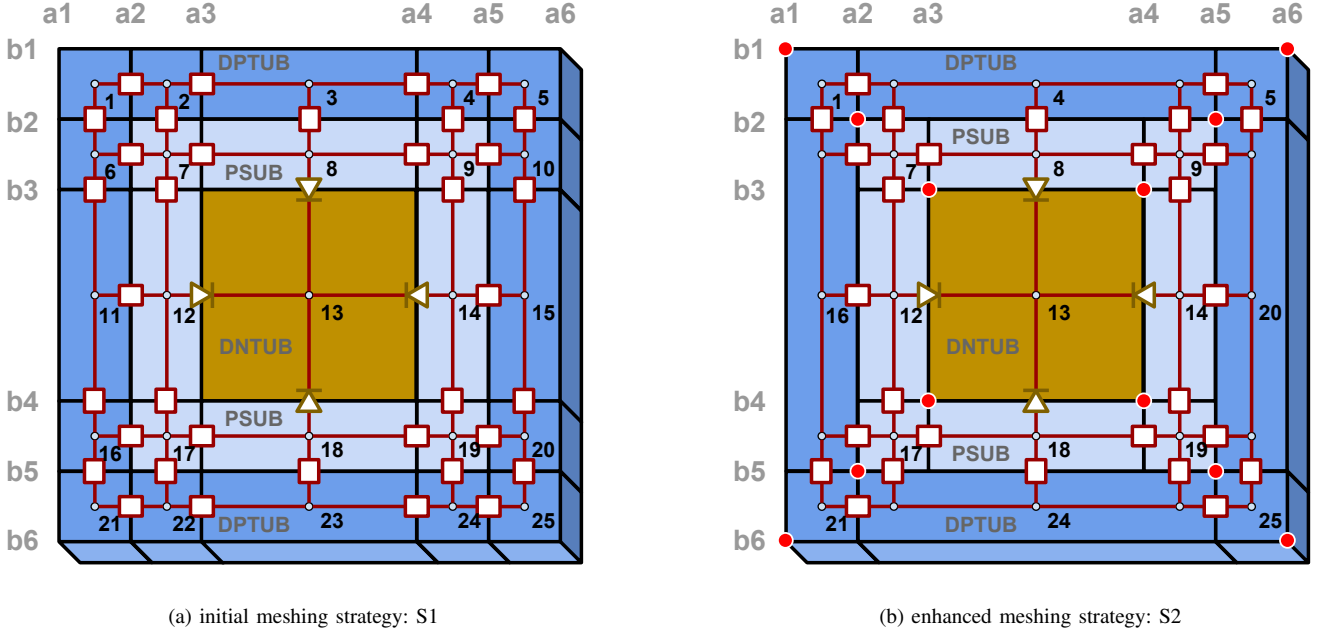


Fig. 4. Idea of 2-D mesh refinement at “top” slice. The red points in (b) represent the vertices of geometrical shapes (DPTUB layer is polygon and DNTUB layer is rectangle).

geometrical of element can be expressed as:

$$\begin{aligned} Length &= UR.x - LL.x \\ Width &= UR.y - LL.y \\ Depth &= d_{slice} \end{aligned}$$

Besides geometry, mesh element has been marked by material type. The available material types are: N-well, P-well, N-implant, P-implant, P-substrate.

3) *Mesh Refinement*: We have just introduced a methodology for substrate meshing. This method relies on a rectilinear mesh in 2-D where substrate region is modeled. In [18], an enhanced strategy for 2-D surface meshing was introduced, which contribute to reduce significantly the size of meshing, thus speed up the entire simulation time. In this section, we recall this mesh refinement strategy on the “top” slice of structure, thus the idea can be applied to each one of the entire meshing in 3-D.

- Initial meshing strategy (S1), as depicted in Figure 4a. In our methodology, mesh is constructed by cuboid in 3-D. Its height is defined by layer depth, and its surface (i.e. x-y) is defined by the diagonal opposed corners. To find these corners, a coordinate system in 2-D is built to help constructing the perpendicular mesh lines, thus the intersections are the corners of resulting mesh. For instance, mesh in Figure 4a has coordinates at the x-axis $Xarray=\{a1, a2, a3, a4, a5, a6\}$, and coordinates at the y-axis $Yarray=\{b1, b2, b3, b4, b5, b6\}$. These coordinates are the projection on x/y-axis of vertices from DNTUB, and DPTUB layers. As an example, vertices from DNTUB give the coordinate $\{a3, a4\}$ to Xarray and $\{b3, b4\}$ to Yarray.

- Enhanced meshing strategy (S2), as depicted in Figure 4b. Beginning with initial mesh, the technique of mesh refinement is applied to reduce the number of elements by combining small sized elements. For those small sized elements who can be merged, they have to meet the following 3 conditions: 1) same material type; 2) the resulting merged element form a rectangular shape; 3) the resulting shape does NOT overlap any vertices (red in Figure). For example, a group of initial elements $\{1, 2, 3, 4, 5\}$ (Figure 4a) overlaps vertices $(a2, b2)$ and $(a5, b2)$, hence they can not be merged even if they consist of the same material type. Thus, the group of initial elements $\{2, 3, 4\}$ (Figure 4a) can be merged to element 4 in Figure 4b. This has a consequence on the extracted parasitic components: the red line crossing the length of element 4 is an ideal connection, the parasitic resistors at the boundaries of elements 1 and 4 and elements 4 and 5 have to be modified to take into account the new geometry.

C. Extraction Phase

Extraction of parasitic components from meshing results in an equivalent netlist. This netlist consists of extracted components together with geometrical patterns. The extraction of component happens between two adjacent elements. Considering two elements, as illustrated in Figure 5, a parasitic component is extracted between their two centers. Depending on their material types, the resulting component can be either an enhanced diode (different material type), an enhanced resistor (same material types) or a homojunction (same material type but different doping concentration) [9] [10]. The parameters to extract are length, area, etc (see Table II).

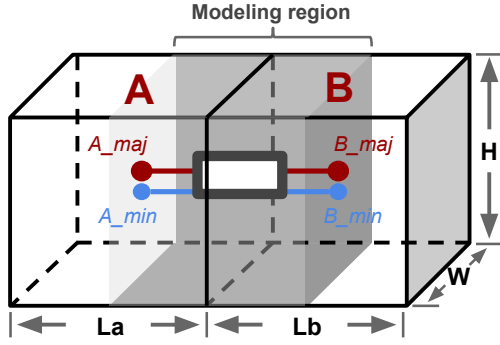


Fig. 5. Basis of a parasitic component extraction from 2 meshed cuboids. Centers act as nodes in resulting netlist. At each center, two nodes are used: one for majority carriers (red) and the other for minority carriers (blue).

TABLE II
LIST OF PARAMETERS TO EXTRACT FOR PARASITIC COMPONENTS.

Parasitic model	Doping profile	Geometrical parameters	
		Length [m]	Area [m^2]
Diode	n	$L_a/2$	$w \times h$
	p	$L_b/2$	
Resistor	n or p	$L_a/2 + L_b/2$	
Homo-junction	n or p	$L_a/2$	
	n+ or p+	$L_b/2$	

Besides geometry, semiconductor materials are extracted as well. For instance, resistor extracted from DNTUB well differs from the one extracted from DPTUB well in terms of silicon doping, and they differ from the one extracted from P-substrate as well. Therefore, resulting extracted resistors are differentiated by definition, such as:

- R_{DP} : inside DPTUB well;
- R_{DN} : inside DNTUB well;
- R_{PS} : inside P-substrate.

The same idea stands for enhanced parasitic model of diode and homojunction. Table III lists all combinations of parasitic component to extract according to describing rules.

TABLE III
POSSIBLE COMBINATIONS AND THE AVAILABLE PARASITIC COMPONENTS.

	PSUB	DNTUB	DPTUB	NDIFF	PDIF
PDIF	H_{PD-PS}	D_{PD-DN}	H_{PD-DP}	N/A	N/A
NDIFF	D_{ND-PS}	H_{ND-DN}	D_{ND-DP}	N/A	
DPTUB	H_{DP-PS}	D_{DP-DN}	R_{DP}		
DNTUB	D_{DN-PS}	R_{DN}			
PSUB	R_{PS}				

IV. MODEL BENCHMARKING

Calibration of technology parameters, such as doping profile and carriers' lifetime, is performed using industrial benchmark structures. Various structures to benchmark the diodes in terms of geometry (area, perimeter), and technology patterns (e.g. DNPS diode, DPDN diode, etc) are provided by ams AG.

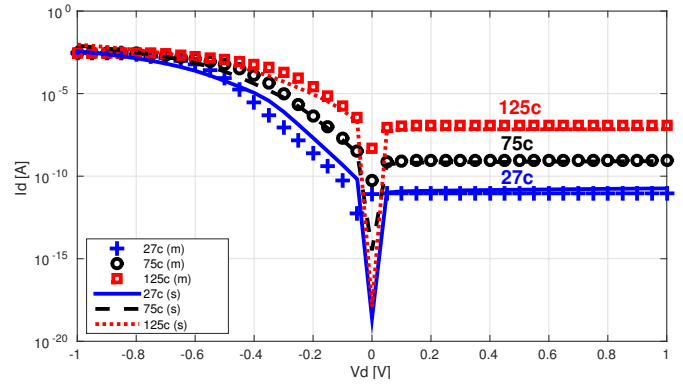


Fig. 6. Temperature behaviors in both forward and reverse biased conditions, at 27°C (blue), 75°C (black) and 125°C (red).

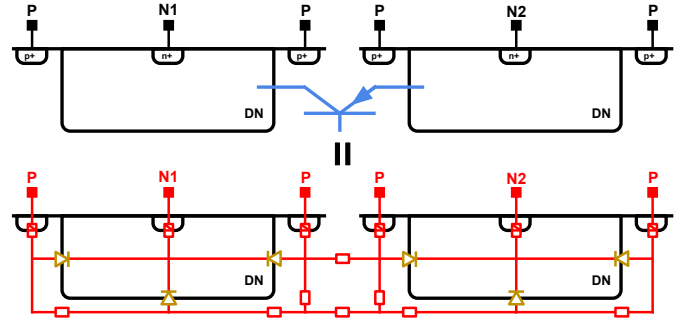


Fig. 7. Illustration of parasitic lateral NPN BJT and its equivalent circuit.

Benchmark structures are extracted using tool and parameters are calibrated using special algorithm to fit simulation results with measured data. We will not detail the calibration process itself, but we show the results of model benchmarking.

A. Modeling of diode

As the first case study, a benchmark structure of DNPS diode has been investigated. The structure under study is an area diode with dimension $800\mu m \times 800\mu m$. The output parameters from extraction and simulation are summarized in Table IV. Results of DC behaviors including forward and reversed biased conditions are reported in Figure 6. Results from simulations are drawn with straight lines and measurements with dots. In the same figure, curves in colors illustrate also the temperature behaviors at: 27°C (blue), 75°C (black) and 125°C (red).

B. Modeling of lateral NPN

Modeling of parasitic lateral NPN BJT is a hard task. In HV-CMOS technology, the emitter of NPN BJT is the injecting N-well of substrate currents (usually power device), the collectors are the surrounding N-wells while the base is the whole substrate. Therefore, extraction of this parasitic device with layout geometry becomes impossible by using standard BJT model. In our methodology, modeling of such parasitic lateral NPN BJT is realized by constructing substrate network as shown in Figure 7. This substrate network models lateral

TABLE IV
OUTPUT PARAMETERS FOR SIMULATION.

Test structures	DNPS	Test-chip1	VERTN1	VERTPH	Current mirror	Test-chip 2	
Total number of nodes	154	1958	238	313	871	6561	
Total number of components	262	3419	440	601	1619	12291	
Substrate extraction	diode*	17	487	71	54	304	2766
	homojunction*	68	163	76	147	261	807
	resistor*	177	2676	280	392	1007	8193
Extraction time (s)		1.96	19.71	2.23	2.57	16	20.82
QRC extraction	diodes	1	15	0	0	0	11
	capacitor	0	47	9	3	8	104
	resistor	0	31	4	5	27	286
	bjt	0	0	0	0	4	62
	jfet	0	0	0	0	8	62
Simulation time (s)		2.5	12.6	1.1	1.23	14.2	295

Components with * are enhanced parasitic models
Work is performed with Intel Core i5-3470S Processor (2.9GHz)

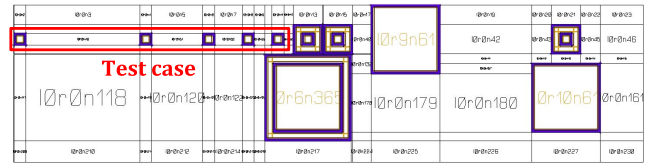
NPN BJT with back-to-back diodes only according to layout geometry. Eventually, bipolar effect of parasitic lateral NPN can be added to circuit schematic.

The second structure is from an industrial design test chip, named *test-chip 1*. This test chip has 15 DNPS diodes sharing the same substrate. It has 16 I/O PADS: the first 15 of them (PADs 1 to 15) connect to each of the 15 N-wells individually, and the last one (PAD16) connects to P-well rings, which are the surrounding substrate contact of the 15 N-wells. The whole test-chip is extracted using our methodology (reported in Table IV). Extraction of whole chip is performed in two steps: 1) the extraction of device (each DNPS diode individually); 2) the extraction of substrate region outside devices. The structure with meshing is depicted in Figure 8a. Since the models in ams AG process include these 15 DNPS diodes, they should be disabled during circuit simulations because our substrate model already takes them into account.

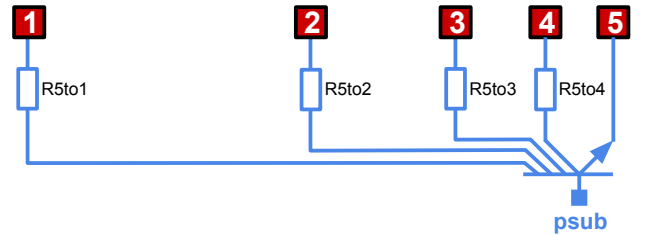
In our test case, as shown in Figure 8b, 5 Nwells PAD1 to PAD5 are involved. We mainly focus on this test structure the investigation of parasitic lateral NPN BJTs where the distance effect is under study. Each N-well has the same dimension ($20\mu\text{m} \times 20\mu\text{m}$), thus different spacing to PAD 5. As for simulation, PAD5 is the emitting point of substrate current while collector is one of the 4 other PADs, and the others are left open. A good agreement to measurements shows reliable results from simulation (see Figure 9), while the temperature behaviors are considered as well.

C. Modeling of vertical NPN and PNP

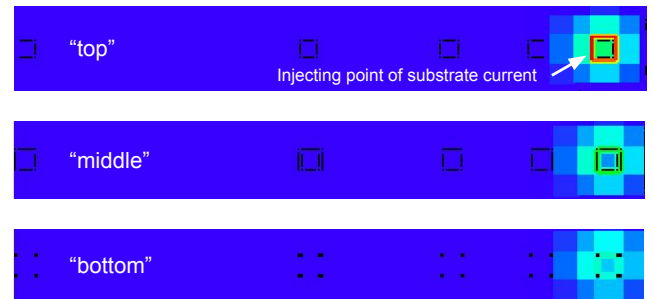
In HV-CMOS technology, a deep N-well isolates the transistors from the substrate. Inherently this structure introduces a parasitic vertical NPN (for N-MOS) or PNP (for P-MOS) bipolar junction transistor (BJT). The drain of P-MOS transistor corresponds to the emitter of vertical PNP, which is usually connected to the load. The below ground or above supply voltage condition activates the vertical BJT that injects substrate current into the substrate. This kind of configuration is often seen in HV automotive application. Typically, the effect of parasitic vertical BJT can be added in compact



(a) Meshing of test-chip



(b) Test case



(c) Color map in test case

Fig. 8. (a) Meshing of the entire test-chip; (b) simplified structure of test case. (c) color map of voltage distribution in terms of minority carriers.

model of standard spice model. However, the propagation of substrate currents is impossible to model since they are layout dependent. Hence, modeling of parasitic BJT is also considered in our methodology.

In previous test structure, effect of the parasitic lateral NPN is observed by adding lateral connected back-to-back diodes

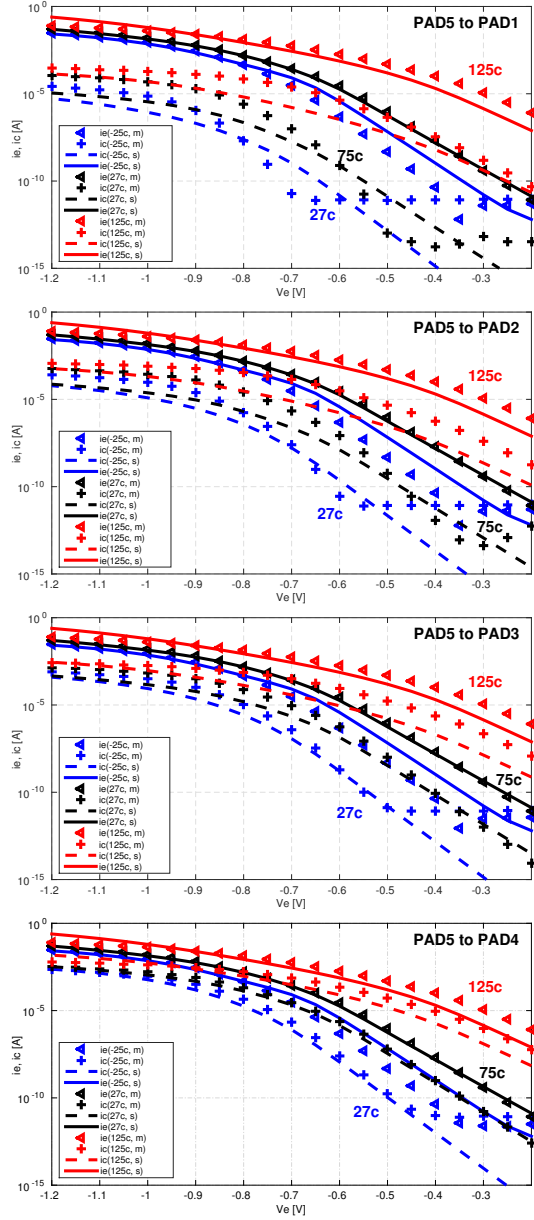


Fig. 9. Current-voltage characteristics and temperature behaviors: -25°C (blue), 27°C (black) and 125°C (red) of parasitic lateral NPN BJTs. The currents at emitter (I_e) and collector (I_c) are shown in figure while simulation (straight lines are I_e and dash lines are I_c) is compared to measurement (triangle symbols are I_e and circle symbols are I_c). The distance effect is observed also from the 4 test cases where collector is PAD1 to PAD4 respectively (from top to bottom).

between N-wells. Following the introduced methodology, extraction of parasitic vertical BJT results from various N and P wells of the substrate. Hence, various types of parasitic diodes are extracted at the PN junction of wells. The back-to-back connection of these enhanced diodes propagates minority carriers allowing NPN transistor simulations. In the same way, the front-to-front connection of the enhanced diodes can simulate parasitic PNP transistor [9].

Besides the DNPS diode (yellow), DPDN diode (blue) and NDDP diode (green) are the two other parasitic diodes to extract (as mentioned at Table III). The calibration of these

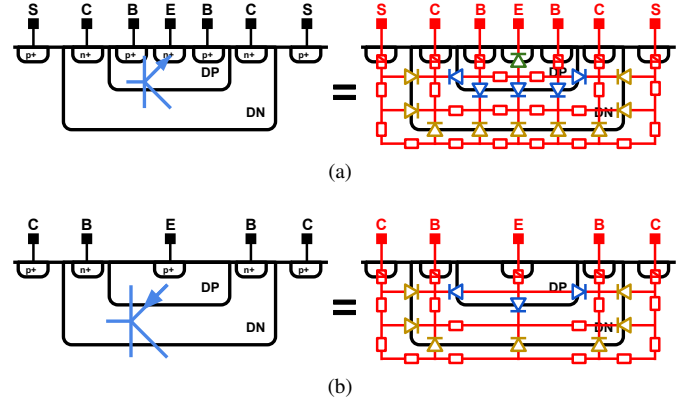


Fig. 10. Structure of NPN (VERTN1, a) and PNP (VERTPH, b) BJT and their equivalent circuits modeled by our methodology.

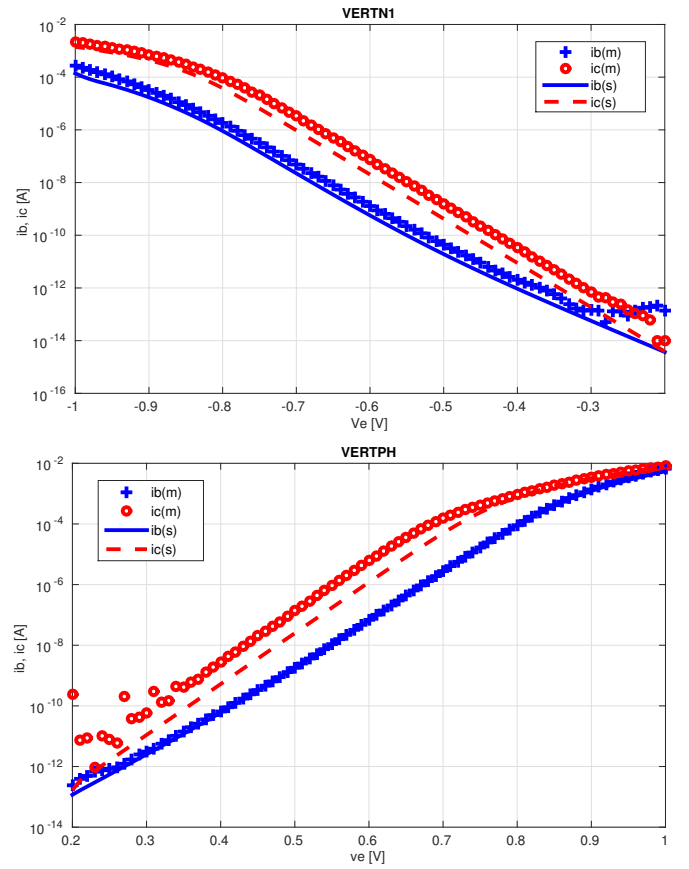


Fig. 11. DC behaviors of NPN (VERTN1, a) and PNP (VERTPH, b) BJT. Results of simulation (lines) are compared to measured data (symbols).

diodes are performed by using the standard bipolar cells from library which has well defined structure of vertical BJT, see Figure 10. Report on extraction and simulation of two BJTs is summarized in Table IV. It has to be noticed that if the target process/models include already these parasitic vertical BJT's then designers would need to disable the instantiation of these BJT's during circuit simulations, since they are included in our substrate model. Curves from simulation are depicted in Figure 11, DC behaviors of BJTs are confirmed by fitting the simulation with measured data.

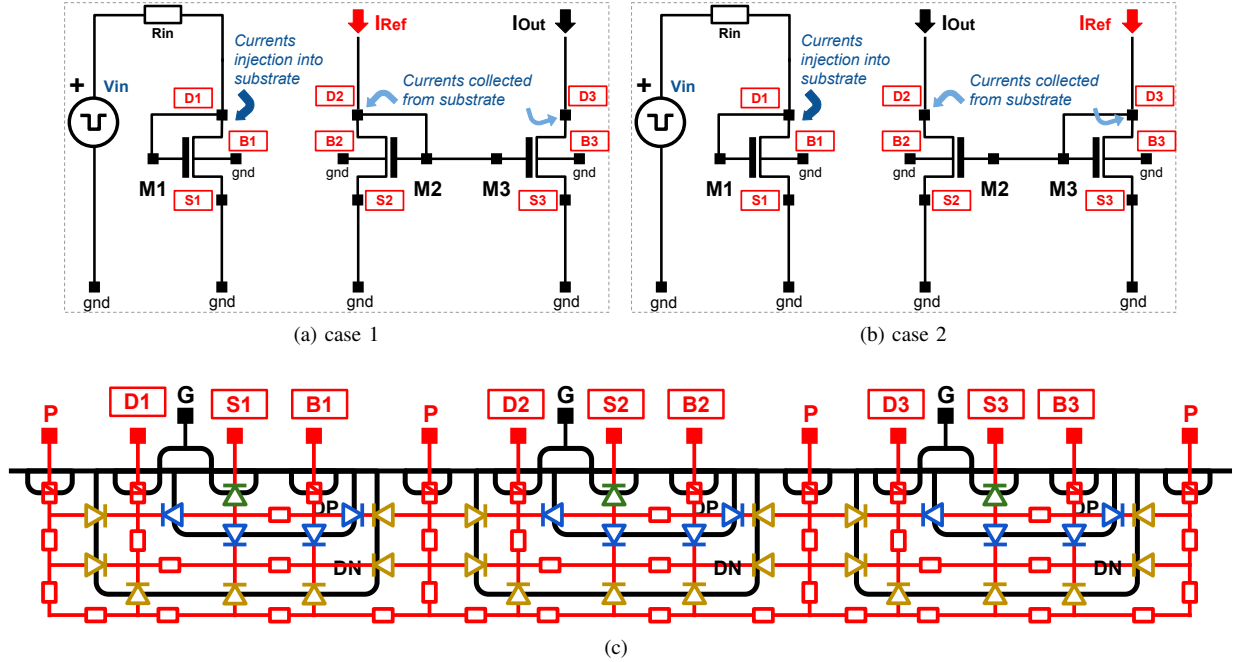


Fig. 12. (a, b) Test circuit of 2 current mirror configurations, and (c) the equivalent substrate network.

V. CASE STUDY

A. Current Mirror

Current mirror is a simple circuit that is widely used in analog IC design. This circuit is designed to replicate a current through one active current path (reference current) to another active current path of circuit, therefore keeping the output current constant regardless of loading. In this case under study, we are interested in the influence of substrate currents to this basic analog circuit. The test circuit is illustrated in Figure 12. Transistor M1 is a self-biasing N-channel LDMOS transistor that injects substrate currents from a negative supply voltage source marked as “Vin” in figure. Transistors M2 and M3 are also N-channel LDMOS and have the same size (i.e. W and L) as transistor M1, thus transistor M2 is closer to M1 than transistor M3 in layout point of view. They are used as a current mirror sink having two different configurations:

- case 1: transistor M2 is the current source of current mirror configuration, it is closed to aggressor M1;
- case 2: transistor M3 is the current source of current mirror configuration, then it is farther from aggressor M1;

The extracted substrate networks in both cases are the same, because they have the same geometry in substrate as depicted in Figure 12c. The extracted netlist of substrate parasitic is back-annotated to circuit schematic through the extracted PIN. A transient signal of negative pulse ($-1V$, $2\mu s$) is applied to input voltage source, see Figure 13. The below ground condition at drain of transistor M1 causes current injection into substrate. As a consequence, the forward biasing of DNPS diode at M1 triggers the parasitic lateral NPN BJT. Hence, currents are coupled to DNTUB wells of transistor M2 and M3. Depending on the distance between devices, the coupled currents are different: $I_{subM2} > I_{subM3}$, since

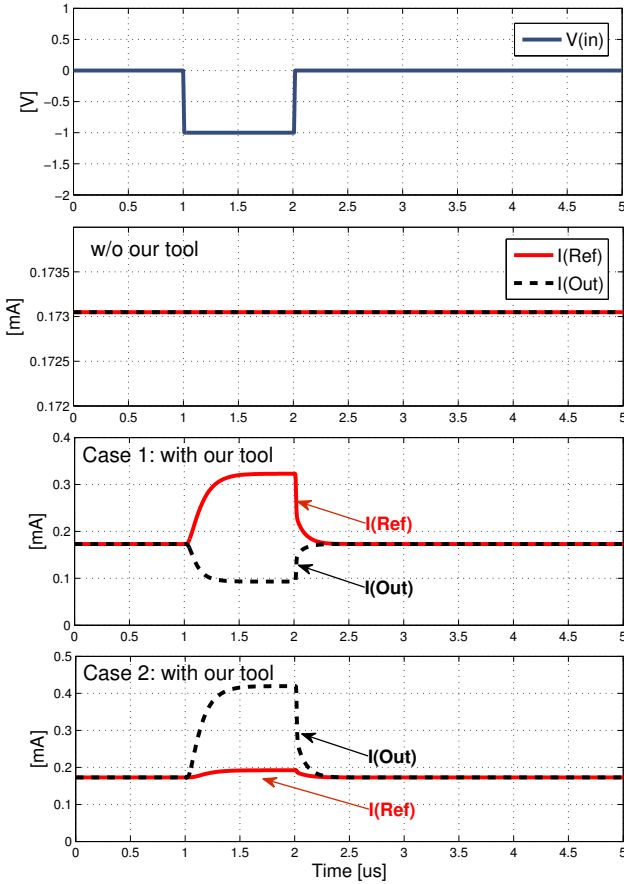


Fig. 13. Transient behaviors with substrate current injection.

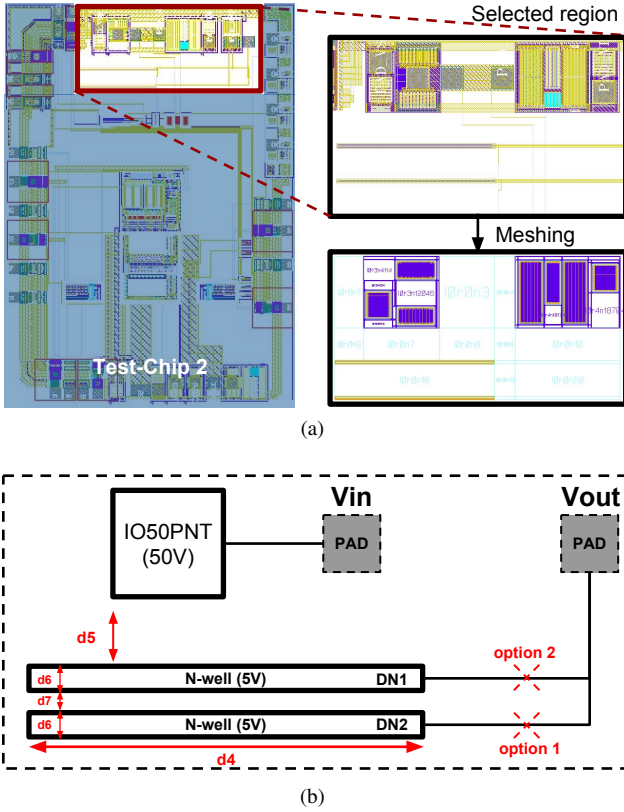


Fig. 14. (a) Layout view of test-chip 2 and chosen test case; (b) simplified structure of test case.

$d_{M1-M2} < d_{M1-M3}$. As a consequence, the voltage drop at DNTUB of transistor M2 is higher than of transistor M3.

- In case 1, transistor M2 is the source of current mirror who converts current into voltage. The voltage drop at drain of M2 (D2) causes the drop of controlling voltage at the gate of M2. Because controlling voltage drops, the mirrored current at transistor M3 decreases. However, the drop of mirrored current cannot be compensated by the increase of coupled substrate currents, then the total current at M3 (I_{Out}) decreases. On the contrary, the total current at M2 (I_{Ref}) increases since the coupled substrate currents are more significant.
- In case 2, transistor M3 is the source of current mirror. Since M3 is farther than M2 from the aggressor of substrate currents, the interference of coupling to mirrored current is less than in the previous case. Hence the decrease of mirrored current is less important than the coupled substrate currents. In both sides, the total currents at M2 (I_{Out}) and M3 (I_{Ref}) are increased depending on the distance to M1.

In Figure 13, results of simulation confirm the correct behaviors of substrate parasitic NPN BJT under test conditions. The interferences of substrate noise to the basic current mirror circuit are clearly observed by using our tool. However, this effect cannot be simulated in the conventional way since the lack of modeling of parasitic NPN BJTs.

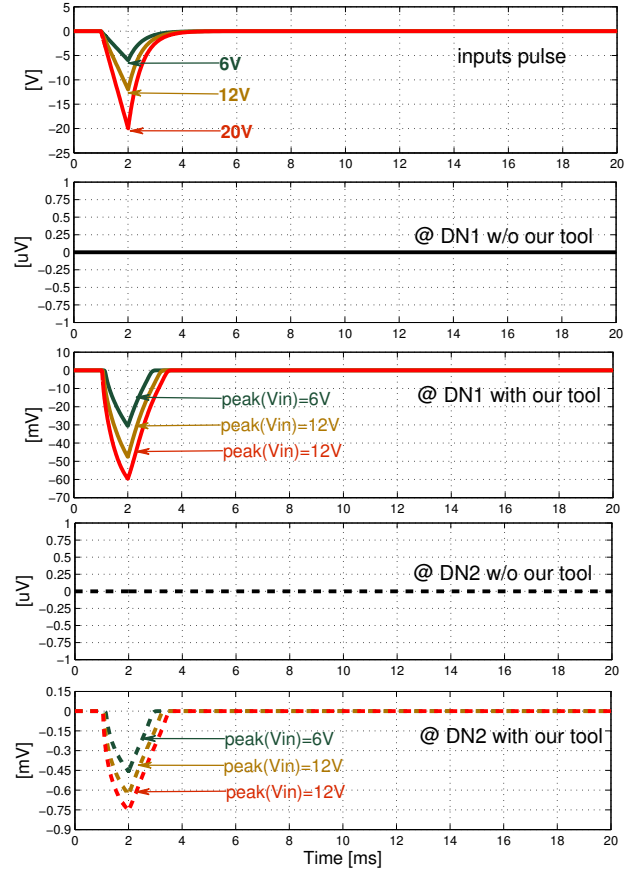


Fig. 15. Result of fast transient simulation with automotive test pulse: as 6V, 12V or 20V peak voltage. Voltages simulated at output on 50Ω with or without our tool. Laser cut option to choose the corresponding N-well: DN1 or DN2.

B. Test-chip 2

The second test case is from an industrial design and fabricated test chip [19]. The principle structure under study is shown in Figure 14. The entry is an IO PAD which consists of two series connected diodes supplied between VDD and ground. The injection point for the aggressor is between two diodes marked as “Vin” in Figure 14. Two N-wells with geometry $d_4 \times d_6$ each, are placed to collect the injected charges. The distance to the emitter is different as d_5 for the closer placed one (DN1) and $d_5 + d_6 + d_7$ for the second one (DN2). The output “Vout” is implemented as PAD. Laser cut options are used to connect or disconnect the different N-wells to PAD “Vout”.

In order to reach production maturity, all automotive products must pass qualification tests. Some of these tests may cause substrate parasitic currents. In our test case, a standard automotive test signal (ISO 7637-2 Pulse 1) is applied as injecting signal to PAD “Vin”. This input signal is an example of severe test signal requiring that the product remains fully functional while the output terminals are stressed with negative voltage. The behavior of this test signal is shown on the top of Figure 15. It simulates a negative polarity transient pulse caused by the disconnection of the DC supply through an inductive load. The peak voltage “Vs” is varied as 6V, 12V

and 20V for different tests. The recovery time of this pulse signal is 2ms. Finally the voltage supply VDD is 14V.

Results for this tests are shown in the rest of the Figure 15 as voltage at output "Vout" measured on 50Ω. The curves displayed are according to the different values of peak voltages: 6V (green), 12V (yellow) and 20V (red). In the conventional way, signals caused by substrate coupling cannot be simulated. However by using our tool, pulse signals are observed on the corresponding well (DN1 and DN2). In agreement, the simulated signal on the corresponding well is higher for the larger input signal. Shorter distance to the substrate current source results in a higher signal.

VI. CONCLUSION

Substrate noise modeling becomes of interest for designing Smart Power ICs. The noise coupling in substrate is due to carriers injection and propagation, in particular from HV power devices. Moreover, they could be even worse in high operating temperature condition. In conventional way, this kind of coupled noises are not predictable in simulation because the lack of modeling of substrate parasitic lateral NPN. In this paper, a post-layout extraction and simulation methodology for substrate parasitic was presented. This methodology is based on a layout extraction tool where substrate network is generated. The use of our tool completes the existing post-layout verification flow. Thus the behaviors of substrate currents can be also taken into account in simulation. In 0.35μm process node of ams AG HV-CMOS technology, we extracted the technology parameters of substrate model from various benchmark structures. We have investigated in this work the effect of parasitic lateral NPN BJTs in two different test cases: the interferences of substrate currents to a current mirror configuration was studied at first. Then, an automotive test case was included. The proposed approach at post-layout stage gives the designers the possibility to simulate the substrate parasitic behaviors. The verification at early phase before fabrication enables the optimization of design against substrate coupling. Eventually, it contributes to reduce the design cycle thus increases the reliability and safety of Smart Power ICs.

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