



**HAL**  
open science

## The channeling effect of Al and N ion implantation in 4H-SiC during JFET integrated device processing

Mihai Lazar, Farah Laariedh, Pierre Cremillieu, Dominique Planson,  
Jean-Louis Leclercq

► **To cite this version:**

Mihai Lazar, Farah Laariedh, Pierre Cremillieu, Dominique Planson, Jean-Louis Leclercq. The channeling effect of Al and N ion implantation in 4H-SiC during JFET integrated device processing. Nuclear Instruments and Methods in Physics Research Section B: Beam Interactions with Materials and Atoms, 2015, 365, pp.256 - 259. 10.1016/j.nimb.2015.07.033 . hal-01391844

**HAL Id: hal-01391844**

**<https://hal.science/hal-01391844>**

Submitted on 9 May 2019

**HAL** is a multi-disciplinary open access archive for the deposit and dissemination of scientific research documents, whether they are published or not. The documents may come from teaching and research institutions in France or abroad, or from public or private research centers.

L'archive ouverte pluridisciplinaire **HAL**, est destinée au dépôt et à la diffusion de documents scientifiques de niveau recherche, publiés ou non, émanant des établissements d'enseignement et de recherche français ou étrangers, des laboratoires publics ou privés.

# The channeling effect of Al and N ion implantation in 4H-SiC during JFET integrated device processing

M. Lazar<sup>1</sup>, F. Laariedh<sup>1</sup>, P. Cremillieu<sup>2</sup>, D. Planson<sup>1</sup>, J.-L. Leclercq<sup>2</sup>

<sup>1</sup>Université de Lyon, Laboratoire AMPERE, INSA Lyon, UMR CNRS 5005, 21 Avenue Jean Capelle, 69621 Villeurbanne, France,

<sup>2</sup>Université de Lyon, Institut des Nanotechnologies de Lyon, Ecole Centrale de Lyon, UMR CNRS 5270, 36 Avenue Guy de Collongue, 69134 Ecully, France

## Abstract

A strong channeling effect is observed for the ions of Al and N implanted in 4H-SiC due to its crystalline structure. This effect causes difficulties in subsequent accurate estimation of the depth of junctions formed by multiple ion implantation steps. A variety of lateral JFET transistors integrated on the same 4H-SiC wafer have been fabricated. Secondary Ion Mass Spectrometry measurements and Monte-Carlo simulations were performed in order to quantify and control the channeling effect of the implanted ions. A technological process was established enabling to obtain devices working with the presence of the channeling effect.

**Keywords:** 4H-SiC, lateral JFET, ion implantation, channeling effect, Monte-Carlo simulations, SIMS

## 1. Introduction

Silicon carbide (SiC) is a wide bandgap semiconductor. The bandgap of the 4H-SiC (the most frequently polytype used in power electronic devices) is 3.27 eV, conferring higher thermal stability compared to conventional silicon. The thermal conductivity is also 3 times higher and the breakdown critical electric field approximately 10 times higher [1, 2].

Power discrete SiC devices are already commercialized as Schottky diodes, BJT, JFET and MOSFET. A monolithic integration of this type of devices in SiC single crystal wafers is suitable to improve performance and reliability in power electronics. The size of the resulting converters is thus reduced, improving the switching operation and significantly decreasing the power loss.

For this purpose, structures must be fabricated involving a high number of specific technological steps as the plasma reactive-ion-etching (RIE) and doping by ion implantation. Due to the low values of diffusion coefficients of dopants in silicon carbide (SiC), ion implantation is required during fabrication of power SiC devices. Al and N are the typical dopants to form p and n-type layers in 4H-SiC.

In this work we fabricated a variety of 4H-SiC JFET transistors with lateral channel conduction (L-JFET). A considerable number of ion implantations of Al and N have been performed in order to realize p and n-type wells under the contact electrodes, buried channels and other specific layers necessary to prevent the electric field increase inside the device. The distribution in the hexagonal 4H-SiC crystalline structures of the implanted ions and particularly the channeling effect [3] are critical for the JFET operation and their electrical output

characteristics. Wafer and consequently crystal disorientation are imposed in order to minimize the channeling effect in 4H-SiC without being able to completely eliminate it [4]. In order to quantify and accurately control the depth of the implanted layers and the influence of the channeling effect of the dopant ions, we have performed a specific experimental study based on Secondary Ion Mass Spectrometry (SIMS) measurements and Monte-Carlo (MC) simulations. A number of batches of JFET transistors have been fabricated.

## 2. Experimental details

To avoid amorphisation, ion implantations have been performed at  $\sim 400^\circ\text{C}$  in disoriented 4H-SiC wafers. The tilt was  $7^\circ$  from the wafer normal and the rotation  $90^\circ$  with respect to the wafer flat, assuming a  $8^\circ$  off-axis surface and the wafer flat parallel to  $\langle 11\bar{2}0 \rangle$ . Multiple energy implants always started with the highest energy. To electrically activate the Al and N ion implanted dopants, post-implantation annealing at  $1700^\circ\text{C}$  during 30 min has been performed in a RF-induction furnace with a C- cap [5]. The different structures are isolated by dry RIE etching using  $\text{SF}_6/\text{O}_2$  chemistry and Ni based hard mask [6]. Ohmic contacts have been obtained using Ni for the back-side of the  $n^+$  substrate and on  $n^+$  wells, and using a specific Ni-Ti-Al alloy on the  $p^+$  wells [7]. These contacts have been annealed by Rapid-Thermal-Annealing under Ar at  $900^\circ\text{C}$  and  $800^\circ\text{C}$ , respectively.

The transistors fabricated in this process have been electrically characterized by current-voltage (I-V) measurements with a "Signatone S1160" probe station and "Keithley 2410" Source Measure Unit (SMU). Electrical characterizations were carried out at room temperature without a substrate bias.

### 3 First batches of SiC L-JFET

Lateral SiC-JFETs were fabricated on 4H-SiC epitaxial wafers, and JFETs with p and n-type channels have been obtained on individual  $n^+$  and  $p^+$  substrates (Fig. 1). The drift region between the drain and the source areas has a double RESURF (Reduced Surface Field) structure based on the super-junction theory [8]. These areas with the channel have been made by ion implantation.

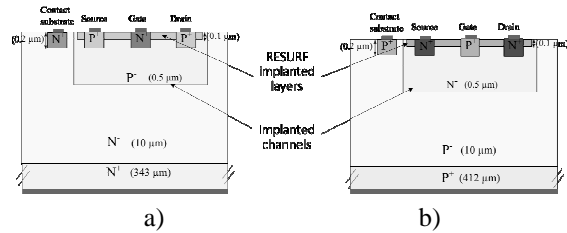


Fig.1. Schematic presentation of the SiC L-JFET with, a) p-type channel and b) n-type channel

Considering also the  $p^+$  and  $n^+$  wells under the contacts, a number of six ion implantations have been made, the type of doping of various layers depending on the type of transistor (n-channel or p-channel). The doping profiles have been obtained and optimized by SRIM (Stopping and Range of Ions in Matter) Monte Carlo-type simulations [9]. The doping profiles are shown in Fig. 2.

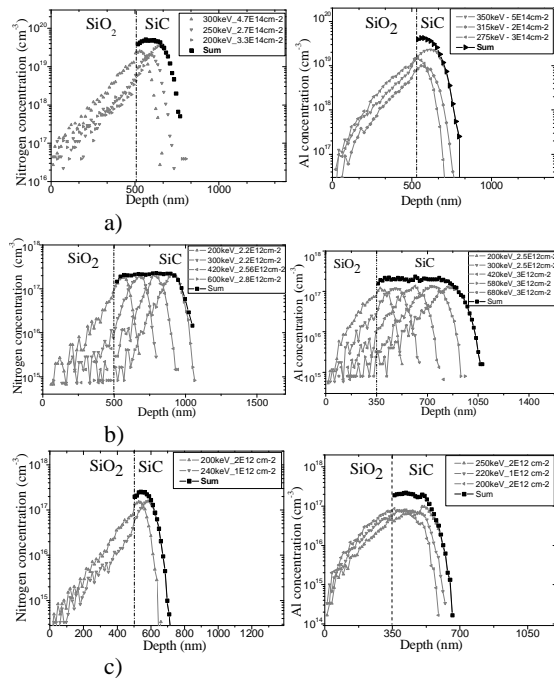


Fig.2. Ion implantation parameters obtained by SRIM simulations for : a) source, drain and gate of  $n^+$  and  $p^+$  wells, b) n-type and p-type channels, c) n-type and p-type RESURF layers.

During fabrication of the transistors from the first lot only one ion implanter accelerator 100 to 400kV has been used. We created "box" profiles with multiple ion energies of Al and N over the ranges

between 200 to 680 keV. Double charged ions have been implanted to avoid contaminations ( $^{16}\text{B}^{11}\text{O}$  has the same mass as  $^{27}\text{Al}$ ). In order to obtain profiles close to the SiC surface a thin  $\text{SiO}_2$  layer has been deposited onto the SiC samples. The thickness has been calculated by SRIM simulation considering the whole structure ( $\text{SiO}_2$  and SiC).

Figure 3 presents typical  $I_{\text{DS}}-V_{\text{DS}}$  electrical characteristics, plotted as a function of  $V_{\text{GS}}$ , for both n and p-type JFETs. We obtain a modulation of the channel resistivity by varying the  $V_{\text{GS}}$  gate-source bias only for the N-JFET. The drain saturation current is 6 mA at a gate voltage of 1 V. For the P-JFET the current is very small (in the  $\mu\text{A}$  range) and the p-type channel seems to be always blocked off. As we designed (600V) power devices, structures with large distances between wells have been fabricated (in the order of  $10\mu\text{m}$ ), leading us to the conclusion that the blocking behavior is not due to a lateral undermask penetration of ions which is limited to few micrometers [10].

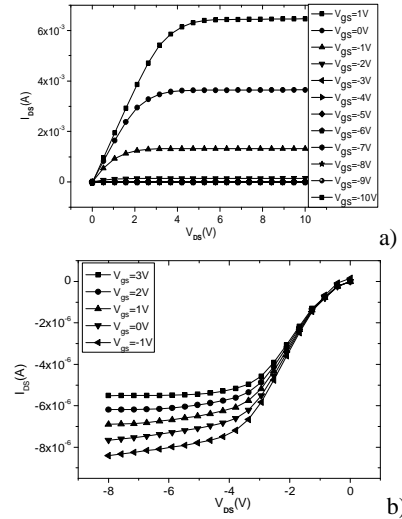


Fig.3. Typical  $I_{\text{DS}} - V_{\text{DS}}$  versus  $V_{\text{GS}}$  characteristics of the a) N-JFET and b) P-JFET from the first batches.

The electrical characteristics obtained on the fabricated transistors determined us to analyze and reconsider the ion implantation parameters and the technological process employed. If high energy ion implantation is benefic to obtain deep channels it seems to be an impediment in the creation of isolated  $p^+$  and  $n^+$  wells in surface. High energies involve also high projected ranges ( $\Delta R_p$ ), and a spreading in the depth of the gate profiles. Moreover, the MC simulations with SRIM do not consider the crystalline structure of the 4H-SiC and consequently the presence of the channeling phenomenon was ignored. The channeling of the Al implanted ions in 4H-SiC is quite difficult to control and to eliminate even when an amorphous layer as  $\text{SiO}_2$  is present in the surface [11]. Therefore the channel of the P-JFET seems to be obstructed and even hidden by the presence of the gate layer implanted at the surface, as Fig. 4 schematically presents.



and  $n^+$  wells, thanks to the lack of the  $\text{SiO}_2$  layer in surface. For the  $p^+$  and  $n^+$  wells we changed also the ion implanter accelerator, a medium current Eaton has been utilized. This allowed us to decrease the ion energies in the 25 to 60keV for the Al and 25 to 100 keV for the nitrogen. Therefore lower  $\Delta R_p$  values have been obtained for the multiple ion implants performed for the  $p^+$  and  $n^+$  gates.

Decreasing the thickness of the gates by decreasing the ion implantation energies and predicting the channeling part of the doping profiles allowed us to obtain thicker n and p-type channels. Figure 9 shows the  $I_{DS}-V_{DS}$  electrical characteristics plotted as a function of  $V_{GS}$  for n and p-type JFETs from the second batches. The N-JFET is measured on the high voltage structure and the P-JFET on the low power structure. We can observe that even the electrical current through the n-type channel is increased. The drain saturation current is measured at 100 mA at a gate voltage bias of 0 V.

The conduction in the lateral P and N-JFET is improved by decreasing the channel resistances. The channel resistance is decreased by increasing the channel depths as well as by preserving the channel doping from the compensation which can occur from the channeling part of the gate doping. Monolithically integrated P and N-JFET transistors with a normally-on conduction are obtained.

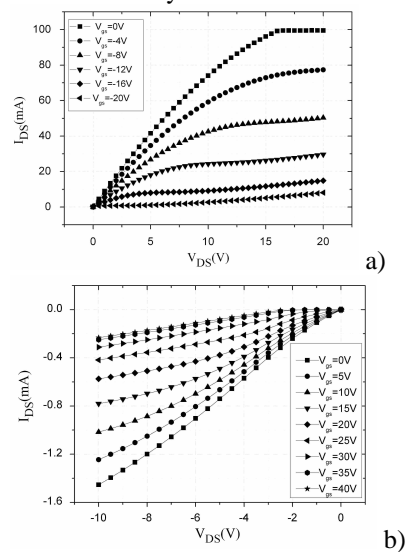


Fig.9. Typical  $I_{DS} - V_{DS}$  versus  $V_{GS}$  characteristics of the a) N-JFET (high voltage structure) and b) P-JFET (low power structure) from the second batches.

## Summary

We fabricated various JFET transistors, with n and p-type channels, integrated on the same 4H-SiC wafer. A considerable number of ion implantations have been performed in order to obtain p and n-type wells under the contact electrodes, buried channels and other specific layers necessary to prevent the electric field increase inside the device. In order to quantify and control the influence of the channeling effect of the implanted ions, we have performed an

experimental study based on SIMS measurements and MC simulations with a dedicated code considering the 4H-SiC crystalline structure. Several processing batches have been fabricated, and finally a new technological process was defined that enables to obtain P and N-JFET devices working within the presence of the channeling effect.

The number of ion implantation steps has been reduced. A particular effort has been done in order to carefully preserve the channel and avoid masking by the channeling part of the gate doping. The depth of the channels has been increased by implementing the highly doped wells for the gates in surface using low energy ion implantations while keeping high energy ion implantations for the realization of channels. For the low power structures the channels were not created by ion implantation, the channel conduction being ensured directly by the epitaxial CVD layers.

Limiting (but not eliminating) the channeling phenomenon in the hexagonal SiC, we showed that it becomes possible to fabricate on the same 4H-SiC wafer integrated and operating lateral JFET with even a p-type conduction channel. Increasing the tolerances of the structural device parameters (thickness and doping) allows us to obtain JFET transistors with a normally-on conduction.

## References

1. M. Willander, M. Friesel, Q.-U. Wahab and B. Straumal, *Journal of Materials Science: Materials In Electronics* 17 (2006) 1
2. A. Hiroyuki Matsunami, *Japanese Journal of Applied Physics*, 43, No. 10 (2004) 6835
3. B. El-Kareh "Fundamentals of Semiconductor Processing Technology", (Springer 1995) p.401
4. J. Wong-Leung, M. S. Janson, B. G. Svensson, *J. Appl. Phys.*, 93, No. 11 (2003) 8914
5. E. Oliviero, M. Lazar, A. Gardon, C. Peaucelle, A. Perrat, J. J. Grob, C. Raynaud, D. Planson, *Nucl. Instrum. Meth. B* 257 (2007) 265
6. M. Lazar, F. Enoch, F. Laariedh, D. Planson, P. Brosselard, *Mater. Sci. Forum.* 679-680 (2011) 477
7. F. Laariedh, M. Lazar, P. Cremillieu, J. Penuelas, J.-L. Leclercq, D. Planson, *Semicond.Sci Tech* 28 (2013) 045007
8. T. Fujihira, *Jpn. J.Appl. Phys.*, 36, no. 10 (1997) 6254
9. <http://www.srim.org/>
10. G. Lulli, *IEEE Trans. Electron Devices*, 58, (2011) 190
11. E. Morvan et al., *Diamond and Related Materials* 8 (1999) 335
12. <http://www.cree.com/LED-Chips-and-Materials>
13. <http://www.iivibg.com/manufacturing.html>