



**HAL**  
open science

## Vertical Termination Filled with Adequate Dielectric for SiC Devices in HVDC Applications

Thi Thanh Huyen Nguyen, Mihai Lazar, Jean-Louis Augé, Hervé Morel,  
Luong Viet Phung, Dominique Planson

► **To cite this version:**

Thi Thanh Huyen Nguyen, Mihai Lazar, Jean-Louis Augé, Hervé Morel, Luong Viet Phung, et al.. Vertical Termination Filled with Adequate Dielectric for SiC Devices in HVDC Applications. Materials Science Forum, 2016, 858, pp.982-985. 10.4028/www.scientific.net/MSF.858.982 . hal-01391838

**HAL Id: hal-01391838**

**<https://hal.science/hal-01391838>**

Submitted on 6 May 2019

**HAL** is a multi-disciplinary open access archive for the deposit and dissemination of scientific research documents, whether they are published or not. The documents may come from teaching and research institutions in France or abroad, or from public or private research centers.

L'archive ouverte pluridisciplinaire **HAL**, est destinée au dépôt et à la diffusion de documents scientifiques de niveau recherche, publiés ou non, émanant des établissements d'enseignement et de recherche français ou étrangers, des laboratoires publics ou privés.

# Vertical termination filled with adequate dielectric for SiC devices in HVDC applications

Thi Thanh Huyen Nguyen <sup>1, a</sup>, Mihai Lazar <sup>1, b\*</sup>, Jean-Louis Augé <sup>1, c</sup>,  
Hervé Morel <sup>1, d</sup>, Luong Viet Phung <sup>1, e</sup>, Dominique Planson <sup>1, f</sup>

<sup>1</sup>Université de Lyon, CNRS, Laboratoire Ampère, INSA-Lyon, Université Claude Bernard Lyon 1, UMR 5005, F-69621, France

<sup>a</sup>thi-thanh-huyen.bui@insa-lyon.fr, <sup>b</sup>mihai.lazar@insa-lyon.fr, <sup>c</sup>jean-louis.auge@univ-lyon1.fr,

<sup>d</sup>herve.morel@insa-lyon.fr, <sup>e</sup>luong-viet.phung@insa-lyon.fr, <sup>f</sup>dominique.planson@insa-lyon.fr

**Keywords:** SiC, peripheral protection, high voltage.

**Abstract.** Recently, thanks to the advancement in SiC process technology, the deep trench termination (DT<sup>2</sup>) technique becomes an appropriate choice for future high voltage SiC power device. This technique termination is based on the use of a wide and deep trench, which is filled by a dielectric and associated with a field plate. DT<sup>2</sup> technique increases the breakdown voltage ( $V_{BR}$ ) to a value near to the ideal one that can be obtained in a plan case; and at the same time, reduces drastically the chip area comparing to the previous conventional techniques. In this work, the DT<sup>2</sup> used for a 3 kV 4H-SiC bipolar vertical diode is presented. Simulations using TCAD SENTAURUS software show that a maximum breakdown voltage of 3300 V at room temperature can be achieved with a deep trench of 20 $\mu$ m corresponding to 98 % of a parallel plane breakdown voltage for the drift layer of 18  $\mu$ m. Those simulations also point out the important impact on the  $V_{BR}$  of the structure of the trench; the dielectric critical electric filled ( $E_c$ ), the permittivity ( $\epsilon_r$ ) of the dielectric used, the etching defects as microtrench and fixed charges at the interfaces...of power device.

## Introduction

Due to its properties such as wide band gap, high thermal conductivity, large breakdown voltages ( $V_{BR}$ ), high saturated electron drift velocity, SiC have the ability to withstand harsh environmental changes and become an attractive material for high-power, high-temperature, high-voltage electronic device applications. However high blocking performance, which the material potentially has, can only be reached if a edge termination structure is properly designed so that the electric field crowding effect taking place at the junction edges of power device is reduced. So far, based on planar technology, numerous techniques have been adapted to improve the  $V_{BR}$ . Those techniques are numerous: guard ring [1], field plate (FP) [2], semi-insulating polycrystalline silicon (SIPOS) [3], junction termination extension (JTE) [4], 3D RESURF [5]... However for high voltage power devices, these techniques have the drawback of consuming large areas. To increase the  $V_{BR}$  up to almost the ideal value while keeping the chip area small with respect to conventional structures, a termination technique using very deep trenches for high-voltage power device was presented the first time in 1999 by D. Dragomirescu [6]. The results was validated for Silicon in simulation with POWER2D [7]. In 2003, this concept has been demonstrated experimentally in Si technology [8] for a diode of 1200 V. They also show the possibility to use the Cyclotene 4026 - 46 BCB (BenzoCycloButene) resin in thick layer to realize DT<sup>2</sup>.

Recently, several junction terminations with a deep trench have been reported [8] named as well T3 JTE [6], or deep trench junction termination (DT<sup>2</sup>) created by using inductively coupled plasma reactive ion etching (ICP-RIE) [9]. Some others studies have proposed electrical improvements. F.Baccar et al [10] studied the electrical variations after passive thermal ageing. Several degradations have been implemented in the simulated structure such as creating voids and adding traps to the interface between BCB and Si. Seto et al. [11] emphasized the clear relationship between the trench depth and the termination length for optimum design. Kamibaba et al. [12] pointed out that positive charges due to the holes accumulated in the trench side wall effectively determinate the high electric field in chip edge region, which is the key mechanism for the edge termination design with deep trench structure. All these studies demonstrated that the application of technique termination DT<sup>2</sup>

termination technique for power devices is promising. Up to now, all these researches and experimentations are applied for Silicon (Si) semiconductor materials. In this paper, we demonstrate that the DT<sup>2</sup> technique can be applied for SiC power devices by simulation using Sentaurus software first and then by experimental steps development.

## Deep Trench termination concept and simulation results

Fig.2 shows the 2D cross section structure of the 4H-SiC DT<sup>2</sup> diode. The vertical diode structure is composed by an anode based on a P<sup>+</sup> epilayer 1 μm thick, 5×10<sup>18</sup> cm<sup>-3</sup> doped on the top of the structure, a N<sup>-</sup> epilayer 18 μm thick much less doped (8×10<sup>14</sup> cm<sup>-3</sup>) and a N<sup>+</sup> substrate. The ideal breakdown voltage (V<sub>br</sub>) for one dimensional PiN diode structure with an i-layer thickness of 18 μm is 3354 V. The DT<sup>2</sup> edge termination structure is based on a large (W<sub>T</sub>) and deep trench (D<sub>T</sub>) filled by a dielectric associated to a field plate. The field plate is needed to draw out the electrostatic potential in the trench.

Sentaurus TCAD (Synopsis Inc) software is one of the most advanced tools for electronic device simulation, using physical models to describe the semiconductor material properties and solving the semiconductor equations. The device is represented as a meshed finite-element structure. Each node of the device has properties associated with it, such as material type and doping concentration. For each node, the carrier concentration, current densities, electric field, generation and recombination rates, and so on are computed.

Our challenge is to try to optimize the depth and width of the trench for obtaining a structure with the V<sub>BR</sub> as close as possible to the value of the plane structure case, and at the same time by reducing the chip area. In a first time, we do not use field plate, the trench was filled by SiO<sub>2</sub> (relative dielectric permittivity 3.9). Results presented in the Fig.1 show that by keeping the width of the trench constant at 30 μm, equipotential lines are more widely dispersed on the surface of power device with the deeper trench. The trench absorbs almost all equipotential lines, and decreases the peak field at the edge of the junction. Thus, V<sub>BR</sub> is increased. Beside, it was found that the trench width affects also V<sub>BR</sub> but to a lesser degree than the depth. We pointed out that, the innovative benefit of this technique will increase the V<sub>BR</sub> without increasing the device surface.

The trench depth versus the trench width is showed in Fig.3 with constant V<sub>BR</sub>. These curves show that the shallow trenches can reduce highly the termination length. Moreover, it is found that the trench width for each trench depth has no influence on the V<sub>BR</sub> above a threshold value. There is an optimum value of the width of the trench for each depth. For each width of the trench, the V<sub>BR</sub> increases significantly with the trench depth. The maximum breakdown voltage of termination without field plate does not exceed 2335 V, even if the trench is very large.

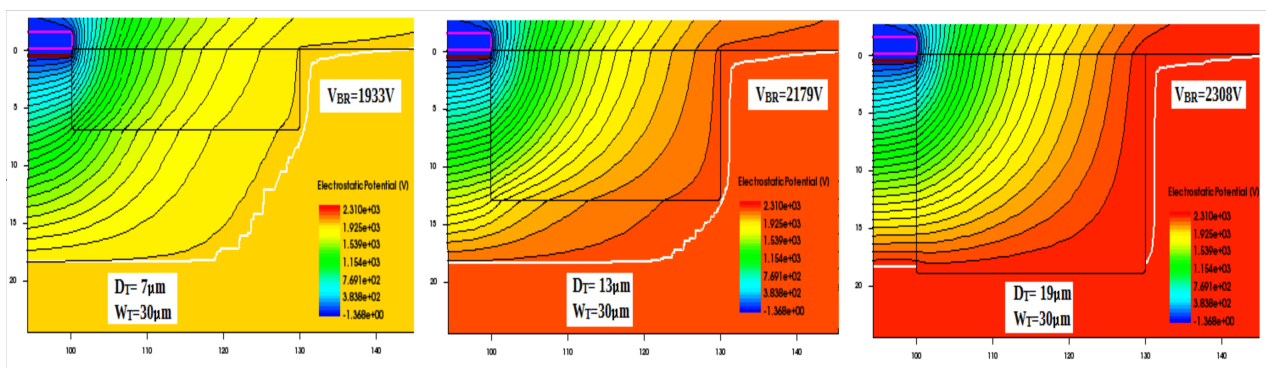
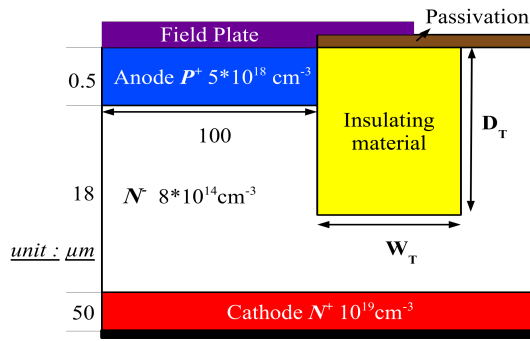
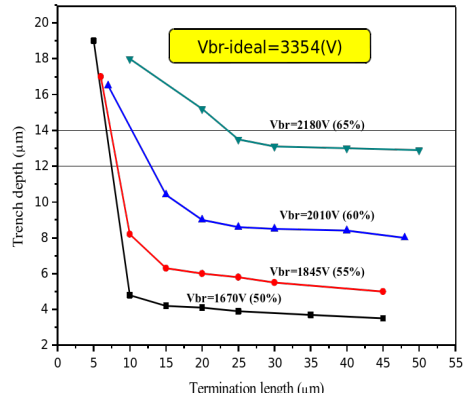


Fig. 1. Potential distribution in trenches with a constant width (W<sub>T</sub>=30 μm) and varying depth (D<sub>T</sub>) from 7 to 19 μm

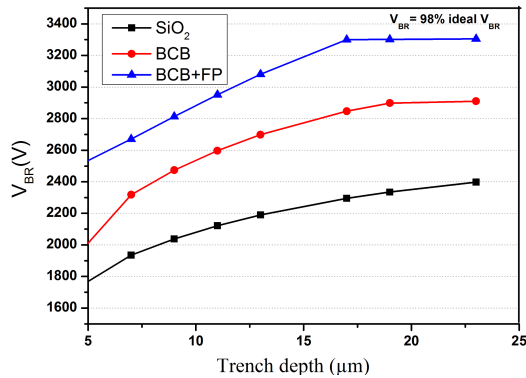


**Fig. 2.** Cross section of the schematic structure of the 4H-SiC DT<sup>2</sup> diode

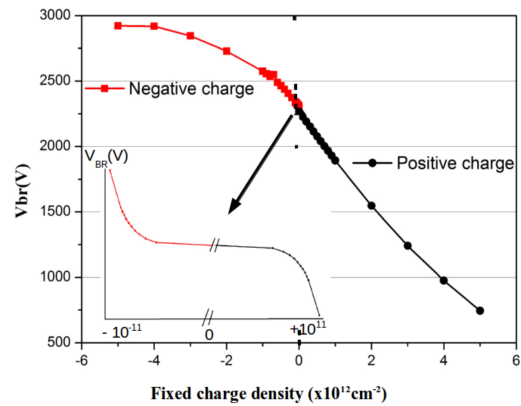


**Fig. 3.** Trench depth as a function of trench width for constant breakdown voltage

Performances of DT<sup>2</sup> depend not only on the structure of the trench and field-plate dimensions but also on the dielectric characteristics of the filling material. BenzoCycloButene (BCB) was chosen because of its good characteristics and highly ability success in filling wide and deep Si trench. BCB also have a lower dielectric permittivity value ( $\epsilon_r=2.65$ ), a higher critical electric field ( $E_c=5.3$  MV/cm) than those of silicon oxide. Fig. 4 shows the obtained  $V_{BR}$ . The surface charge density at the SiC-dielectric interface was considered negligible. BCB sustains all the equipotential lines and the field plate draw out the equipotential lines in the trench, guaranteeing a  $V_{BR}$  of the termination near the ideal value (3300 V, 98% efficiency with filed plate and 2830 V, 85% efficiency without field plate).



**Fig. 4.** Breakdown voltage as a function of trench depth, dielectric material and field plate (FP). With BCB + Field plates,  $V_{BR}$  reached 2% of the  $V_{BR}$  ideal



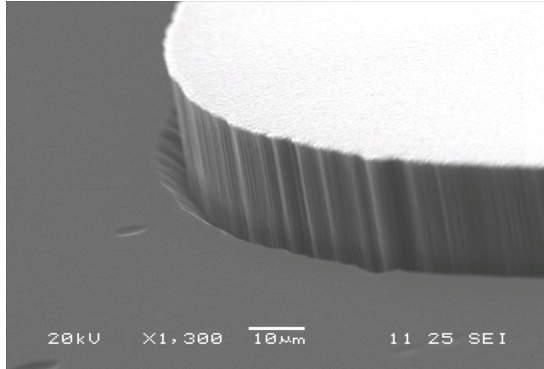
**Fig. 5.**  $V_{br}$  as a function of charge density for a structure with 7  $\mu\text{m}$  DT<sup>2</sup> depth filled with BCB

Fixed charges may appear at the SiC/BCB interfaces for many reasons as thermal variations or impacts of technological processes. Positive and negative fixed charges have been considered. The influence of these charges was studied qualitatively and quantitatively. The results shown in the Fig. 5 correspond to a 7  $\mu\text{m}$  SiC depth trench filled with BCB. For positive or negative charge densities below  $10^{11}$   $\text{cm}^{-2}$ , the  $V_{BR}$  is not changed (see the inset in the Fig. 5 which details the  $V_{BR}$  for this range of charge densities). For negative charge density below  $-10^{11}$   $\text{cm}^{-2}$ , the  $V_{BR}$  increases rapidly and for positive charges density higher  $10^{11}$   $\text{cm}^{-2}$  the  $V_{BR}$  decreases also quickly. This  $V_{BR}$  behavior is correlated with a shift of the boundaries of the space charge region by increasing or decreasing the distance between the equipotential lines.

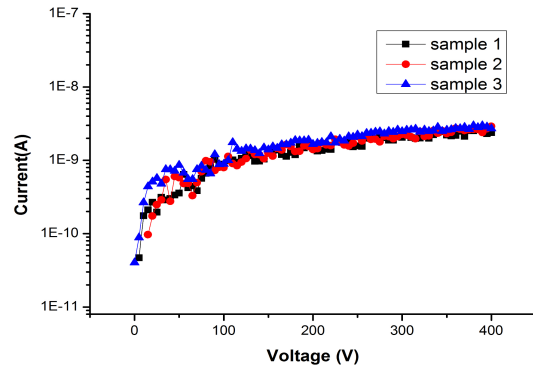
## Experimental

In order to validate the DT<sup>2</sup> method for 4H-SiC vertical power devices, experiments were done to create the trench on the 4H-SiC material by ICP and RIE techniques.  $\text{SF}_6$  and  $\text{SF}_6/\text{O}_2$  plasma chemistries have been used, protecting the unetched surface with a hard Ni-based mask. The obtained results show that more than 20  $\mu\text{m}$  of depth trench could be obtained (Fig. 6). With a reasonable process duration ( $\sim 80$  min), an etching rate of  $\sim 0.22 \mu\text{m}/\text{min}$  has been used in order to obtain smooth wells. However we note the presence of microtrenches, an increasing of the etching

rate near the corners compared to the center of the trench. Technical parameters of the etching process such as power, DC bias, pressure and gas flow rate has been studied and optimized without being able to completely eliminate this phenomenon. Simulation results shown that the  $V_{BR}$  is not strongly affected by these microtrenches, especially in the case that etching occurred until to the substrate (trench depth greater than the thickness of the epitaxie layer).



**Fig. 6.** SEM images of 23min SiC etch from ICP etching with optimised process parameters to obtain a maximum etch rate of 0.22  $\mu\text{m}/\text{min}$ .



**Fig. 7.** Measured I-V reverse characteristics.

After etching process, we made electric tests under air and room temperature to examine the reverse bias leakage current. The result obtained in Fig.7 showed a low reverse current around 1 nA which is an optimistic result in spite of the microtrench observed in the lower corners of the etched wells and confirming the quality of our smooth etched wells.

## Conclusion

This work points out the ability of using  $\text{DT}^2$  technique to improve the  $V_{BR}$  of 4H-SiC high-voltage power device. With the help of TCAD Sentaurus tools, it has been demonstrated that  $\text{DT}^2$  technique allows to reduce the chip area comparing to the previous conventional techniques. The maximum voltage obtained was 3300 V meaning that a 98% efficiency value is reached thanks to a 19  $\mu\text{m}$  depth and 30  $\mu\text{m}$  width trench filled by BCB, and combined with filed plate. The proposed termination techniques are relatively simple to fabricate and attractive for SiC power devices junction termination. A 23  $\mu\text{m}$  depth trench was obtained by ICP technique, using  $\text{SF}_6$  plasma chemistries, protecting the unetched surface with a hard Ni-based mask. With a process duration reasonable ( $\sim 80$  min), an etching rate of  $\sim 0.22$   $\mu\text{m}/\text{min}$  smooth wells have been obtained. The leakage current range between few nano-amperes and few tens nano-amperes is very small, indicating that the parameters of the etching process are appropriate. Indeed, the etching process does not negatively affect the device operation, as the fixed charge accumulation at the surface of the trench which seems to be very small. The etching process must still be optimized to completely eliminate the micortrench phenomenon. The realization of SiC PiN diode is underway to validate this concept (including deposits of dielectric layers and planarisation techniques of structures...).

- [1] Y. C. Kao, E. D. Wolley, Proceedings of the IEEE, vol. 55, 1967.
- [2] C. B. Goud, K. N. Bhat, IEEE Trans. Electron Devices, vol. 38, pp. 1497–1504, Sept. 1991
- [3] D. Jaume, G. Charitat, J.M. Reynès, P. Rossel, IEEE Trans. Electron Devices, vol. 38, pp. 1681-1684, July 1991.
- [4] V. A. K. Temple, W. Tantraporn, IEEE Trans. Electron Devices, vol. ED-33, pp. 1601-1608, Oct. 1986.
- [5] J.A. Appels, H.M.J. Vaes, Electron Devices Meeting, Internationa, vol 25, pp. 238-241, 1979.
- [6] D.Dragomirescu, G. Charitat, F. Morancho, P. Rossel, CAS '99 Proceedings, 1999.
- [7] E. Stefanov, G. Charitat, N. Nohier, Ph. Spiesser, Materials Research Society Symposium Proceedings, pp363-368, dec 1997.
- [8] L. Théolier, H. Mahfoz-Kotb, K. Isoird, F. Morancho, Power Semiconductor Devices & IC's, ISPSD 2009. 21st International Symposium on, pp. 176 – 179.
- [9] C. Park, N. Hong, D. J. Kim, and K. Lee, Proc. ISPSD, pp. 257–260, 2002.
- [10] F. Baccar, F. Le Henaff, L. Theolier, S. Azzopardi, E. Woigard. Eurosime 2014, pp. 1–7
- [11] K. Seto, R. Kamibaba, M. Tsukuda, and I. Omura, ISPSD 2012, pp. 161–164.
- [12] R. Kamibaba, K. Takahama, and I. Omura, ISPSD 2010, pp. 107–110.