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A Novel Approach to Extract the Thyristor Design Parameters for Designing of Power Electronic Systems

Atef Jedidi, Hatem Garrab, *Member, IEEE*, Hervé Morel, *Senior Member, IEEE*, and Kamel Besbes, *Member, IEEE*

Abstract—Accurate simulation is an essential task in designing of integrated power systems to predict their electrical behavior. Thus, a very good description of their wiring circuits is required, and the availability of accurate models of power semiconductor devices and associated design parameters is crucial. This paper focuses on a novel extraction approach of design parameters for a 1-D finite-element-method model of the thyristor. These design parameters are also essential for physics-based analytical models. This paper presents an extraction procedure of the main design parameters of an ultrafast thyristor: the effective area of the device, the ambipolar lifetime, the doping concentration and width of the low-doped base region, and the doping concentration and width of the gate region. The extraction procedure of the thyristor design parameter is based on a comparative computation between simulation and experimental results, taking into account the physics of the component. Measurements are carried out on a sophisticated test circuit, which must be modeled with a sufficient accuracy. This paper details the parameter extraction procedure. Various electrothermal simulation results about the thyristor under test, using the extracted values of design parameters, show good agreement with experiment and confirm the validity of the presented extraction procedure.

Index Terms— Modeling, Finite Element Method (FEM), Thyristors, Simulation.

I. INTRODUCTION

Thyristors and gate turn-off thyristors (GTOs) continue to be used in power electronic applications particularly for high power application [1]–[6]. Thyristors are also available as new silicon carbide devices with strong capabilities [7]–[9]. However, silicon devices are further available at lower cost. Therefore, the availability of thyristor models is highly recommended for the analysis and design of power electronic systems, including thyristors and even GTO. Modeling and

simulation are an essential part of the design flow of power electronic systems. The modeling is used to consider nonmeasurable amounts of real devices, to optimize the realization cost and to increase the reliability of designed circuits. A precise description of power system behavior requires the availability of accurate component models. The validity of the semiconductor device models depends not only on semiconductor equations but also on device design parameters, i.e., the structure definition. Since it is difficult to obtain these parameters directly from the manufacturers, the extraction of these parameters may be based on reverse engineering techniques, but it remains a sensitive and a destructive task. There is therefore great interest in the development of nondestructive extraction and appropriate methods to obtain accurate models of power devices [10]–[15]. This paper describes a step-by-step extraction procedure to identify the main design parameters of a thyristor. This is a first step toward the design and optimization of power electronic systems using thyristors and GTO based on silicon or silicon carbide materials dedicated to transportation systems and power distribution and transmission of electricity.

Section II presents a state-of-the-art of the thyristor modeling and the selected modeling approach. Section III presents the model of the circuit used for the comparison between simulation and experiments. Section IV presents the extraction procedure. Section V presents some preliminary results and the analysis of the validity domain of the obtained parameters. This paper finishes by some conclusions.

II. THYRISTOR MODELING

Given the complexity of physical phenomena that governs thyristor operation, published model accuracy for such device is usually weak [16]–[20]. The SPICE model in [16] is not accurate since it does not consider the high-level injection phenomena in the thyristor epitaxial layer. Literature reports also models using lumped-charge techniques [18]–[20]. These models use localized charge method to get a pretty accurate description of the charge behavior in the component base region. These models as those based on finite-element methods (FEMs) depend on device design parameters.

The FEM is one of the most accurate approaches in power devices modeling. In this paper, the FEM is selected for thyristor modeling. The 2-D basic structure of a vertical power thyristor is presented in Fig. 1. It is based on a lightly doped N-type

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A. Jedidi, H. Garrab, and K. Besbes are with the Microelectronics and Instrumentation Laboratory (LR13ES12), Department of Physics, Science Faculty of Monastir, University of Monastir, 5000 Monastir, Tunisia (e-mail: atef_jedidi@yahoo.fr; garhat@yahoo.fr; kamel.besbes@fsm.rnu.tn).

H. Morel is with the Ampere Laboratory, University of Lyon [Institut National des Sciences Appliquées (INSA)], Centre National de la Recherche Scientifique (CNRS), 69621 Villeurbanne, France (e-mail: Herve.Morel@insa-lyon.fr).

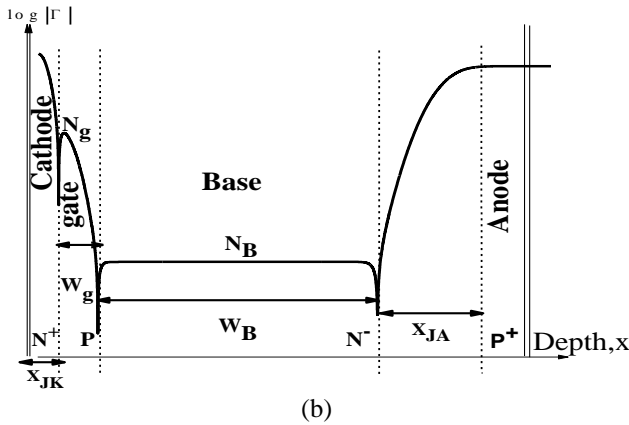
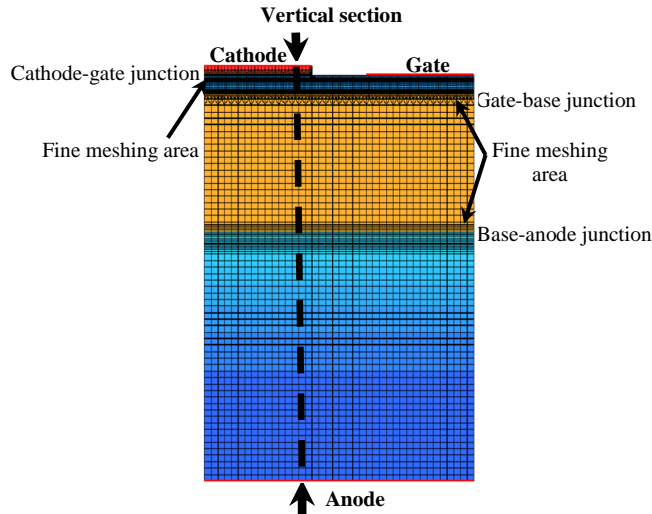


Fig. 1. Simplified 2-D architecture for the thyristor. (a) 2-D structure of a meshed thyristor. (b) Thyristor doping profile according a vertical section from cathode to anode as mentioned in (a)

TABLE I
THYRISTOR DESIGN PARAMETERS

Symbol	Definition
W_B (μm)	Width of the lightly doped base region of thyristor
N_B (cm^{-3})	Doping of the lightly doped base region of thyristor
W_g (μm)	Width of the thyristor gate region
N_g (cm^{-3})	Doping concentration of the thyristor gate region
A (mm^2)	Thyristor effective area
τ (μs)	Thyristor ambipolar lifetime
X_{JA} (μm)	Depth of the anode-base junction
X_{JK} (μm)	Depth of the cathode-gate junction
N^+ (cm^{-3})	Doping concentration of the thyristor cathode region
P^+ (cm^{-3})	Doping concentration of the thyristor anode region

layer (epitaxy or substrate), whose optimized for the blocking voltage of the device. The cathode region, the P-gate area and the anode region contacts, are respectively established on the front side and the back side of the wafer. Table I gives the list of the thyristor design parameters.

The main design parameters that characterize the arbitrary 1-D technological architecture of thyristor are shown in Fig. 1(b). Identification of the N^+ and P^+ regions is behind the scope of this paper since their impacts are of second order on the thyristor transient behavior except at very high current level where the lateral regions control the carrier injection [21].

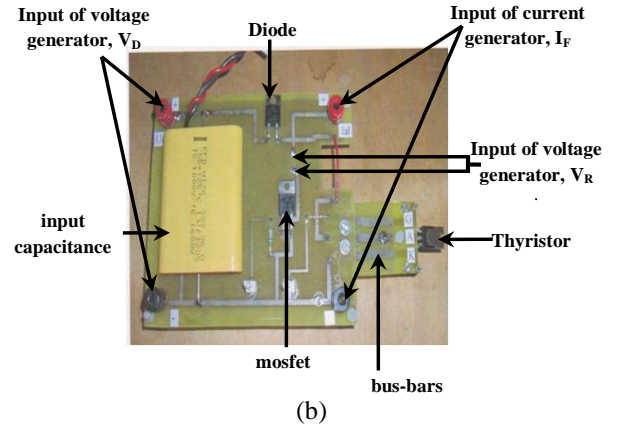
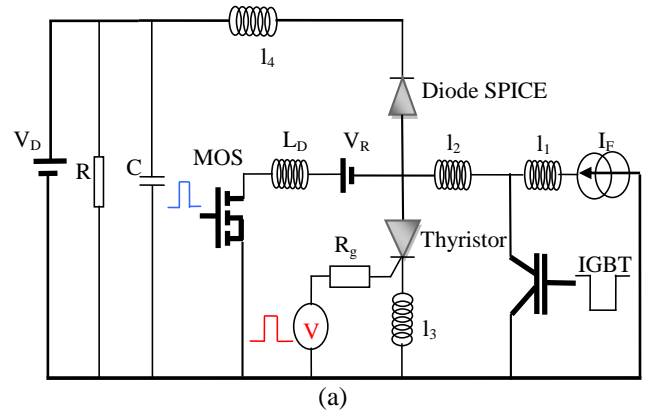


Fig. 2. Experimental circuit for the thyristor design parameter extraction. (a) Schematic. (b) Picture (IGBT transistor not included)

The secondary design parameters of thyristor X_{JA} , X_{JK} , N^+ and P^+ are set arbitrarily as follows $X_{JA} = 40 \mu\text{m}$, $X_{JK} = 2 \mu\text{m}$, $P^+ = 10^{20} \text{cm}^{-3}$ and $N^+ = 10^{20} \text{cm}^{-3}$. These values are of the same order as those of commercial device technologies.

Using the graphical tool, MDRAW-ISE TCAD [22], the thyristor 2-D architecture presented in Fig. 1(a) is implemented in FEM simulator DESSIS-ISE TCAD [23]. A meshing tool is after used to produce the necessary data such as: geometric data structure and doping profile of the component which will be used by the simulator, DESSIS-ISE TCAD. A fine meshing is performed in gate-base, cathode-gate and base-anode junctions and electrode contacts.

III. CIRCUIT MODEL

A sophisticated experimental circuit was designed to acquire the thyristor dynamic characteristics during its turn-off transient behavior, as shown in Fig. 2.

A switching cell using a MOSFET transistor and the device under test (DUT), the thyristor is implemented. In this circuit the MOSFET transistor is used to turn-off the thyristor. A current shunt in a wide bandwidth (from DC to AC 1.2 GHz) [24] is inserted in series with the thyristor. Two voltage probes, Tektronix P5100 [25], are selected. They are connected in differential manner to the thyristor to reduce the interference coming from the synchronous noise signal picked up by the probes [26]. The switching cell consists of two

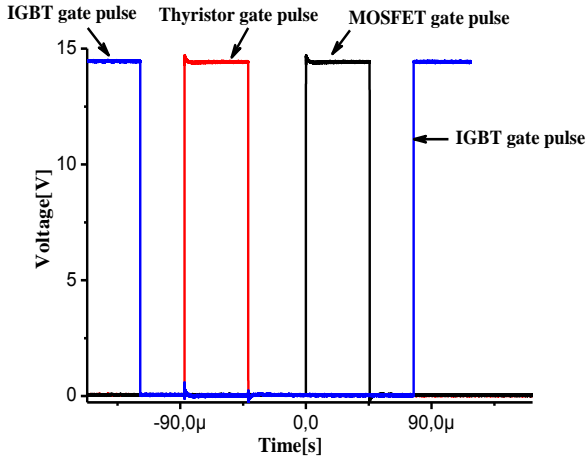


Fig. 3. Experimental control signal for IGBT, MOSFET and the thyristor gate.

voltage generators, a current generator, a MOSFET transistor, an insulated-gate bipolar transistor (IGBT), a p-i-n diode and a drive circuit, including a microcontroller delivering three synchronized pulses. These pulses are after amplified. These three obtained pulses are applied to the MOSFET transistor, the IGBT transistor and the DUT. The control timing diagram is shown in Fig. 3.

The IGBT transistor (MUP304) is turned-off only several tens of microsecond every hundreds of milliseconds and it is turned-on most of the time hence shorting the current source. The IGBT transistor enables to ensure the most part of power dissipation. Therefore, the self-heating of thyristor and MOSFET is avoided.

The experimental circuit is designed to give the best comparison condition between the measurements and the simulation obtained with the circuit model in Fig. 2. Hence, the experimental circuit includes two inductors (I_1 , air-inductor) and (I_2 , core-inductor) in series with the current source, whose purpose to stabilize its current I_F during switching. Polypropylene and ceramic capacitance is added in parallel with the voltage source to stabilize the applied voltage, V_D . The voltage source is not reversible in current, so resistance is added in parallel to the voltage generator V_D to dissipate the average energy returned to the source and allows proper regulation of the voltage source. The IGBT transistor shorts the current source when a pulse is applied to its gate and the I_F current is flowing through the IGBT. However, when the IGBT transistor is turned-off, the current flow in the PiN diode and the DUT is blocked and forward biased by the V_D voltage. Once the thyristor gate is activated, the conduction process of component is triggered. Then, a pulse is applied to the MOSFET gate that turns-on and enforces the thyristor to turn-off in a recovery process. The duration of the pulse that switches the MOSFET should be long enough to avoid immediate turn-on of the thyristor under test at reapplication of the forward voltage. This is related to the TQ of the thyristor. Once the MOSFET is turned-on, the thyristor is reverse biased by the voltage generator (V_R). Thereby, the stored charge in the thyristor base during its conduction phase will be evacuated and the reverse recovery phenomenon of thyristor starts. Experimental current and voltage waveforms

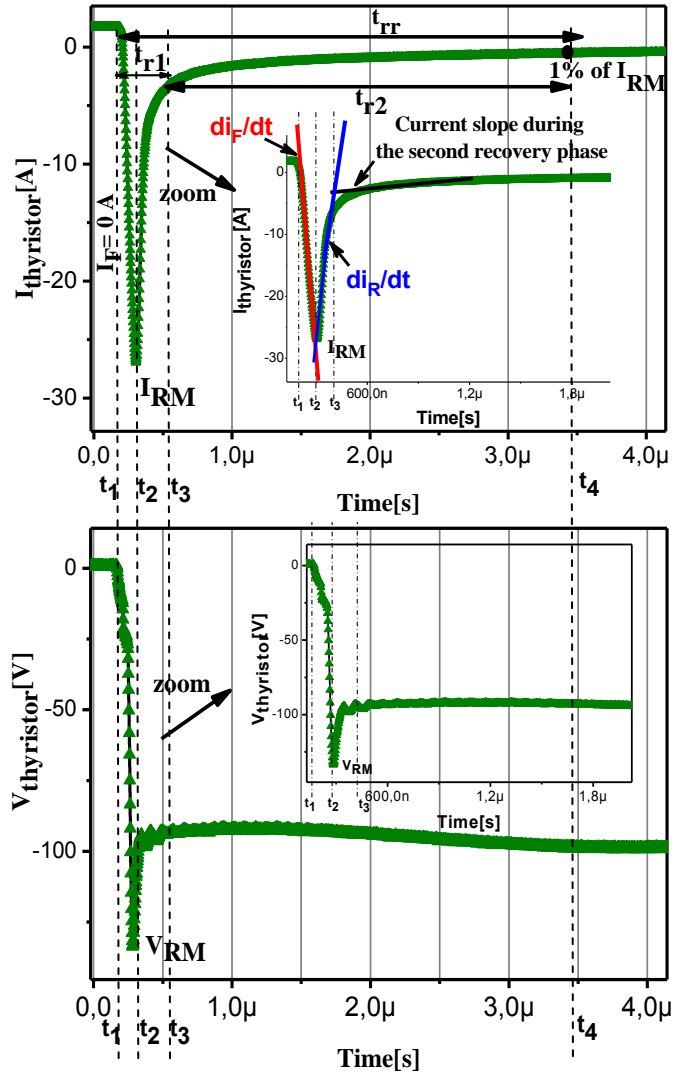


Fig. 4. Experimental current and voltage waveform across the Thyristor during its turn-off phase ($I_F = 2A$ and $V_R = 100V$)

TABLE II.
MAIN SWITCHING PARAMETERS OF THYRISTOR

Symbol	Definition
$I_{RM}(A)$	Maximum reverse current of thyristor
$V_{RM}(V)$	Maximum reverse voltage of thyristor
$t_{r1}(\mu s)$	The first recovery time associated to the stored charge recovery in the thyristor base
$t_{r2}(\mu s)$	the second reverse recovery time associated to recovery of the stored charge amount remaining in the thyristor gate and base region
$t_{rr}(\mu s) = t_{r1} + t_{r2}$	Total reverse recovery time of thyristor

across the thyristor during its turn-off phase are shown in Fig. 4. On these transient behavior characteristics, main switching parameters of thyristor are defined and they are illustrated in Table II.

Main switching parameters will be useful for the extraction procedure since they characterize the simulated and experimental waveforms of current and voltage across the component during its turn-off phase.

During the thyristor conduction phase, a high-level injection regime is established in the central region of the device. As for the p-i-n diode, the integration of continuity equations for holes and electrons gives the amount of the stored charge, i.e.,

$Q_0 = \tau \cdot I$. To turn off the thyristor, all the stored charge should be evacuated. However, during the device turn-off phase, one part of this stored charge is recombined inside the component. The remaining amount called recovery charge is evacuated due to the reverse current. The evacuation process of this recovery charge is decomposed into two parts. Initially, a portion of this charge Q_1 that has been already stored in the thyristor base region is recovered from instant t_1 to t_3 . From t_1 to t_2 , the anode current decreases according to a constant slope dI_F/dt . This slope is essentially determined by values of circuit inductors crossed by the current and value of the reverse applied voltage V_R across the thyristor. Meanwhile, from t_2 to t_3 , the anode current increases according to a constant slope dI_R/dt . For instant t_3 , as mentioned on the current waveform in Fig. 4, the current slope dI_R/dt changes suddenly in terms of value, and the current magnitude is about 10% of the maximum reverse current, I_{RM} , and the space charge region is extended on the maximal position. The remaining amount of charge Q_2 that includes charges stored in the component gate region is evacuated from instant t_3 to t_4 . At instant t_4 , the current magnitude through the thyristor is about 1% of I_{RM} .

In this paper, the developed test circuit has been implemented in DESSIS-ISE TCAD simulator using the mixed-mode simulation. Indeed, a FEM modeling is selected for the thyristor under test. The other components of the test circuit are described by their equivalent circuit models.

The Bennettwilson model [27] and the Philips unified mobility model proposed by Klassen *et al.* [28] are selected for the effective intrinsic density and the bulk mobility, respectively, in the FEM modeling of the thyristor. Temperature dependence is taken into account for the Shokley–Read–Hall lifetimes [29]. In addition, Auger recombination and the avalanche effects are considered. The temperature dependence of the lattice mobility is implemented as in [30]. The carrier intrinsic concentration follows the well-known temperature dependence, as detailed in [31]. The latter options are suitable for simulation of power semiconductor devices [32]. They are not discussed since these issues are behind the scope of this paper.

An advanced MOS2KP model for “IRF740” MOSFET developed in the literature [33] has been accounted in the test circuit modeling, instead of using the classical SPICE Level-3 model due to its poor accuracy. The switching cell is simulated, taking into account the self-inductances and mutual inductances of the layout, as shown in Fig. 5. An inductance matrix describing the wiring parasitic model of the experimental circuit has been identified using the INCA software [34]. This platform uses the partial element equivalent circuit method [35].

A cable model developed in [36], taking into account the propagating effect, is considered for the connection between the shunt and the oscilloscope during the simulation. To avoid any other types of error sources that can introduce delay and distortions for measured signals, the shunt and probe models described in [36] are also considered in this paper.

IV. EXTRACTION PROCEDURE

Commercial systems such Integrated Circuit Characterization and Analysis Program (IC-CAP) [37], [38], do not propose

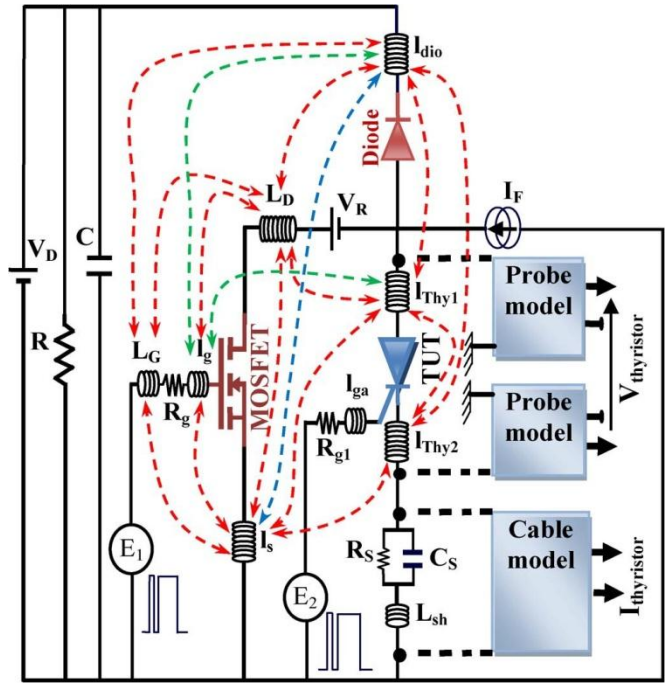


Fig. 5. Circuit model including a parasitic wiring model and probe models.

solutions for the thyristor. Moreover the high-level injection, the dynamic avalanche [39], [40] and the Kirk effect [41] have to be considered. In [42], global optimization algorithms are used to minimize a cost function which is a comparison criterion between measurements and associated simulations during turn-off transient behavior of devices. Since all parameters are coupled together, the proposed technique remains heavy, since it requires hundreds or thousands of simulations and therefore several days of computing time. In this paper, a novel approach based on physics of thyristor component to extract its design parameters is detailed. Indeed, after having characterized some commercial thyristors, an extraction procedure based on a concept of decoupling of their design parameters is described. A step-by-step extraction procedure dedicated for the thyristor device is shown in Fig. 6. The extraction procedure should be performed for thyristor under test, once that an accurate model of the experimental circuit is established.

Step #1 gives the initial values of the width W_B and the doping concentration N_B of the thyristor base region and the width W_g and the doping concentration N_g of its gate region and the effective area A . Step #2 is dedicated to refine the basic parameters N_B and W_B . Step #3 estimates the value of the ambipolar lifetime in the thyristor base region from current waveform during the component turn-off phase. Step #4 is devoted to estimate the value of the doping concentration N_g and the width W_g of the gate region during the device turn-off transient behavior. Step #5 refines the device effective area.

A. Step #1: Initialization of W_B , N_B , W_g , N_g and A

Device engineers are making tradeoffs to best meet the constraint on breakdown voltages, fast switching, low forward voltages and high forward current densities.

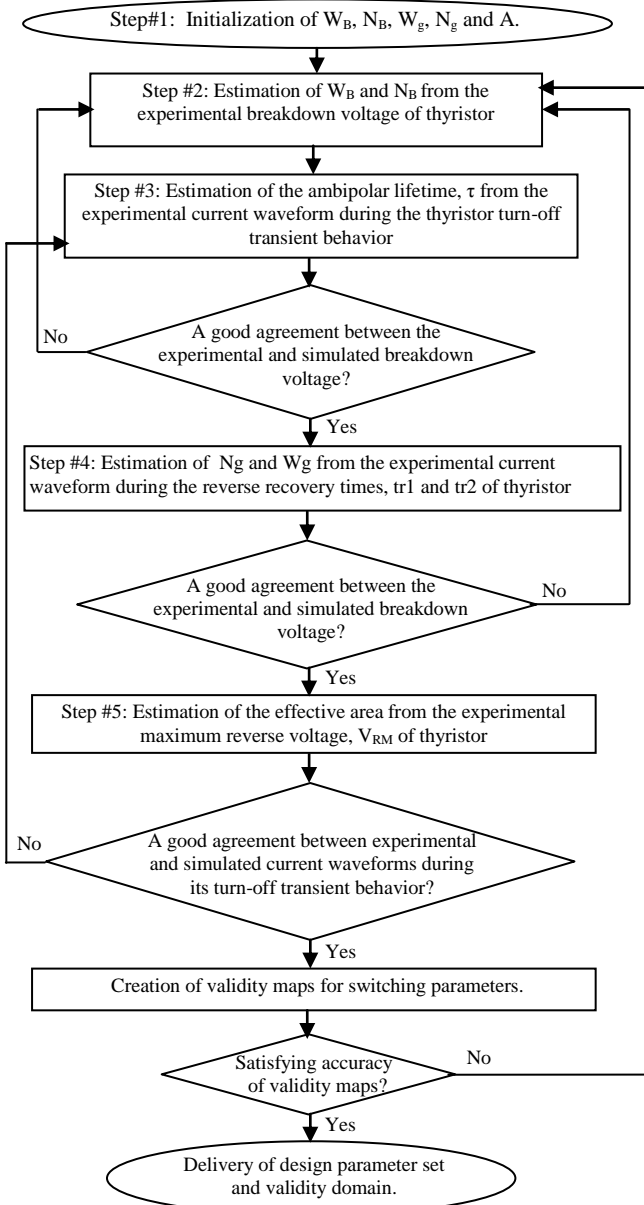


Fig. 6. Extraction procedure algorithm.

The breakdown voltage is related to N_B and W_B of the lightly doped region of the device [37] where the electric field and the space charge region will extend when the component is reverse biased. The study of edge terminations of thyristors is outside the scope of this paper, and the breakdown voltage is assumed to be mainly determined by the device volume properties. The thyristor model shown in Fig.1 is simulated in the circuit of Fig. 7 (a), for various values of N_B and W_B .

In Fig. 7 (b), it is noted that the device breakdown voltage increases as the doping level of the lightly doped layer decreases and when its thickness increases. To optimize the resistance of the lightly doped layer, a good tradeoff between a low forward voltage drop and a high breakdown voltage should be found. This tradeoff corresponds to a parameter couple (W_B and N_B) located just in the knee region [31], [43], as mentioned in Fig. 7 (b).

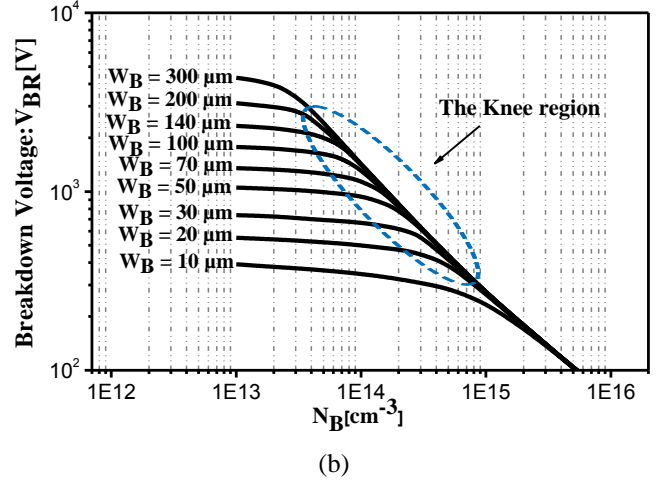
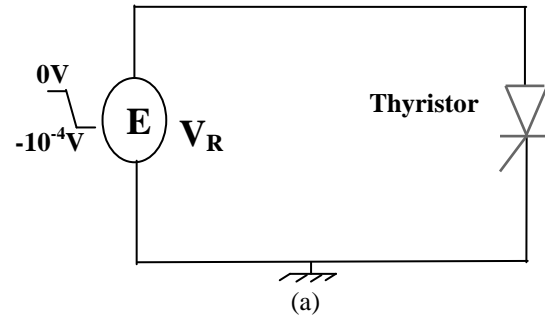


Fig.7. (a) Simulation circuit for breakdown voltage estimation. (b) Estimation breakdown voltage using simplified 2-D model in Fig.1

For setting the W_B and N_B parameters, the smallest thickness and the highest doping of the thyristor base region in the knee region are selected. From a visual inspection, initial values of W_B and N_B are selected. The estimation of the initial value of the effective area of the component can be deduced from the current density usually given by the manufacturer according to the law given by $A_{op} = I_F / J_N$, where J_N is the typical density of current (from 100 to 300 A/cm²) and A_{op} is the optimal effective area of the device.

For initialization of parameter values of the thyristor gate layer, W_g is set to a smaller value than W_B and N_g is set to a higher value than N_B .

B. Step #2: First Refinement of W_B and N_B

The refinement of these two parameters is performed by matching experimental and simulated reverse static characteristics. Using a Tektronix 371A high-power curve tracer, experimental I - V curves of thyristors under test are acquired. The simulation results are obtained through numerical simulation using DESSIS-ISE TCAD simulator in quasi-stationary mode. After having initiated a series of simulation by varying the W_B and N_B parameter values, a good agreement is obtained between the experimental and simulated waveforms of the breakdown voltages of three commercial thyristors 2N6508G, 2N6397G and BT153 as illustrated in Fig. 8(b). The estimated parameters for each component are given in Fig. 8(a).

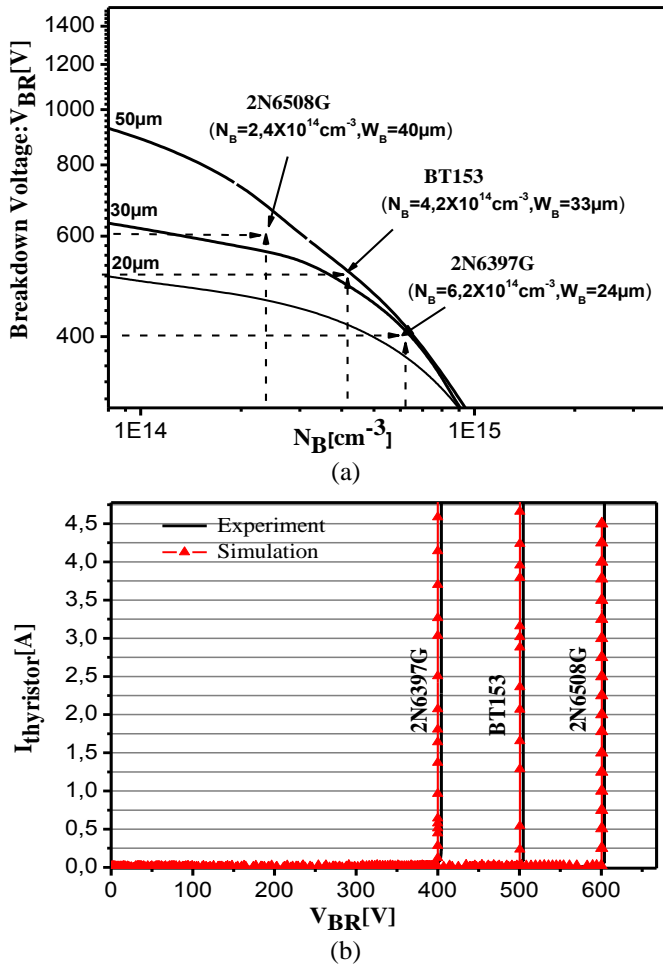


Fig.8 . Refinement of W_B and N_B based on reverse-bias I-V curve. (a) Refined values of W_B and N_B . (b) Simulated and experimental breakdown voltage for three commercial devices.

C. Step #3: Estimation of τ and refinement of W_B and N_B

First, the ambipolar lifetime is a fundamental parameter for industry of power semiconductor devices. This parameter significantly affects the direct and transient behavior of power devices and, in particular, their switching speed. Device design engineering creates deep recombination centers by instance by diffusion of heavy metals (Au or Pt) in the lightly doped region, to optimize and to control the ambipolar lifetime [44]. During turn-off transient behavior of the thyristor, stored charge in the lightly doped region, while the component is turned on, is evacuated. This amount of stored charge in the base and gate regions is related to the ambipolar lifetime. Several simulations are performed to predict the influence of the ambipolar lifetime variation on current and voltage waveforms during the thyristor turn-off switching. It is noted that the switching parameters I_{RM} and the reverse recovery time t_{rr} and, in particular, the first reverse recovery time t_{r1} are very sensitive to change of the ambipolar lifetime. Hence, by varying the ambipolar lifetime value, its estimation is obtained by matching simulated and experimental current waveforms, during turn-off transient behavior of the thyristor, and using the DESSIS-ISE TCAD simulator. For this estimated parameter, practically the same value of reverse current, I_{RM} and reverse recovery time, t_{r1} is obtained for simulated and experimental current waveforms.

Since they are also related to the stored charge during the component turn-on state, N_B and W_B should be adjusted again. Step#2 is repeated for the sake of coherence with the latest parameter estimated of τ and the breakdown voltage of the component is respected.

D. Step #4: Estimation of W_g and N_g of the gate region

Several simulations using the DESSIS-ISE TCAD simulator are performed to observe the influence of width of the gate region W_g and its doping concentration N_g on current and voltage waveforms during the thyristor turn-off phase. Influence of these two parameters occurs during the second phase of evacuation of the remaining amount of stored charge in the thyristor gate region. A change of N_g value has a remarkable influence first on the second recovery time t_{r2} and second on the current magnitude through the thyristor at instant t_3 , as mentioned in Fig. 4. However, a variation of W_g affects the reverse recovery time t_{r2} , while keeping practically the same current amplitude for the instant t_3 . The estimation of the value of doping concentration N_g is obtained by matching the simulated and experimental value of the anode current magnitude at instant t_3 . Afterward, W_g is varied until matching the experimental and simulated value of t_{r2} . For these later estimated parameters W_g and N_g , a good agreement is found between experimental and simulated current waveforms during the thyristor turn-off transient behavior. For this later estimated doping concentration N_g , the anode current magnitude for instant t_3 corresponds practically to 10% of I_{RM} . The N_B and W_B settings must be adjusted again, since they are related to the stored charge. Step #2 should be started again to have a good agreement between the simulated and experimental current waveforms and the same breakdown voltage of the thyristor under test in simulation and experiment. Step #3 should be also repeated by the way since the ambipolar lifetime is also related to the stored charge.

E. Step #5: Estimation of the effective area, A

At the end of the thyristor reverse recovery, the turn-off experimental voltage waveform presents oscillations due to interactions between the silicon-controlled rectifier extended across anode–base and cathode–gate junctions and the external circuit. During the recovery process, the variation of the device effective area has, therefore, a great effect, particularly on the magnitude of the first oscillation of the voltage waveform, corresponding to the maximum reverse voltage V_{RM} . Thus, estimation of the thyristor effective area A is obtained by matching the simulated and experimental value of V_{RM} . This latter estimated value of A corresponds to a good agreement between simulated and experimental voltage waveforms across the component during its turn-off switching. Since the stored charge inside the lightly doped region of the thyristor, when it is turned on, is also related to its effective area, the optimization of the ambipolar lifetime procedure must be restarted again with the estimated value of the effective area. Therefore, the optimization step of N_B and W_B values must be performed again to

TABLE III.
COMPARISON OF SWITCHING PARAMETER VALUES
FOR A 2N6508G THYRISTOR

	Simulation	Experiment	Error
$I_{RM}(A)$	-33	-32,6	1,2%
$V_{RM}(V)$	-108	-111,5	3,1%
$t_{rr}(\mu s)$	5,4	5,32	1,3%

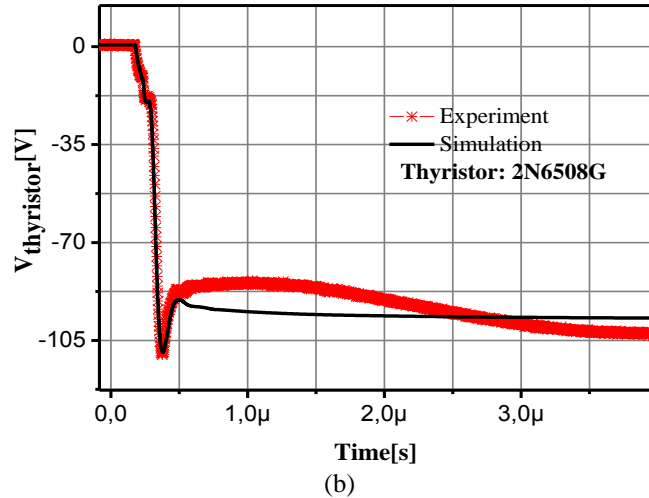
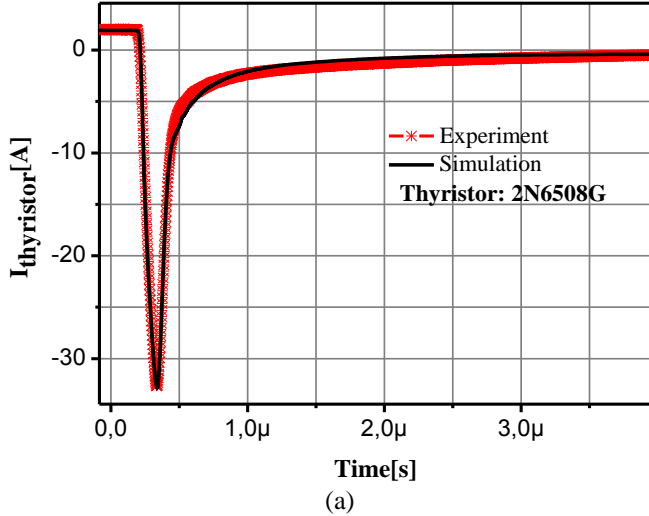


Fig. 9. Comparison of experimental and simulation results. (a) Current waveforms. (b) Voltage waveforms.

respect the measured breakdown voltage of the thyristor under test. Steps #2 and #3 are also repeated.

The step-by-step extraction procedure is adopted and performed for three commercial thyristors under test. Table III reports the experimental and simulated values of the main switching parameters I_{RM} , V_{RM} , and t_{rr} of the 2N6508G thyristor for the following operation conditions: $I_F = 2$ A and $V_R = 100$ V.

A good agreement is observed between experimental and simulated waveforms, as shown in Fig. 9. This agreement is slightly degraded after the high dv/dt and before steady state. Indeed, some oscillations appear in the experimental voltage waveform during this slot time. This disagreement may be due to inaccuracy in the representation of inductive and capacitive parasitic elements and inaccuracy of the component geometry. The 3-D effect not supported in our work for the FEM modeling of the thyristor could be also a cause of this disagreement. This

TABLE IV.
OPTIMAL DESIGN PARAMETER SET
FOR THREE COMMERCIAL THYRISTORS

Thyristor	2N6508G	2N6397G	BT153
N_B (cm ⁻³)	$2,3 \cdot 10^{14}$	$6 \cdot 10^{14}$	$4 \cdot 10^{14}$
W_B (μm)	41	23	32
N_g (cm ⁻³)	$1,95 \cdot 10^{17}$	$1,15 \cdot 10^{17}$	$1,4 \cdot 10^{17}$
W_g (μm)	4,2	6	5
A (mm ²)	35	28	33,6
τ (μs)	9	5	8

disagreement has no important effects on the extracted design parameters.

Extracted design parameters for three commercial thyristors under test are shown in Table IV.

To additionally validate the extracted effective area of the thyristor under test, its current density $J = I_N / A$ is computed, where I_N is its nominal current, and A is its effective area. For example, for the 2N6397G thyristor, $J = 5$ A/28 mm² = 178.6 A/cm². This value is in good agreement with the typical value mentioned previously (100 A/cm² < J_N < 300 A/cm²). Therefore, the effective area of the component fits well with its physical size.

V. VALIDITY DOMAIN

The validity of extracted design parameters of the thyristor under test is examined by an electrothermal simulation study. Indeed, a comparative study is performed between experimental and simulated waveforms of current and voltage across the device 2N6397G for high operating temperatures. Inside the switching cell circuit, the thyristor operating temperature is controlled by an air flow using a thermal stream system model TP041AH, where the temperature is monitored by a thermocouple and controlled by a microprocessor that regulates the air stream temperature with high stability and accuracy. Fig. 10 pictures experimental current and voltage waveforms for various operating temperatures. From this figure, it is noted that the switching parameters I_{RM} and t_{rr} increase with the thyristor operating temperature, while V_{RM} decreases with T_O . To compare these experimental data to simulation results, the electrothermal simulation mode is selected for thyristor modeling using the DESSIS-ISE TCAD simulator, taking into account their extracted design parameters. An excellent agreement is obtained between experimental and simulated current and voltage waveforms for various operating temperatures during the thyristor turn-off transient behavior, as shown in Fig. 10.

The extracted design parameters of 2N6397G, 2N6508G, and BT153 devices shown in Table II are used in the electrothermal simulation. To compare the experimental data to simulation results for these three commercial thyristors, the simulated and experimental values of the main switching parameters are selected to be compared since they characterize the turn-off waveforms. Fig. 11 compares several simulation and experimental results about the main switching parameters for the three commercial thyristors. A good agreement is found between simulated and experimental results since error between them is less than 2%.

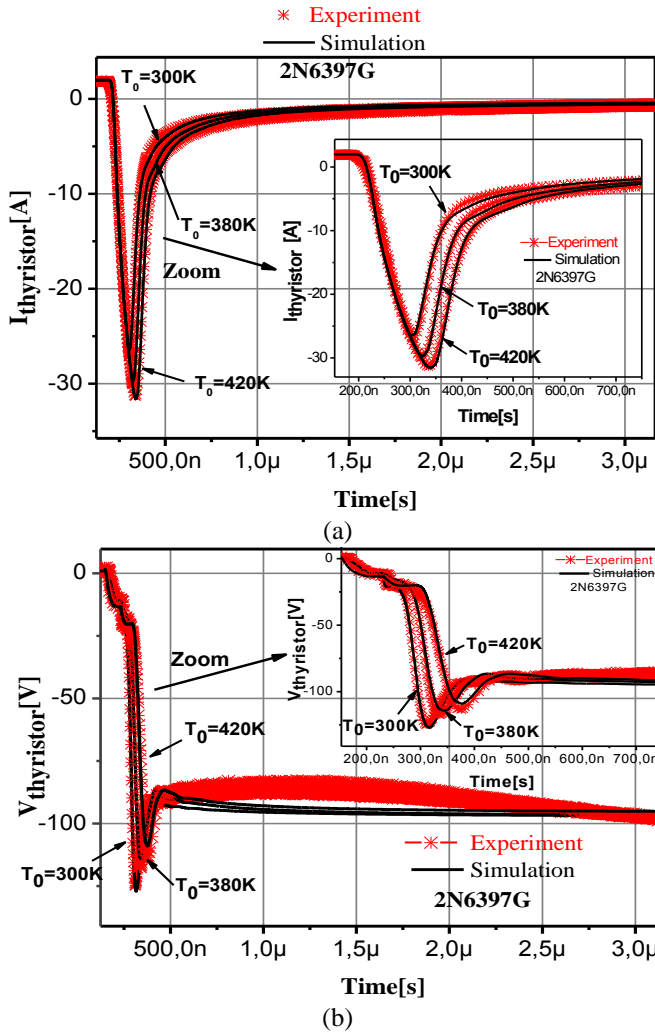


Fig. 10. Comparison of experimental and simulation results at various operating temperatures. (a) Current waveforms. (b) Voltage waveforms.

All extracted design parameters of various thyristors under test are mainly deduced from current and voltage waveforms across components during their turn-off transient behavior for operating conditions ($I_F = 2 A$ and $V_R = 100 V$). To further highlight validity of extracted design parameters, a comparative study between experimental and simulated switching parameter values versus I_F current and V_R voltage should be established. The error evolution between simulated and experimental value of t_{tr} , V_{RM} and I_{RM} parameters versus I_F current and V_R voltage are dressed in maps on Fig. 12.

Thereby the validity maps of thyristor model including extracted parameters could be discussed. An error less than 6.8 % is observed in the V_{RM} validity map. However t_{tr} and I_{RM} validity maps indicate an error less than 4.8%.

Validity maps of V_{RM} , I_{RM} and t_{tr} demonstrates the validity of the extraction procedure and the extracted design parameters of thyristor under test since the error rate between simulated and experimental values of switching parameters remain acceptable. Some perturbations of measurement are found for high current, I_F and for high voltage V_R . These perturbations constitutes the technical limitations of the work bench which explain why the I_F current and the V_R voltage did not exceed respectively 5A and 200V in the validity maps. These technical limitations do not prevent the extraction of the thyristor design parameters.

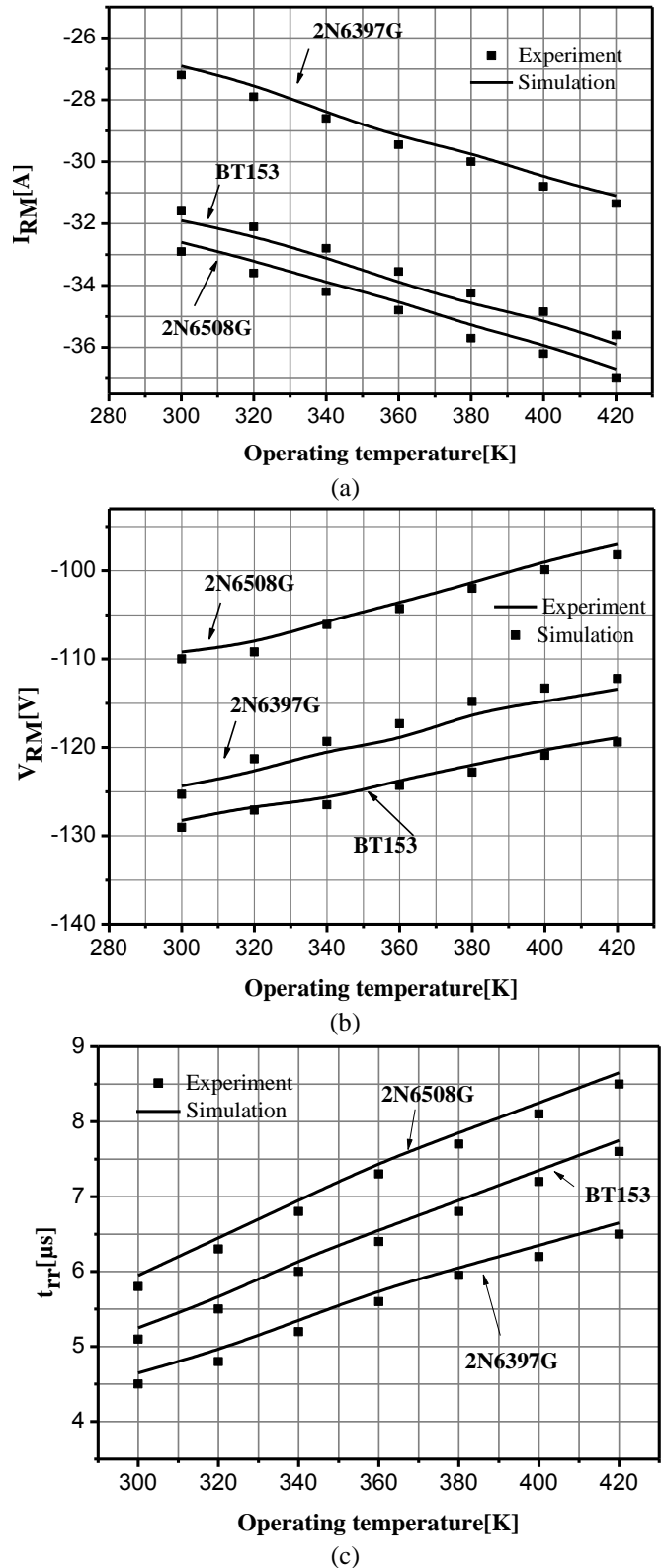


Fig. 11. Experimental and simulated of main switching parameters versus the operating temperature for three commercial thyristors: (a) I_{RM} , (b) V_{RM} and (c) t_{tr} .

VI. CONCLUSION

We have shown that it is possible to accurately extract the main design parameters of thyristor, using a novel approach based on concept of decoupling of their design parameters, taking into account the physics of the component. On the one

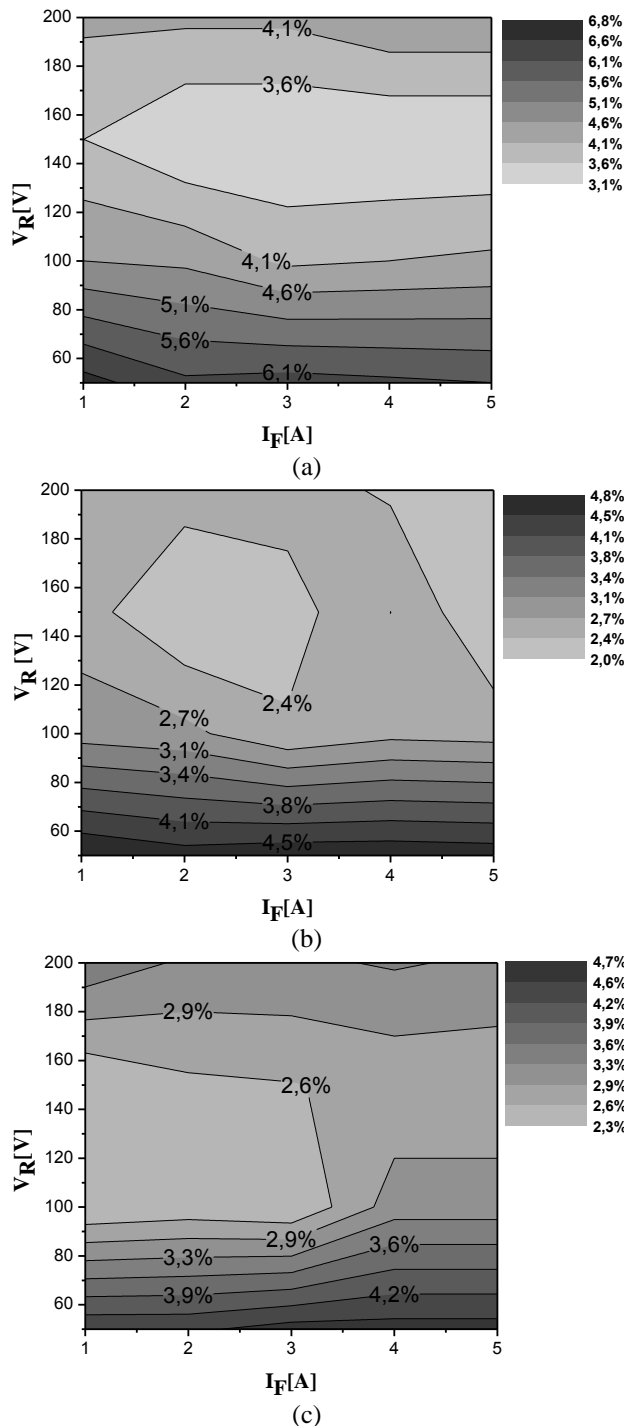


Fig. 12. Validity maps of switching parameters for the device 2N6508G. (a) V_{RM} , (b) t_{tr} and (c) I_{RM} .

a sophisticated switching cell circuit is required to acquire measurements. On the other hand, the simulation requires an accurate model of the switching cell wiring and models for the current and voltage probes. A step-by-step extraction procedure of thyristor design parameters is developed and appears as a 5-step procedure repeated until satisfying accuracy. The design parameters of three commercial thyristors are extracted. To evaluate the efficiency of the extraction procedure, an electro-thermal study of these thyristors is performed and excellent agreements between experimental and simulated results are obtained.

Although a simplified 2-D thyristor design model has been considered, excellent results have been detected in the validity range of the estimated parameters. This extraction procedure of thyristor design parameters appears also very fast since it is not expensive from the CPU-cost point-of-view. It only requires few loops. Finally, such results show that it is possible to perform very accurate simulations of a complete circuit using FEM simulations. This is a starting point for developing accurate analytical models of thyristor, which will be useful in CAD of power electronic systems including thyristors even GTO. Moreover the paper should serve as a reference for the extraction procedure even for future analytical models. The methodology of the developed extraction procedure is dedicated to silicon and silicon carbide thyristor. The next step will be to apply the extraction procedure to SiC-thyristors.

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Atef Jedidi was born in Mulhouse, France, on juillet 11, 1980. He received the M.S. and the Master degrees from the Faculty of Sciences of Monastir, Monastir, Tunisia, in 2006 and 2008, respectively. His current research interests are characterization and modeling of power semiconductor devices and the electrothermal modelization.



Hatem Garrab (M'13) was born in Jemmel, Tunisia, on Avril 05, 1973. He received the M.S. and the Diplome des Etudes Approfondies (DEA) degrees from the Faculty of Sciences of Monastir, Monastir, Tunisia, in 1995 and 1997, respectively, and the Ph.D. degree from the Institut National des Sciences Appliquées (INSA), Lyon, France, in 2003.

In 2003, he joined the University of Sousse as an assistant Professor in Electronics and microelectronics in the Institut Supérieur des Sciences Appliquées et de technologies de Sousse, Sousse, Tunisia. His research interests include power semiconductor device modeling and characterization and multi-physics modeling based on bond graphs.



Hervé Morel (M'00–SM'07) was born in Reims, France in 1959. He received the Engineer and PhD degrees from Ecole Centrale de Lyon in 1982 and 1984 respectively.

In 1985, he joined the CNRS as Associated Scientist. He is currently a CNRS Senior Scientist at the INSA Lyon, Ampere Lab. From 2012 to 2014, he was a program officer at the ANR, the French research founding agency (Renewable generation and management of electricity). He published more than 90 articles in referred journals.

His research area includes power semiconductor device characterization and modeling, CAE of Power Electronic System Integration, multi-physics modeling based on bond graphs. He is particularly involved in the design of high temperature power electronics for the More Electric Aircraft, and high voltage power electronics for the electric grids.



Kamel Besbes (M¹³) born in 1960 in Monastir, Tunisia, received M.S. degree from the Ecole Centrale de Lyon-France in 1986, the PhD degree from INSA Lyon, France in 1989 and the “State Doctorate Degree” from the Faculty of Sciences of Tunis-Tunisia in 1995.

In 1989, he joined the University of Monastir. He established teaching and research laboratories in microelectronics since 1990. Research efforts are focused on microelectronics from devices to embedded systems and Instrumentation for detection, navigation and nano-satellite programs.

He has 140, published and presented papers at workshops and conferences. He participated to committees of several workshops and conferences as IC-Microelectronics since 1992 and Smart-Systems & Devices since 2001.

He was the Vice-Dean (2000-2005) and the Dean of Sciences Faculty of Monastir (2008-2011). Since 2005, he is a Member of the University council. He is now a full Professor and the head of the Microelectronics and Instrumentation Lab.