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# Optimization of VLS Growth Process for 4H-SiC P/N Junctions

Selsabil Sejil<sup>1,2 a\*</sup>, Mihai Lazar<sup>2, b</sup>, F. Cayrel<sup>3, c</sup>, Davy Carole<sup>1, d</sup>,  
Christian Brylinski<sup>1, e</sup>, Dominique Planson<sup>2, f</sup>, Gabriel Ferro<sup>1, g</sup>,  
Christophe Raynaud<sup>2, h</sup>

<sup>1)</sup> Laboratoire des Multimatériaux et Interfaces, Université de Lyon,  
Université LYON 1, CNRS, 69622 Villeurbanne, France

<sup>2)</sup> Laboratoire AMPERE, INSA Lyon, Ecole Centrale de Lyon,  
69621 Villeurbanne, France

<sup>3)</sup> Laboratoire GREMAN, pôle MTECH, Université François Rabelais, 16, rue Pierre et Marie Curie,  
B.P. 7155, F37071 Tours Cedex, France

<sup>a, \*</sup> selsabil.sejil@etu.univ-lyon1.fr, <sup>b</sup> mihai.lazar@insa-lyon.fr,  
<sup>c</sup> frederic.cayrel@univ-tours.fr, <sup>d</sup> davy.carole@univ-lyon1.fr, <sup>e</sup> christian.brylinski@univ-lyon1.fr,  
<sup>f</sup> dominique.planson@insa-lyon.fr, <sup>g</sup> gabriel.ferro@univ-lyon1.fr,  
<sup>h</sup> christophe.raynaud@insa-lyon.fr,

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**Abstract.** P/N junctions have been fabricated with N<sup>+</sup> commercial 4H-SiC substrate on which Vapor-Liquid-Solid (VLS) selective epitaxy was used to create a localized p-type doping. The influence of the carrier gas nature (argon or hydrogen) has been investigated in terms of quality of the growth morphology, deposit thickness and electrical behavior of the P/N junction. Distinct results have been observed with a clear improvement when using VLS selective epitaxy under hydrogen.

## Introduction

Along the recent years, the Vapor-Liquid-Solid (VLS) selective epitaxy [1] has been investigated as an alternative solution to ion implantation for the localized p-type doping of 4H-SiC, leading to considerable reduction of the p-type material resistivity and improvement of the ohmic contacts formed on it, reaching specific contact resistance values as low as  $1.3 \times 10^{-6} \Omega \cdot \text{cm}^2$  [2]. The next target has been to obtain reliable 4H-SiC P/N junction fabricated using this method. However, up to now, a post growth annealing at high temperature (1700°C) was required in order to obtain direct bias threshold voltages close to the desired value  $\sim 3$  V (expected for a true 4H-SiC P-N junction). Without annealing, this threshold voltage value was remaining in the 1 - 2V range [2].

The main goal of the present work has been to define growth conditions allowing the recovery of the targeted threshold voltage of 3 V without the need of high temperature annealing. Toward this aim, the influence of the chemical nature of the carrier gas (either H<sub>2</sub> or Ar) on the quality of the P<sup>+</sup> deposit and the electrical characteristics of the P/N junction was investigated.

## Experimental section

This VLS growth was performed on a N<sup>+</sup> (0001)-Si face (8° off) commercial 4H-SiC substrate. At first, bowls have been created in the SiC by plasma etching using photoresist as a mask instead of the commonly used Ni-based metal mask. This process provides several advantages such as elimination of surface pollution risk by metal residues and simplification of the mask manufacturing process. Following this process scheme, 1 μm deep vertical bowls with circular shapes and different diameters have been etched into the top surface using fluoride chemistry Inductively Coupled Plasma.

The surface of each bowl was then locally covered by Al-Si layers stack ( $\sim 2.6 \mu\text{m}$  total thickness) deposited by e-beam evaporation. It was then patterned using a combination of plasma and wet etching processes. The melting of this Al-Si stack provides the materials for the liquid phase of the VLS process. The experimental conditions for the VLS growth processes are: sample temperature of  $1100^\circ\text{C}$ , propane flow of 1 sccm,  $\text{H}_2$  or Ar carrier gas flow of 10 slm, and VLS “plateau” duration of 15 min. After the VLS sequence, the residual Al-Si alloy was wet etched using alternates of acid and basic solutions.

The thickness of the deposit was estimated by mechanical profiling across the deposited areas and occasionally confirmed by transmission electronic microscopy (TEM) cross section analyses which gave also information on the quality of the deposit. Current-voltage (I-V) measurements on P/N structures have been performed with a “Signatone S1160” probe station and a “Keithley 2410” Source Measure Unit (SMU). These measurements were done on vertical diode configuration with  $900^\circ\text{C}$  annealed Ni-based ohmic contacts made onto the back face of the sample substrates.

### Results and discussion

As a first result, dramatic differences were observed between the samples grown under Ar or  $\text{H}_2$ . Under  $\text{H}_2$ , an excellent and uniform step-bunching morphology was obtained with regular and small terraces with jagged step edges (Figure 1.a). The corresponding thickness of the  $\text{P}^+$  SiC deposit is rather thin,  $\sim 50 \text{ nm}$ , but uniform over the entire areas of deposition.

On the other hand, under Ar, the morphology is much rougher (Figure 1.b), consisting in a rather disturbed step-bunching with more irregular step edges and a high density of pits on the terraces. In this case, the corresponding thickness of the deposit is much higher  $\sim 700 \text{ nm}$  and more irregular over the deposited areas. It can reach locally values as high as  $900 \text{ nm}$ . We believe that the pits are the visible imprints of  $\text{Al}_4\text{C}_3$  parasitic inclusions because this compound gets more stable when the Si content of the liquid phase gets too low [3]. Indeed, since the amount of Si in the liquid phase is limited, the thicker the SiC growth by VLS epitaxy, the lower the quantity of Si remaining in the Al-Si liquid phase. As a result, the use of  $\text{H}_2$  instead of Ar as carrier gas seems to lead to significant improvement of the crystalline quality of the SiC deposit.

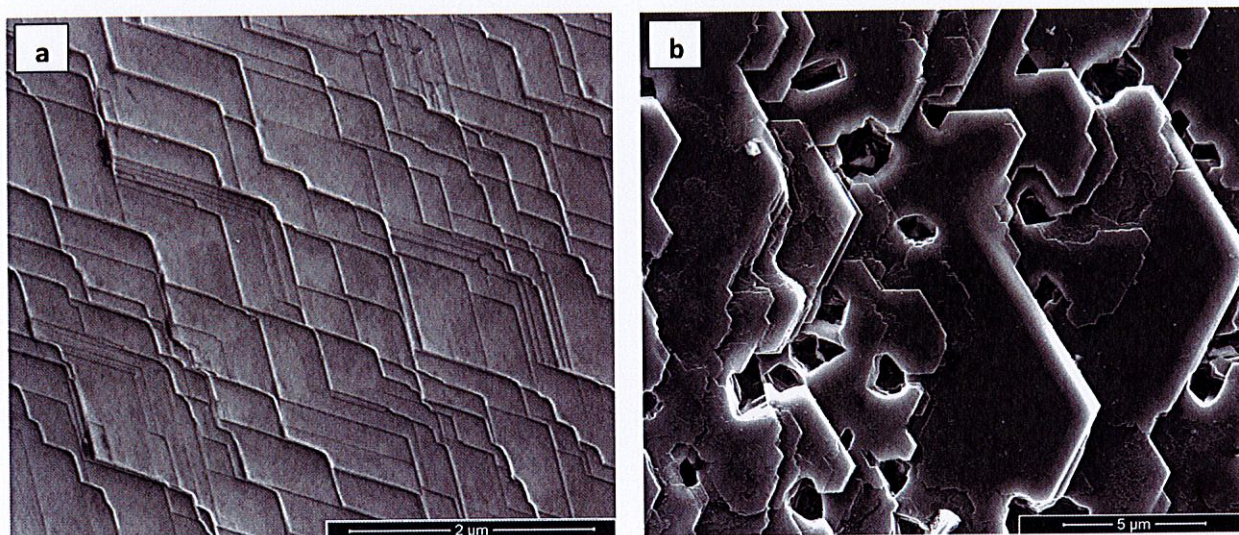


Figure 1: Surface morphology after etching of the remaining alloy on samples grown by VLS using (a)  $\text{H}_2$ , and (b) Ar as the carrier gas.

Confirmation of this improvement with  $\text{H}_2$  carrier gas was obtained from TEM characterization (Figure 2). For sample grown under  $\text{H}_2$  (Figure 2a), the deposited layer is found very thin,  $\sim 40 \text{ nm}$  thick, a value which is very close to the one estimated by surface stylus profiling. For the sample grown under Ar, the deposited thickness is confirmed to be much higher,  $\sim 600 \text{ nm}$ . In addition, a

lot of extended crystalline defects are observed in this SiC layer, defects which are hardly ever observed in the case of samples grown under H<sub>2</sub> (note that observation at higher magnification would be required to confirm this point).

As a result, both surface morphology and cross section observations show that the use of H<sub>2</sub> instead of Ar as carrier gas leads to significant improvement of the quality of the deposited 4H-SiC layer. This result may be correlated to the lower growth rate obtained under H<sub>2</sub>, which should be beneficial for high quality epitaxial growth. This significant difference in growth rate can be attributed to the H<sub>2</sub> reducing effect which can lower propane cracking efficiency on top of the liquid phase. Low growth rate can also help avoiding Al<sub>4</sub>C<sub>3</sub> parasitic growth by keeping closer to equilibrium condition.

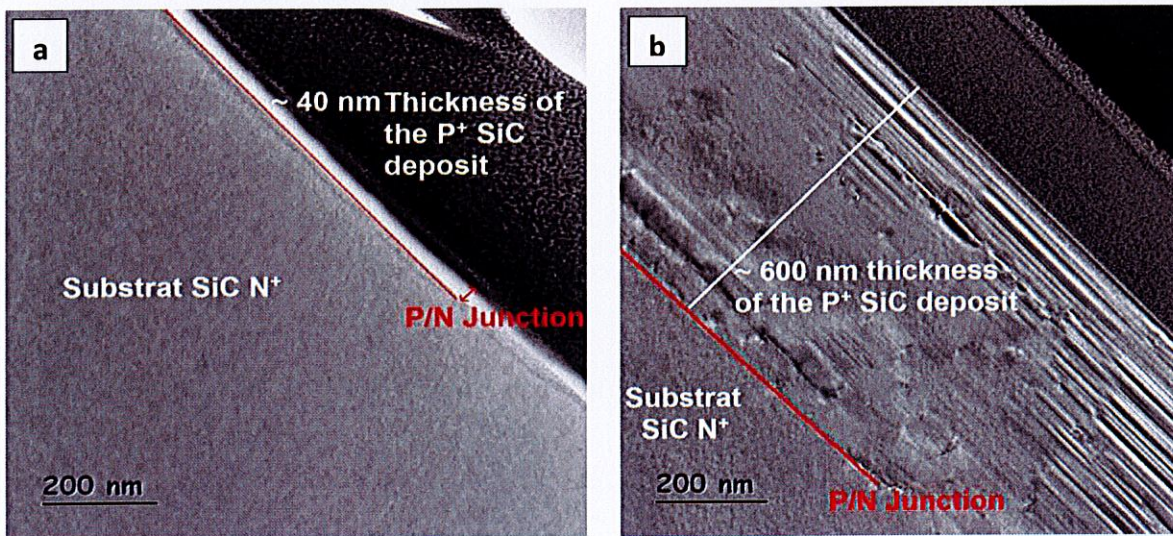


Figure 2: TEM cross section observations for samples grown by VLS with (a) H<sub>2</sub> and (b) Ar as carrier gas. In figure (a), some contrast is obtained between the N<sup>+</sup> substrate and the P<sup>+</sup> layer due to the doping type difference.

### Electrical characterization

Typical I-V characteristics measured on the VLS P/N structures are presented in Fig. 3. In direct bias, the expected threshold voltage for 4H-SiC PN junction, ~ 3 V, was only observed for the samples with P<sup>+</sup> VLS growth under hydrogen (Figure 3a). On samples with VLS growth under Ar, this threshold voltage is significantly lower, which excludes the achievement of a standard 4H-SiC PN junction. Most probably, post-VLS annealing at 1700°C should be still required to recover the expected 3V threshold value. Moreover, on samples grown under H<sub>2</sub>, higher current density can be achieved for identical voltage compared to samples grown under Ar.

Under reverse bias, several orders of magnitude improvement was also observed on the leakage current density with samples grown under H<sub>2</sub>, as compared to samples grown under Ar (Figure 3.b).

As a result, the electrical characteristics of the P/N junctions confirm the trend found previously, i.e. the H<sub>2</sub> carrier gas gives better quality junction than Ar. This is most probably due to the higher crystalline quality and better surface morphology of the deposit obtained under H<sub>2</sub>. After further optimization of the VLS growth process under H<sub>2</sub> carrier gas, thicker p-type 4H-SiC layers have been obtained, up to 500 nm, while preserving the regular step-bunching surface morphology, similar to that presented on Figure 1a.

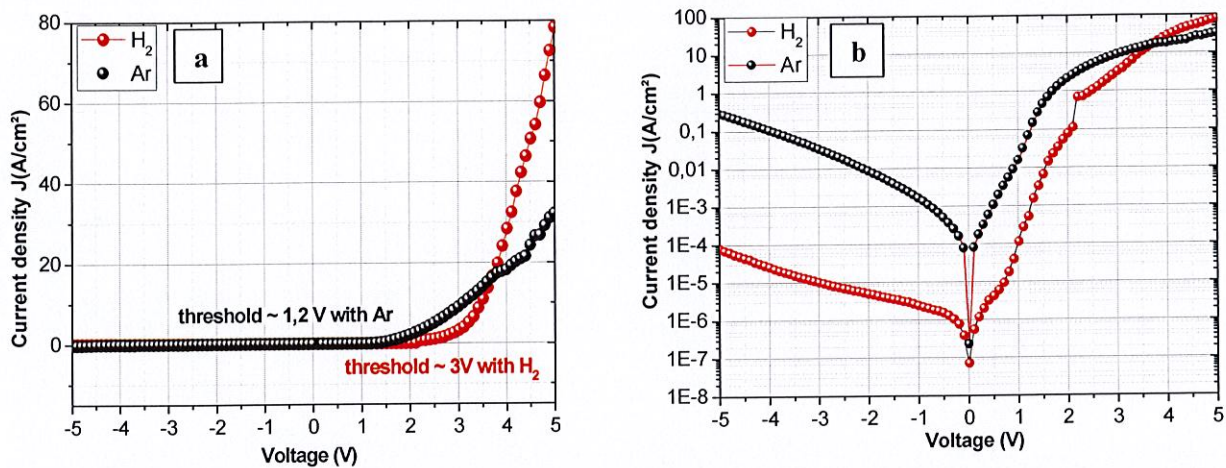


Figure 3: Current-voltage characteristics of P/N junctions fabricated with  $P^+$  zones grown by VLS under Ar or  $H_2$  carrier gas: a) linear scale for threshold voltage estimation and b) logarithm scale for leakage current comparison.

## Conclusion

By changing the carrier gas Ar by  $H_2$ , using the same experimental conditions for VLS selective epitaxy, several significant improvements were obtained in terms of surface morphology, crystalline quality and electrical behavior of the P/N junction. For VLS growth under  $H_2$  carrier gas, without any post-growth annealing at high temperature, the threshold voltage of the PN junction was  $\sim 3$  V in direct bias, which is expected for a standard P/N junction. This was also associated with a clear improvement in leakage current (without any peripheral protection or passivation). As a matter of fact, a process allowing localized epitaxy of  $P^+$  4H-SiC at  $1100^\circ\text{C}$  is now available for the fabrication of 4H-SiC PN junctions.

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