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Wide Bandgap Semiconductors for ultra high voltage devices. Design and characterization aspects

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Abstract— The development of high voltage devices is a great challenge. At least, railway and smart grids are examples of applications requiring high voltage devices. SiC power devices and technology seem to be mature enough to give a short term solution. Indeed, silicon carbide devices appear to be the semiconductor of choice for high voltage (> 6.5 kV) applications compared to Gallium Nitride. Diamond also is considered as a promising material for the next generation power devices. For high voltage devices, periphery protection is mandatory in order to reduce the well-known electric field crowding taking place at the junction edge. Some details are given about the different periphery technics (JTE, guard rings, MESA) applied to SiC and diamond devices, before combining some of them to reach higher and higher breakdown voltages. Finally, a new setup is under development in order to extract the ionization coefficients, compulsory to predict the breakdown voltage.

Keywords—component; high voltage device; silicon carbide; gallium nitride; diamond; device design; device characterization; OBIC.

1. Introduction

During the past decades, successive improvements in wide bandgap (WBG) semiconductors allowed electrical designers to consider them in power converters. Two applications will show the use of ultra high voltage devices, hence the introduction will be splitted in two parts.

A. Railway applications

Silicon components are widely used in railway traction through IGBT with different voltage ranges (1200, 1700, 3300 and 6500V) depending on the applications (Tramway, regional and high speed trains). Most of the power flows through the power devices, but auxiliary systems become more and more important (heating, air conditioning system, lighting, communication and information…) and require an increasing volume in the coach. Downsizing the volume of the converter is now possible with the use of 1200V SiC available unipolar devices (Schottky, JFETs and MOSFETs) by increasing the switching frequency, and hence decreasing the size of the passive components. These devices also allow reducing the size of the cooling system due to smaller losses and better conduction of the heat thanks to SiC.

High voltage devices (more than 10 kV) are required for power supply chain. A heavy high voltage transformer decreases the supply voltage (25 kV) down to a lower voltage to supply the 1500V DC with the help of a rectifier. This transformer is heavy (more than 10 tons) and bulky (more than 50% of the locomotive). In order to replace it, research projects aim to develop an AC/DC converter with several stages (using between 12 and 18 Si-IGBT 6.5 kV). With the use of high voltage devices, this number could be reduce by a factor of 2, allowing to split the converter in several parts and thus increasing the number of travelers in the train [1].

B. Smart Grid Applications

With the arrival of renewable energy (photovoltaic and wind turbines) and the growing energy demand, the high-voltage distribution network is changing since the beginning of 2000. The European network is interconnected and long distance exchanges of energy are now a reality [2], [3].

From the early years of the 20th century to now, the present solution uses AC high voltage. However the increasing distance (more than 100 km) make the DC high voltage more profitable from the economic point of view due to the line losses. Moreover, the DC transport requires one conductor less. In order to give some existing projects, we can mention the “NorNed” is the longest submarine power link (700 MW, 580 km, ± 450kV), the existing link between UK and Netherlands “BritNed” (1000 MW, 260 km, ± 450kV). Outside Europe, the largest HVDC transmission multi-terminal link “Biswanath-

Agra" will be built in India (6000 MW, 1825 km, 800kV) [4].

The very good yield of power electronic converters makes them attractive for DC transport of electricity. According to the prediction of major T&D actors (Alstom Grid, GE, ABB…), DC/DC converters are required with the following voltages 600kV/150kV, 150kV/50kV, 50kV/10kV and finally 10kV/500V. This is the reason for high voltage devices able to sustain at least 15 kV. Smart grid applications are one of the major issues in this field to realize AC/DC converters.

2. Requirements for ultra high voltage devices

Railway and smart grid applications require high voltage devices. Both high voltage (>10kV) and high current (>1kA) are required.

A given material ability to sustain high voltage is set by the doping concentration and the thickness of the epitaxial layer. "**Fig. 1**" exhibits the minimum thickness required to sustain a given voltage for the main WBG semiconductors. This is the theoretical value given for a 1D-layer. In order to set the doping level, and thanks to the ionization coefficients of the material, TCAD could be used to optimize the breakdown voltage. Since the data provided by **"Fig.1"** are given for a 1D-layer, a security margin must be chosen depending on the periphery protection.

According to the material and the technological means, the periphery protection must be chosen as described in Section 3.

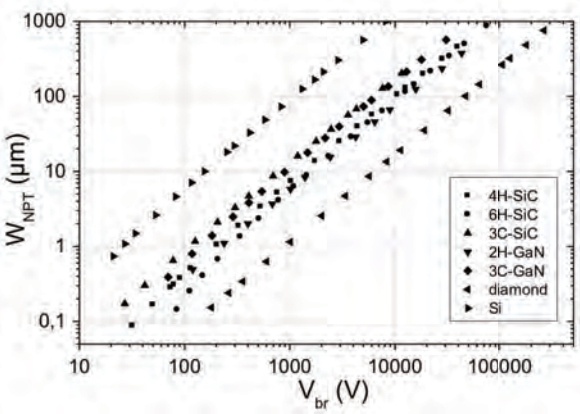

Fig. 1: Non punch through width vs. theoretical breakdown voltage for several wide band gap materials. [5]

Among WBG semiconductor materials, GaN devices breakdown voltage limitation below 1kV is related to technological issues: no p-type doping, no high quality bulk material nor thick epilayer are available. Moreover, the thermal conductivity is too low.

Concerning diamond, it is seen as the "ultimate" semiconductor. Even if high voltage diamond diodes have been demonstrated [6], the substrate size dimensions (4mm × 4mm) and the doping issues are still limiting their performances. The lack of n-type doping forces to adapt specific periphery protection, as described in the next paragraph.

Conversely, SiC has now the most advanced technological development for now, and high voltage devices have been demonstrated. The world record 27 kV (bipolar diode) using a two-zone JTE combined with JTE-rings [7] as shown in **"Fig. 8"**. An interesting result with a shorter JTE length combined with a MESA was presented in [8] for a 10 kV PiN diode.

9 kV JBS (Junction Barrier Schottky) have been achieved thanks to field rings assisted JTE. The leakage current is kept at a very satisfying level of 100 µA@10 kV [9].

All kinds of transistors have been demonstrated with breakdown voltage higher than 9 kV. While unipolar devices exhibit a large on-resistance, their switching speed is lightning fast contrary to the bipolar transistor which performances are strongly dependent on the minority carrier lifetime. Concerning unipolar switches, a 9 kV JFET, protected by MESA/JTE has been fabricated [10], but a quite high gate bias (-50 V) is necessary to block the transistor. In order to achieve high voltage and high current applications requirements, i.e. to overcome the large resistance of high voltage unipolar devices, twelve 10 kV MOSFETs have been connected in parallel with JBS diodes in the same module [11]. For bipolar devices, MESA/JTE protected BJT (Bipolar Junction Transistor) have shown a 10 kV breakdown voltage, but the current gain is limited [12]. Etched JTE has been used to protect nearly 6 kV thyristors to replace the commonly used implanted JTE [13].

Another extremely important feature of the semiconductor material is the ionization coefficients. Thanks to accurate ionization coefficients and well-designed periphery protections, device simulators are able to estimate the breakdown voltage of any structure and to help designers to gain time.

The next section will review the periphery protections technics applied to SiC diodes and transistors and diamond Schottky.

3. Different periphery technics

High voltage devices are characterized by their vertical structures where the current flows from one electrode at the top to the other one at the bottom. It allows to exploit the full thickness of the epilayer as a drift layer, which reduces the device's size compared to a lateral structure. It requires an important drift layer length with an optimal doping to match the trade-off between on-resistance and breakdown voltage.

From a device design point of view, the realization of an effective edge termination is one of the biggest challenges. Many techniques like guards rings, floating field rings, JTE… are used to make the electric field uniform at the edge of the device. In the first part of this section, different periphery protections will be reviewed shortly, then a state of the art will be presented and finally the remaining works to reach high voltage devices will be drawn.

A. Junction termination extension (JTE)

Junction Termination Extension (JTE). This protection is very often used in SiC. As shown in "**Fig. 2**", this surrounding ring is realized with aluminum or a boron implantation with a controlled dose and requires an additional mask level.

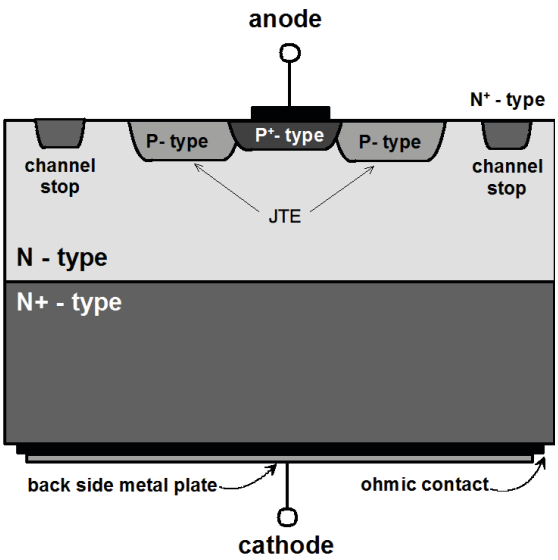

Fig. 2: Schematic view of the PiN diode with a JTE termination and a channel stop.

When the device is reverse biased, the depletion layer spreads into the JTE. Once totally depleted, the JTE becomes a highly resistive area and the electric potential is distributed over the full length of the JTE.

The total dose of the JTE must be chosen properly so that it can be totally depleted before field crowding occurs either at the JTE end or at the intersection between P+ and JTE zone. Three parameters define the JTE characteristics: first the JTE length must be optimized and then the breakdown voltage strongly depends on the JTE dose as it could be seen on "**Fig. 3**". When the dose is too high, the JTE protection has no effect and the breakdown voltage drops drastically since a strong electric field peak is located at the edge of the JTE. Such a peak is decreased with the dose decreasing. The optimal dose is reached once all the peaks have exactly the same magnitude.

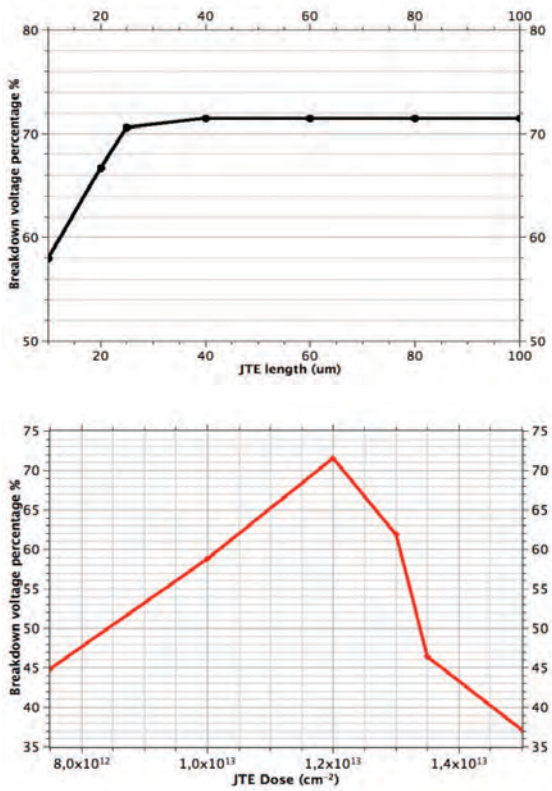

Fig. 3: Influence of the JTE length (a) and dose (b) for a PiN diode with a JTE termination. The y-axis is a percentage of the breakdown voltage (V_{br}) obtained from the ratio between the actual voltage and the ideal one.

B. Guard rings

These surrounding rings (see "**Fig. 4**") are realized in the same time as the main junction either with ion implantation or by VLS [14].

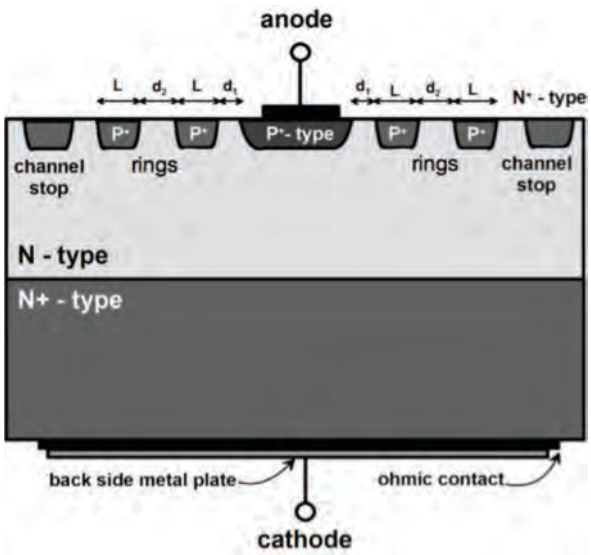

Fig. 4: Schematic view of the PiN diode with a guard rings termination

The rings act as an equipotential spreader and hence decrease the electric field. Each ring is equipotential. The parameters to be optimized are the number of rings and the distance between them.

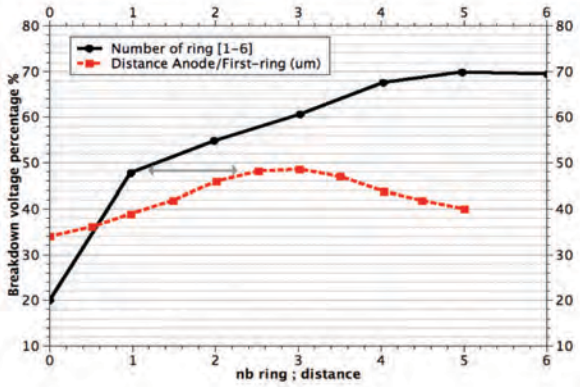

Fig. 5: Breakdown voltage percentage versus the distance between the anode and the first ring (red curve) and the optimized breakdown voltage versus the number of rings (black curve).

The breakdown voltage is very sensitive to the distance between the rings and these are getting smaller when the number is increased. Numerical simulations are mandatory to optimize the distance based on the electric field equilibrium at the border of each ring.

C. MESA/JTE combinations

An etching process is used to remove the surrounding material at the periphery of the main junction. The breakdown voltage depends strongly on the etch depth, and for the high voltage device, this technique is often combined with a JTE, and is described as MESA-JTE as shown in **"Fig. 6"**. The parameters to be optimized are the MESA etch depth, the JTE length and also the dose of the JTE.

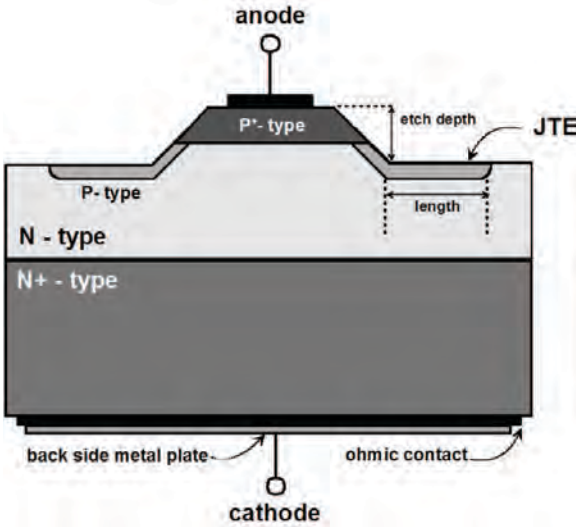

Fig. 6: Schematic view of the PiN diode with a MESA-JTE termination.

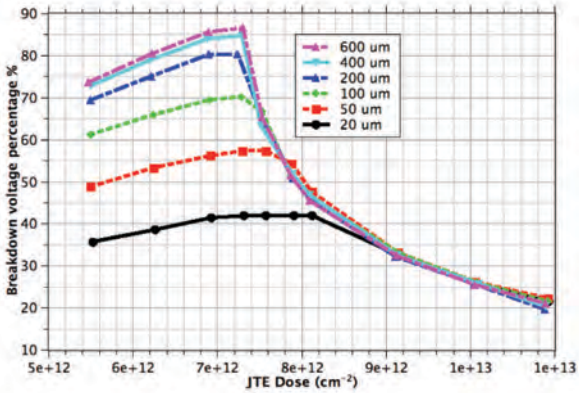

Fig. 7: Breakdown voltage percentage of a MESA-JTE diode versus the implanted dose of the JTE for different JTE lengths. Etch depth was fixed to 4 µm.

For a dose of 7×10^{12} cm^{-2}, the breakdown voltage is close to the ideal $P^{+}N$ plane semi-infinite junction (16.5 kV) and is independent of the JTE length (see "**Fig. 7"**). When the etching depth increases the range of optimized dose also increases, and the protection efficiency increases. The combined MESA-JTE allows obtaining better results than MESA or JTE edge terminations.

D. OTHERS COMBINATION OF TERMINATIONS

The advantages of each termination could be combined and adapted to the junction features, as an example, the etched JTE has been applied to the thyristor structure [15].

New protections are needed, using combination of MESA, single and/or multiple JTE, and guard rings in order to increase the

breakdown voltage (see e.g. "**Fig.8**"). It allows widening the parameter ranges and being closer to the 100% efficiency, but one should keep in mind that the area used by the protection itself should be reduced as much as possible to reduce the total cost of the device. It is particularly true for high voltage device, due to the thick drift layer.

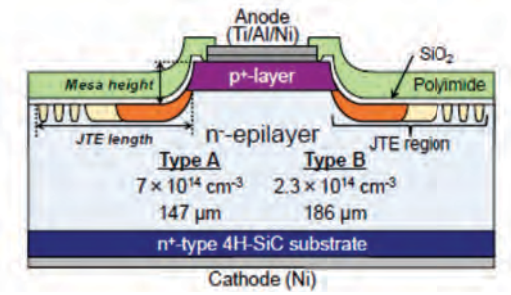

Fig. 8: Schematic cross section of a 4H-SiC PiN diode protected by two-zone JTE and space-modulated JTE [7].

E. SPECIFIC PROTECTION FOR DIAMOND

The lack of n-type doping prevents the use of the classical technics for diamond devices. As shown in **"Fig. 9"**, specific dielectric combined with field plate were applied in [16] to a pseudo-vertical Schottky diode.

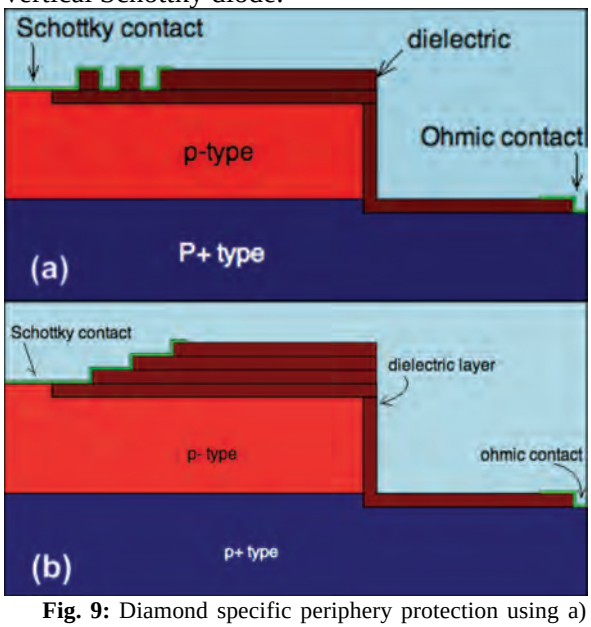

Fig. 9: Diamond specific periphery protection using a) pillars and b) graduated dielectric form.

4. Work to be done to increase the breakdown voltage

The high voltage devices are mainly used in high power applications, it means that increasing the area of the active part of the device is important. Rectangular shape of device is one way to increase the size in comparison with circular one. In such case, rounded corner are designed to avoid electric field crowding.

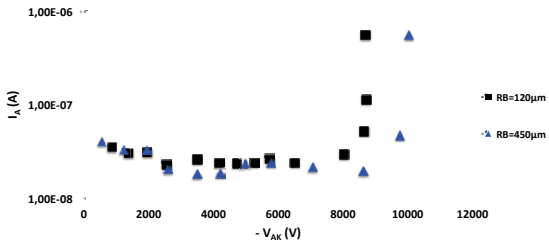

Fig. 10: PiN diode breakdown voltages for two bend radius (120 µm and 450 µm)..

A 3D-simulation has been performed to exhibit the effect of the bend radius on the maximum electric field in the structure. The simulation was stopped for the same critical electric field in both structures. As shown in "**Fig. 10**", the bigger bend radius allows an increase on the breakdown voltage of almost 2 kV compared to the smaller one allowing an increase in JTE efficiency from 66 % up to 80 %.

Passivation layers

Higher voltage devices will induce a high electric field stress in the passivation layer. Therefore, extended performances of packaging materials are necessary to sustain higher voltage and also temperature. An insulation material with appropriate high dielectric rigidity will prevent the formation of premature arcing. Polyimides appear as potential candidates for the surface electrical insulation of these high voltage devices [17]. Fluorinated parylenes have also good physical properties with respect to temperature [18].

Packaging

Specific packages are required for high voltage devices. The material itself must be able to sustain high electric field, but the layout of the electrodes must be properly designed (distance between electrodes).

Ionization coefficients determination

An experimental bench to measure Optical Beam Induced Current (OBIC) is under development in our laboratory. **"Fig. 11"** is a schematic view of this set-up. The aim is to create carriers using a focused laser beam in a diode under reverse bias. When carriers are created in a space charge region (SCR), they are separated by the electric field and collected at the electrodes, so that a photocurrent, called OBIC, is measured. Using motorized mirrors allow to shift the laser beam along the surface of the device. Finally, we are able to make a mapping of the OBIC for the

device under test. This gives an image of the distribution of the electric field around the devices. A second aim of this bench is to determine the ionization coefficients for several semiconductors. In this case, the aim is to measure the OBIC as a function of the applied reverse voltage, at a given point (ideally at the center of the diode, which need to realize an optical window through the frontside contact). Then theoretical calculations allow to extract ionization coefficients. Recently, we have demonstrated the feasibility of such a technique using a wavelength much more less than the bandgap. Therefore, two photons are required to ionize a dopant atom. That is the so-called biphotonic generation [19].

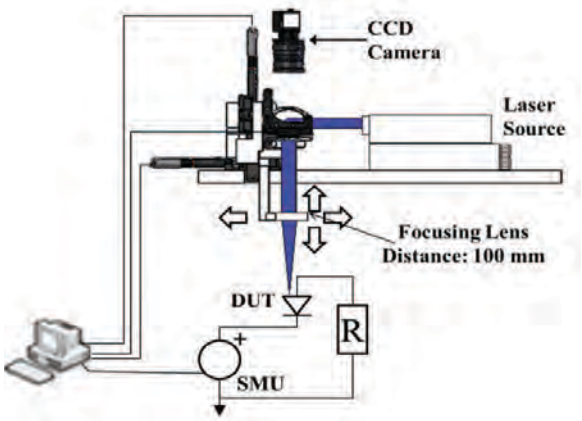

Fig. 11: Basic principle of experimental setup OBIC [19].

5. Conclusion

Last decade has witnessed a fast increase in blocking voltage, however the introduction of these devices in power electronics is still in its infancy. For ultra-high voltage devices, based on WBG semiconductors, some improvements are still necessary, in terms of device design, device characterization, material growth for good quality material, lifetime control, packaging, material knowledge…

6. References

[1] M. Mermet-Guyennet, *"New Power Technologies for Traction Drives"*, SPEEDAM, Int. Symp. On Power Electronics Electrical Drives, Automation and Motion, pp. 719-723, 2010.

[2] S. M. Kaplan, *"Smart Grid. Electrical Power Transmission: Background and Policy Issues"*, The Capital.Net, Government Series, pp. 1 – 42, 2009.

[3] Smart Grid: [Online] Available: http://www.en.wikipedia. org/wiki/Smart_grid (retrieved on July 25, 2014).

[4] M. Petit, S. Bacha, X. Guillaud, H. Morel, D. Planson, B. Raison, *"Les réseaux HVDC multi-terminaux : des défis multiples en génie électrique"* SGE, Cachan, France, 8-10 Juillet 2014.

[5] C. Raynaud, D. Tournier, H. Morel, D. Planson, *"Comparison of high voltage and high temperature performances of wide bandgap semiconductors for vertical power devices"*, Diamond & Related Materials vol.19 (2010) pp. 1-6.

[6] P.N. Volpe, P. Muret, J. Pernot, F. Omnes, T. Teraji, Y. Koide, F. Jomard, D. Planson, P. Brosselard, N. Dheilly, B. Vergne, S. Scharnolz, *"Extreme dielectric strength in boron doped homoepitaxial diamond"*, Appl. Phys. Lett. 97, 223501 (2010)

[7] N. Kaji, H. Niwa, J. Suda, T. Kimoto, *"Ultrahigh-Voltage (>20 kV) SiC PiN Diodes with a Space-Modulated JTE and Lifetime Enhancement Process via Thermal Oxidation"* Materials Science Forum Vols. 778-780, pp. 832-835, 2014

[8] T. Hiyoshi, T. Hori, J. Suda, T. Kimoto. *"Bevel Mesa Combined with Implanted Junction Termination Structure for 10 kV SiC PiN diodes"*, Materials Science Forum, Vols 600-603, pp. 995–998, 2009.

[9] M. Berthou. *"Implementation of high voltage Silicon Carbide rectifiers and switches"*. PhD thesis, INSA de Lyon, 2012.

[10] V. Veliadis, E.J. Stewart, H. Hearne, T. McNutt, W. Chang, M. Snook, A.J. Lelis, C.J. Scozzie, "Design and Yield of 9 kV Unipolar Normally-ON Vertical-Channel SiC JFETs", Materials Science Forum, Vols 679-680, pp. 617–620. 2011.

[11] M.K. Das, C. Capell, D.E. Grider, R. Raju, M. Schutten, J. Nasadoski, S. Leslie, J. Ostop, A. Hefner, *"10 kV, 120 A SiC Half H_Bridge Power MOSFET Modules Suitable for High Frequency, Medium Voltage Applications"*, Energy Conversion Congress and Exposition (ECCE), 2011 IEEE, pp. 2689-2692, 17-22 Sept. 2011

[12] Q.C. Zhang, R. Callanan, A.K. Agarwal, A.A. Burk, M.J. O'Loughlin, J.W. Palmour, C. J. Scozzie, *"10 kV, 10 A Bipolar Junction Transistors and Darlington Transistors on 4H-SiC"*, Materials Science Forum, Vols 645-648, pp. 1025– 1028. 2010.

[13] G. Pâques, S. Scharnholz, N. Dheilly, D. Planson, R.W. De Doncker, *"Comparison of SiC Thyristors with Differently Etched JTEs"*, Materials Science Forum, Vols 717-720, pp. 1167–1170. 2012.

[14] D. Carole, S. Berckmans, A. Vo-Ha, M. Lazar, D. Tournier, P. Brosselard, V. Soulière, L. Auvray, G. Ferro, C. Brylinski, *"Buried Selective Growth of p-doped SiC by VLS Epitaxy"*, Materials Science Forum, Vols 717-720, pp. 169–172. 2012.

[15] G. Pâques, N. Dheilly, D. Planson, R.W. De Doncker, S. Scharnholz, *"Graded Etched Junction Termination for SiC Thyristors"*, Materials Science Forum, Vols 679-680, pp. 457-460. 2011.

[16] H. Arbess, K. Isoird, *"Field Plate Termination for High Voltage Diamond Schottky Diode"*, International Conference on Microelectronics (ICM-Beyrouth / Lebanon) June 2013.

[17] S. Diaham, M.L. Locatelli, T. Lebey, C. Raynaud, M. Lazar, H. Vang, D. Planson, *"Polyimide Passivation Effect on High Voltage 4H-SiC PiN Diode Breakdown Voltage"*, Materials Science Forum, Vols 615-617, pp. 695-698. 2009.

[18] R. Khazaka, M.L. Locatelli S. Diaham, M. Bechara, H. Hourdequin, R. Kumar, *"Conduction Currents in Fluorinated Parylene PA-HT at High Temperature"*, IEEE Int. Conf. on Solid Dielectrics, Bologna, Italy, June 30, July 4, pp. 49-52. 2013

[19] H. Hamad, C. Raynaud, P. Bevilacqua, D. Tournier, B. Vergne, D. Planson, *"Optical Beam Induced Current Measurements based on two-photon absorption process in 4H-SiC bipolar diodes"*, Applied Physics Letters 104, 082102, 2014. doi:10.1063/1.4866581