



From quasi-static to transient system level ESD simulation: Extraction of turn-on elements

Fabien Escudié, Fabrice Caignet, Nicolas Nolhier, Marise Baffleur

► To cite this version:

Fabien Escudié, Fabrice Caignet, Nicolas Nolhier, Marise Baffleur. From quasi-static to transient system level ESD simulation: Extraction of turn-on elements. Electrical Overstress/Electrostatic Discharge Symposium (EOS/ESD), 2016 38th, ESD Association, Sep 2016, Anaheim, United States. pp.1 - 10, 10.1109/EOSESD.2016.7592563 . hal-01387072

HAL Id: hal-01387072

<https://hal.science/hal-01387072>

Submitted on 28 Oct 2016

HAL is a multi-disciplinary open access archive for the deposit and dissemination of scientific research documents, whether they are published or not. The documents may come from teaching and research institutions in France or abroad, or from public or private research centers.

L'archive ouverte pluridisciplinaire **HAL**, est destinée au dépôt et à la diffusion de documents scientifiques de niveau recherche, publiés ou non, émanant des établissements d'enseignement et de recherche français ou étrangers, des laboratoires publics ou privés.

From Quasi-static to Transient System Level ESD Simulation: Extraction of Turn-on Elements

Fabien Escudié (1), Fabrice Caignet (1), Nicolas Nolhier (1), Marise Bafleur(1)

(1) LAAS-CNRS, Université de Toulouse, CNRS, UPS, Toulouse, France
tel.:05 61 33 62 00, e-mail: fescudie@laas.fr.

Abstract – Transient simulation is a main challenge to achieve system level ESD failure prediction. During the turn-on of the protections, complex phenomena introduce complex transient behaviors. In this paper we investigate the parameters that have to be added to perform accurate transient simulations and we propose a methodology to extract them by measurements.

I. Introduction

Achieving efficient system level electrostatic discharge (ESD) reliability is a main challenge in embedded systems. As there are more and more embedded systems, they are exposed to severe environments and the failure requirements are growing in importance. The analysis and understanding of malfunction is usually very difficult. The ESDA (ESD Association) industry council has pointed out the importance in performing System Efficient, ESD Design (SEED)[1]. Several studies were done in order to predict the impact on systems of electrical fast transients using a behavioral simulation [2,3,4,5,6]. The models created by I(V) curves obtained from Transmission Line Pulse (TLP) allow quasi-static simulations. In these papers good measurement correlations are obtained when the rest of the system is modeled with a high level of accuracy. However, an accurate transient behavior cannot be obtained with this simple I(V) model. The dynamic turn-on behavior of the protection can have a large influence on the overshoot or on the time to trigger and up to now this has not been studied except one that will be discussed [14].

A method to predictive ESD simulation is being developed in seven labs within the ESD association working group WG26: “Models for system level simulation”. The main goal is to cover a wide range of ESD protections like the ones in digital, fast communication and automotive components. This work focuses on a LIN (Local Interconnect Network) for automotive applications. Three different products are tested, that allow testing three different on-chip protections. Thanks to these differences we will investigate different transient behaviors.

The developed board to inject the ESD stress and measure the corresponding response will be presented in the first chapter. The measurement setup will be described in detail with its frequency limits. The next paragraph will summarize how conventional modeling approach is performed, and the models built for the three devices. In

this section the model of the devices is built from quasi-static I(V) TLP measurements.

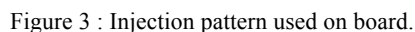
One of the first important goals of modeling is the validation of the models. In the following section two case of configuration are presented: without external elements and with an external decoupling capacitance. We have chosen an external decoupling capacitance because when a snapback protection turns on, the discharge of the capacitance into the device is mainly limited by the on-chip transient parameters. In our opinion, it represents one of the most complex transient event, exhibiting a very high current discharge into the chip, which is only limited by the transient behavior of the protections. For each configuration the three devices are tested and the validity of the “basic” model is discussed.

The observations will confirm that transient parameters are needed to accurately reproduce voltages and current waveforms. In this paper we proposed to obtain transient parameters from TLP measurements. Two main parameters are extracted: the first one just before the turn-on of the protection, to be sure that the transient charge of the input pin device is reproduced and a second one, reproducing the dynamic turn-on behavior of the protection. The extracted parameters allow generating an advanced model, and we will demonstrate the benefits of the model on the cases of study. A description to build the model and the experienced difficulties are detailed. Finally, two LIN boards are connected with a cable and the injection is made between them. The objective is to predict how the on-chip protections behave.

II. System under test

The main goal of this study is to validate the classical SEED modeling approach that is presented in most of the papers. Following this objective, a dedicated PCB has been developed in order to allow various injections, have multiple system configurations and to be able to perform voltage and current measurements. The system under test is

The LIN driver is an eight-pins device with one power supply (Vsup), one ground (gnd), the output communication wire (LIN) two control mode signals (Wake & INH) and 3 pins connected to a microcontroller (EN, RxD & TxD). Among these pins, only two are connected to the outside world and are supposed to undergo ESD events. So the IC models will be built between Vsup, GND and LIN pins. As reported in figure 1, the system can be powered using a LM312 regulator with its decoupling capacitances. A picture of the board is given in figure 2.



Current measurement is carried out using a near field probe placed above a micro strip line [8,9,10]. The induced voltage from the magnetic field is computed in the frequency domain to reconstruct the current through the stripe line. The frequency response on the probe has been precisely measured using the calibration pattern and a VNA (Fig. 5). We can observe that the S21 parameter has a +20dB/Dec slope that confirms the purely inductive coupling effect between the probe and the PCB line.

The graph displays the S21 Current probe response. The x-axis is logarithmic, with major ticks at 10000000, 100000000, 1E+09, and 1E+10. The y-axis is linear, with major ticks every 5 units from -30 to -75. A single data series, labeled 'S21 Current probe', is plotted as a blue line. The curve starts at approximately -72 for x=10^7, decreases steadily to about -45 at x=10^8, and then continues to decrease more slowly, reaching approximately -35 at x=10^9. The curve exhibits some high-frequency noise, particularly in the region between 10^8 and 10^9.

Figure 5 : Frequency response of the near field current probe.

III. Conventional model generation and system simulation

Following the methodology presented in most papers dealing with SEED, behavioral models are created with quasi-static measurements performed using a TLP tester. Usually the TLP have a 100 ns and a rise time around 1 ns. The exposed pins are measured (between ground and power supply), and a behavioral on-chip strategy is built. The compact models of the protection are made up using a piecewise linear description.

In the paper, we will follow the same method to build the model and we will show that it could induce strong error depending on the system configuration. The component's pins are tested in pairs with positive and negative pulses. For the Lin device only one pin is exposed to the outside world, and three pins are measured (LIN, GND, VDD pins). Figure 6 reports the LIN to GND I(V) curves obtained from three different providers called (A,B,C).

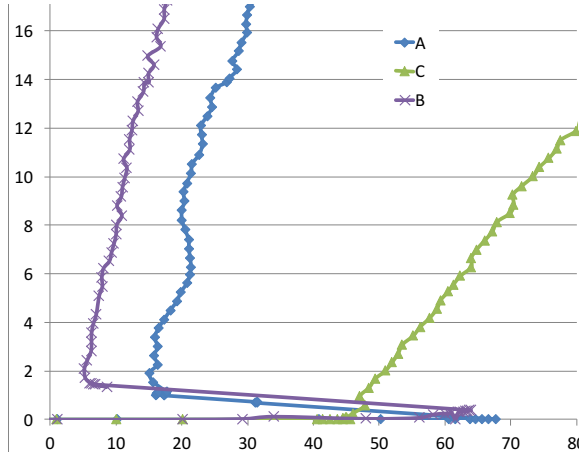


Figure 6 : I(V) curves of the 3 LIN components for positive pulse on LIN-GND pins.

Piecewise linear models are developed from the TLP measurement data (fig.7). The I_x, V_x points describe the ESD protection by piecewise segment, which is included in simulations like state machines in VHDL-AMS [11]. For the component C, the model of fig. 7 (a) is used. For components A and B that exhibit a strong snapback, the model of figure 7(b) is used with a strong non-linearity. Such model describe in VHDL-AMS can be found in **Erreur ! Nous n'avons pas trouvé la source du renvoi..**

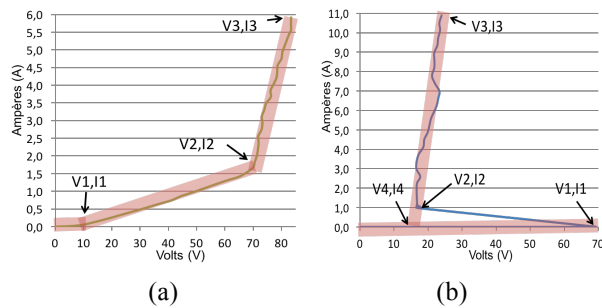


Figure 7 : IV curves « linear » and « non-linear » piecewise modeling.

The LIN component is composed by the I(V) curves obtained between the LIN, VSUP and GND pins with the IBIS information (R package, L package and C package) [12] associated. The three devices have exactly the same electrical schematic, only the description of the protections is different. As they have the same package, the parasitic elements (Rpck, Lpck and Cpck) are the same (even if some small differences can exist.)

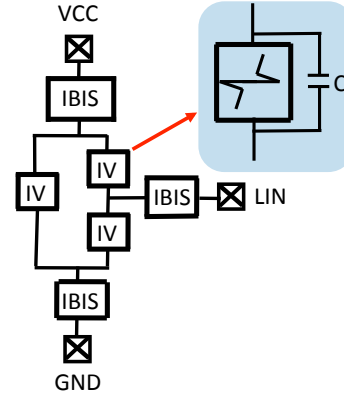


Figure 8 : Schematic diagram of the Lin component .

The whole measurement setup, the transmission lines and the PCB are reproduced in simulation (fig. 9). The TLP generator is made of a transmission line, the 1ns time rise filter is made of RLC elements [13], the attenuator is represented by a T of resistors, all cables are inserted as a transmission line and the PCB is introduced in simulation as LC distributed elements.

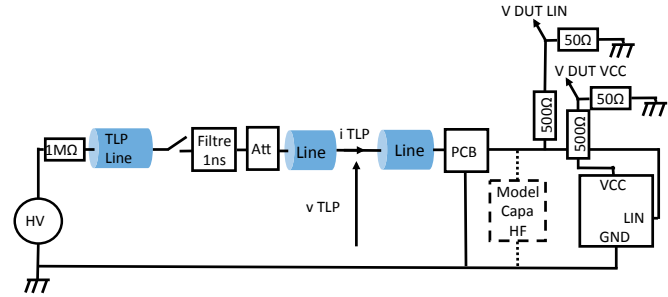


Figure 9 : Schematic diagram of the whole simulated system.

IV. Simulation analysis

In a first step, only TLP injection is done. This allows a better understanding of the phenomenon we want to characterize. Each time, simulation is compared with voltage and current measurements, but depending on the analysis, only the most significant observations will be reported. First, the quasi-static simulation results are investigated to establish the validity of using piecewise linear model and its limits. Next transient simulation is investigated to clearly show the inaccuracies in the methodology.

A. Quasi-static simulation

Figure 10 & 11 report the voltage measurement and simulation for 100V, 400V and 800V TLP injection respectively. If we look at the plateau of the waveform, the

simulated voltage fits perfectly with the measurements as expected. We can just notice that the measurement of 100V TLP injection on the B component shows a continuous increase of the voltage until the protection triggers at around 30ns. The model extracted from the TLP measurements could not be reproduced, because the I-V points are computed at around 80ns.

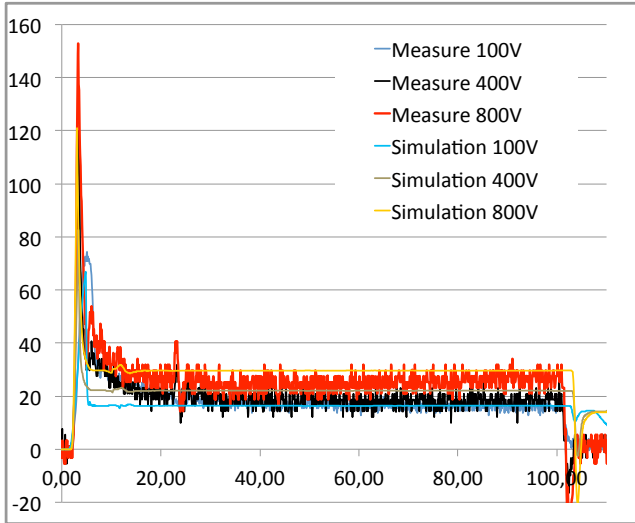


Figure 10: Comparison of voltage measurement with simulation with no external elements for component A – TLP injection 100V, 400V, 800V.

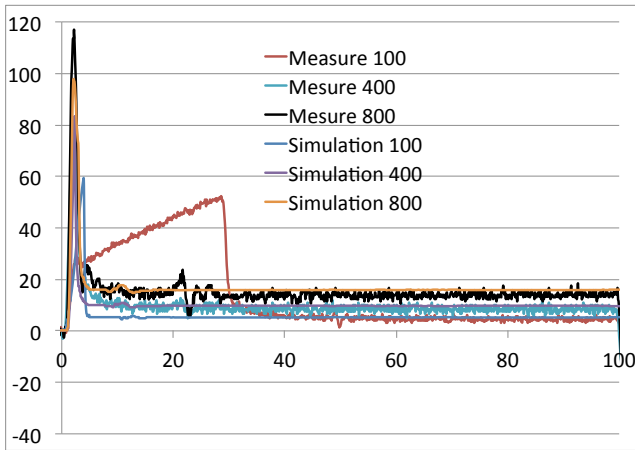


Figure 11: Comparison of voltage measurement with simulation with no external elements for component B – TLP injection 100V, 400V, 800V.

B. Transient simulation

Such result is predictable but we are also interested by the response of the model with an external component like a decoupling capacitance of 1nF on the LIN input. The main point is to validate the model whatever the external component is placed around the device. Even if it looks as a simple device, an external decoupling capacitance introduces complex phenomena. Figure 12 reports measurement and simulation with and without a 1nF capacitance placed in parallel to the input of the LIN for component A (The configuration without this capacitance is

also reported), 100V TLP injection. In this simulation the output capacitance is modeled with its high frequency parameters extracted using VNA.

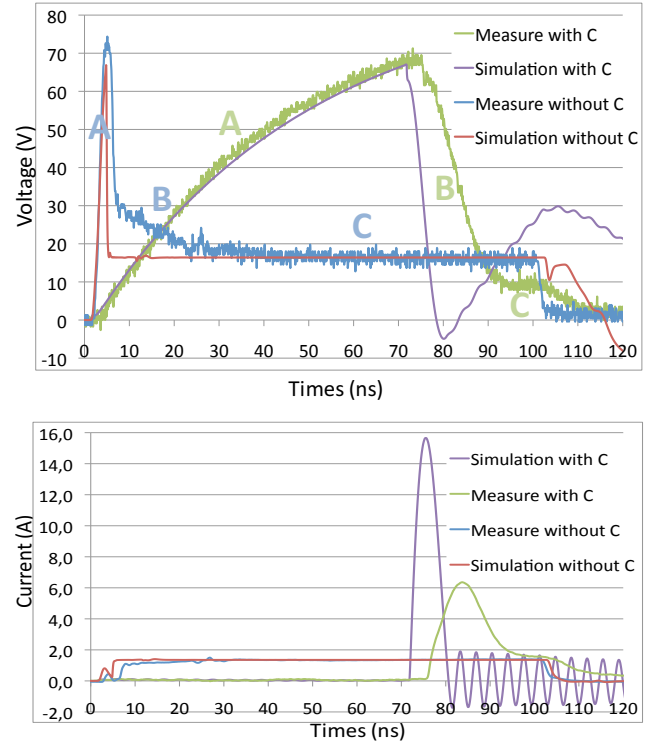


Figure 12 : Comparison between simulation and measurement for voltage and current on LIN-GND pin (component A), 100V TLP injection.

These curves can be divided into 3 parts, the charge of ESD protection before the triggering voltage (A), the time from peak voltage to give a stable level (B) and the quasi-static level (C). The simulations matched well during the first and the third state. In area B, the current through the component is much more important in simulation caused by a fast discharge of the capacitance (strong snapback). It appears that another phenomenon controls the current path just after the triggering of the protection. The on-resistance extracted from TLP I(V) measurement is not the one foreseen by the protection during a few nanoseconds. This can be observed on the voltage (measure and simulation) without the capacitance. On measurement, after the triggering of the protection, the voltage continues to increase (5V) and the first peak is larger than the simulation one. At 30V the voltage decreases slowly to its stable value at $t=25\text{ns}$.

Figure 13 reports the transient measurements obtained, with a 100V TLP injection between LIN and GND pins for component B. Quasi-static simulations exhibit a perfect correlation with the measurements for voltage and current levels at 80ns. But the measurements show that from 0 to around 30ns the voltage increased slowly. Following the classical model methodology, the simulation is not able to predict this (fig.13 – Simulation 1). To take into account such transient events into the simulation, additional parameters must be added. The next paragraph details what

parameters we chose and the way to extract them from measurements.

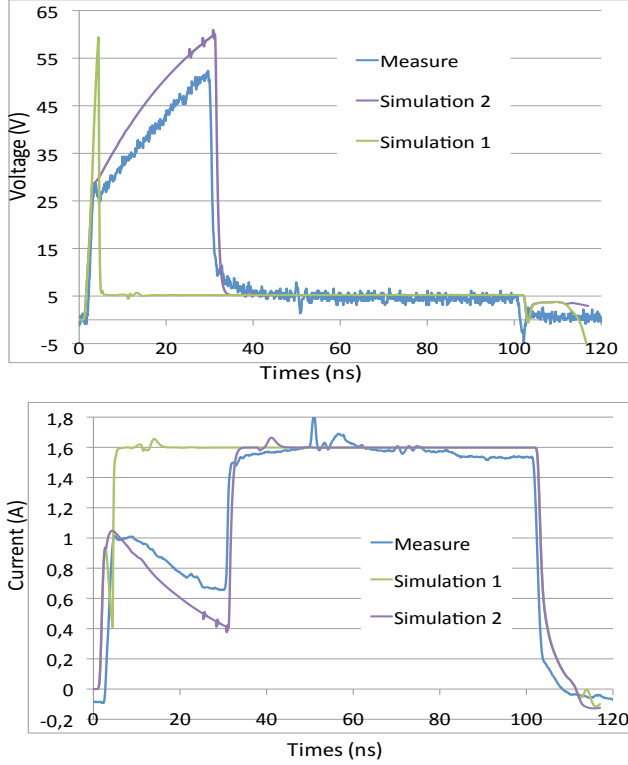


Figure 13: Comparison between simulation and measurement for voltage and current between LIN and GND pins with 100V TLP injection (component B).

IV. Model extension with transient parameters

A. Charge parameter extraction

The input capacitance of the device often added into the simulation reflects the time to reach the triggering voltage. This parameter could be obtained from the data sheet or is given into IBIS models. Most of the time, it is obtained using a VNA, which means a small signal analysis. This part is mostly purely passive. Looking at the measurement in figure 13, it is clear that during high injection, the behavior of the element(s) before the triggering of the protection could be non-linear. In this case, we make the assumption that it looks like a “non-linear capacitance” (even if it could be physically related to some active parts). The next step is to find a way to extract this “non-linear capacitance”. We built a set-up using a high precision capacitance (COG type) placed in parallel in footprint 3 (fig. 3) to get I(V) curves before the triggering voltage level. We calibrate this 1nF capacitance to be sure that it has a stable value from 0V to the triggered voltage level (around 70V). This capacitance will slow down the charge. Figure 14 reports the I(V) curves obtained at 80ns for the 1nF capacitance and the three components.

Component A follows the measurement of the 1nF capacitance. This confirms that before the snapback the behavior is purely capacitive. Component B shows a change (around 30V) that reflects an on-chip active part, then, it seems to increase as a capacitance up to 50V

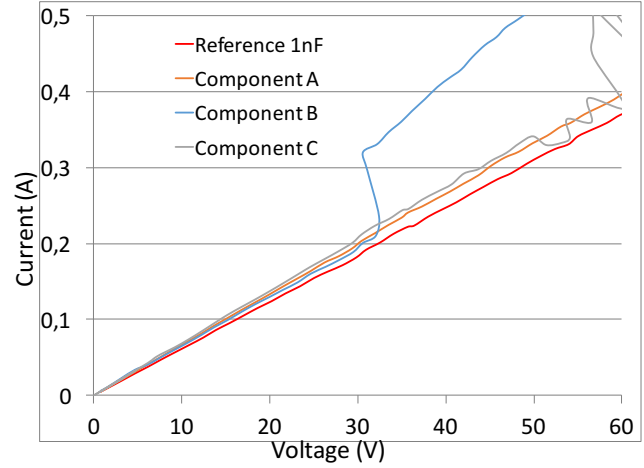


Figure 14: I(V) curves before triggering voltage with 1nF capacitance between LIN and GND pins.

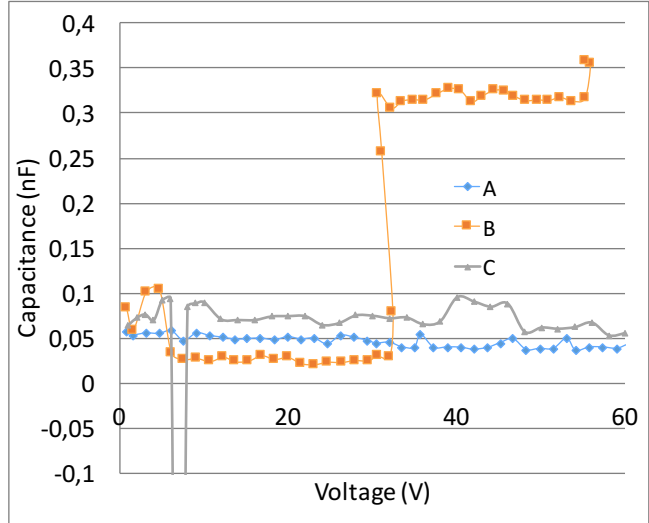


Figure 15: Equivalent capacitance of the LIN_GND protection.

In figure 15, the capacitance value from figure 14 is extracted using the charge capacitance formula (1 & 2).

$$uc(t) = E \times (1 - e^{-t/\tau}) + V_{ini} \times e^{-t/\tau} \quad (1)$$

$$c = -\frac{t}{R \times \ln\left(\frac{uc(t) - E}{V_{ini} - E}\right)} \quad (2)$$

Where $Uc(t)$ is the dynamic voltage, V_{ini} is the precharge voltage of the capacitance, E is the TLP charge voltage and τ the time constant of the RC network. To get figure 15, the time corresponds to the one chosen for the voltage measurement on the TLP waveform ($t=80ns$), and the initial voltage is $V_{ini}=0$. The capacitance C is calculated assuming that the resistance is 50Ω .

One of the most important results is that we succeed to get the input capacitance during the stress of component A (50pF). For component B we get a 30pF from 0V to 30V then something looking like a 300pF upon the turn on of the protection. For component C we obtained 70pF. If we look at the transient voltage curve $v(t)$ with 80V TLP injection (fig.16), there is a change in capacitance charge at 24V.

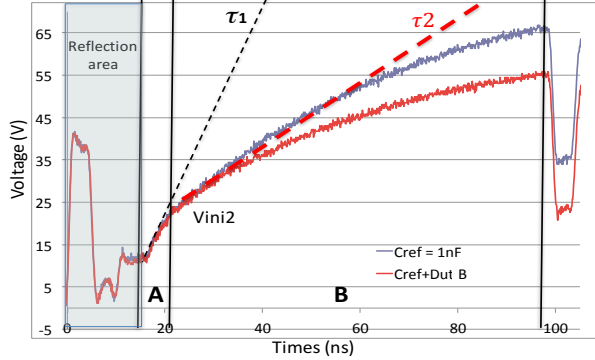


Figure 16: LIN-GND $v(t)$ curve at 70VTLP for the component B with 1nF external Capacitance in parallel.

The capacitance corresponding with τ_1 calculated in the A area is 30pF. In the B area the first 300pF obtained were calculated assuming that the initial voltage was zero and so the 300pF is not correct. We need to readjust V_{ini} and the time in equation (2). Taking into account the appropriate values, we found a 600pF capacitance for the LIN-GND protection on the B area. A variable capacitance for which the value is related to the voltage was introduced in the model and the simulation result is shown in fig.13 (Simulation 2).

B: Dynamic turn-on parameter extraction

If we focus on the two components A and B, they both have different turn-on conditions. Looking at the transient behavior, without external decoupling capacitances, the component B exhibits a quick turn-on, as the component A seems to have two different slopes when the voltage reaches its stable snapback value. When simulations are performed without external capacitances, this is not really important and both simulations give accurate results for both voltage and current. With the capacitance, a strong error is observed on the current simulation. This is mainly due to the prediction of the speed of the discharge into the component. Using a protection model based only on TLP measurements introduces a quasi-static resistance of around 1Ω that generates in the simulation a current discharge of 16A, and the measurement does not exceed 6A. An additional turn-on parameter is needed.

Recently, in paper [14], a first interesting transient modeling has been proposed. The model focuses on the transient aspect of the turn-on. No real parameter is extracted and a behavioral model is built using an equivalent dynamic resistance and an equivalent voltage

generator. This equivalent Thevenin model is built step by step in time domain. For each time point, the equivalent generators and resistances are extracted from the transient voltage response of the protection under TLP stress. This gives a $R(t)$ and $E(t)$ parameters.

In this paper we propose to build an equivalent SPICE schematic of the protection that represents both its static and dynamic responses. The main idea is that during transient the velocity of the operating point is driven by a higher resistance than the one get by TLP. We assume that the model built around quasi-static measurement can be enhanced with a dynamic part (Z_{dyn}) as reported in figure 17.

The generator E_p and the R_{stat} resistance represent the quasi-static equivalent model of the protection when the device turns-on. These two parameters are extracted from the quasi-static $I(V)$ curve. C_p represents the equivalent capacitance to define the charge slope (just before the triggering). This capacitance also impacts the turn-on speed. This parameter has been extracted in the previous paragraph.

To represent the dynamic aspect, a set of resistance R_{dyn} , in parallel with an inductance L_{dyn} is used. When the protection triggers ($t_0 + \epsilon$), the dynamic inductance passes no current and all the current goes through R_{dyn} . Instantaneously the equivalent serial resistance of the protection is $R_{dyn} + R_{stat}$. After few nanoseconds, depending on the value of L_{dyn} , the inductance acts as a short circuit reducing the serial resistance to R_{stat} . R_{dyn} and L_{dyn} form the dynamic impedance Z_{dyn} .

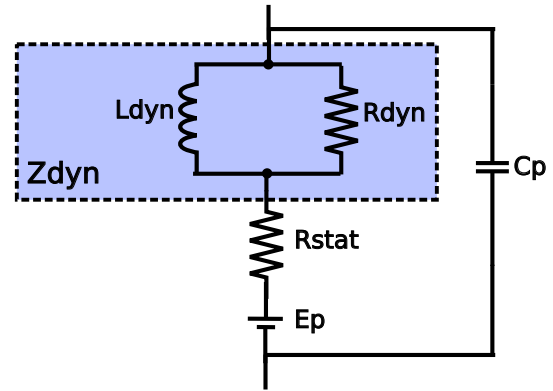


Figure 17: Equivalent electrical schematic of the protection when it turns-on.

On this paper we propose to directly extract R_{dyn} from TLP measurements and to adjust L_{dyn} by looking at the transient responses. The theory applied to extract the dynamic resistance is the same as the one used to get the dynamic resistance as applied to the small-signal behaviour of a semiconductor like diode or MOS devices [15].

Basically, to calculate the operating point of the snapback device under TLP stress, we plot the static load line (or DC load line) over the electrical mounting. During the triggering of the protection, we consider that a dynamic resistance drives the voltage and current. And so, the transient response follows the dynamic impedance represented in the dynamic load line (or AC load line).

From the transient response of the device to TLP, an I(V) curve is traced and reported in Fig. 18 for the component A and Fig 19 for component B. The quasi-static response of the protection is reported in red. The green, purple and blue curves are the dynamic responses of the protections for 100V, 400V and 800V TLP injection respectively. In the two figures, we draw the dynamic load line that fits the most linear part of the curves (400V & 800V). For component A, these two lines are perfectly parallel, meaning that the dynamic resistance must be the same whatever the value of the voltage across the protection. The extraction of the dynamic resistance for component A resulted in $R_{dyn} = 8\Omega$. In figure 19, the two load lines are not perfectly parallel. As the protection is faster than the previous one, the linearity is less defined, the inductance effect is more important. Nevertheless, on the linear part, we get $R_{dyn} = 11\Omega$ for 800V and 18Ω for 400V. In this case, the dynamic resistance could be a function of the current. In the simulation reported in this paper, we will fix it at 15Ω . For the component C, the same methodology is used to get $R_{dyn} = 11\Omega$ (not reported here).

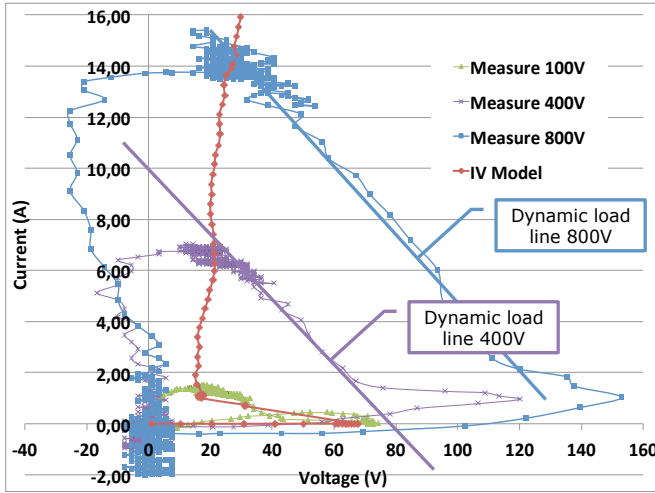


Figure 18: transient I(V) curves obtained during TLP stress (no external elements) of component A .

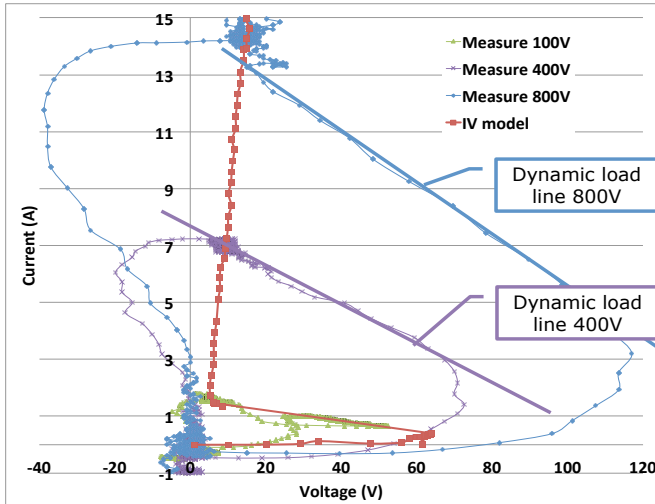


Figure 19: transient I(V) curves obtained during TLP stress (no external elements) of component B.

V. Validation of the extended transient models

After extracting from TLP measurements additional charge parameters and dynamic turn-on parameters, a new model is built for each A, B, C components. The results shown take into account the decoupling capacitance of 1nF placed in parallel, which exhibits the most complex discharge events.

Figure 20 reports the comparison between measurements and simulations of the basic model and the extended one taking into account the transient parameters. 800V and 100V TLP injection are compared. Looking at 800V injection, the advanced model is perfectly able to reproduce both the voltage and the current waveforms (overshoot and pulse duration). The current reaches 24A for a 14A injection. This means that the model is perfectly able to reproduce the transient turn-on of the snapback protection.

For 100V injection, there are small differences on the voltage. Regarding the current, the peak amplitude is reduced from 16A to 10A, and the measured value is 6A. For such small injection level, our model seems to be not accurate enough. If we look at the figure 12, the component A exhibits a turn-on in two parts: a first one very quick, and a long voltage decrease from 5 to 20ns. This second turn-on phenomenon (somehow not classical) is not reproduced by our modeling method.

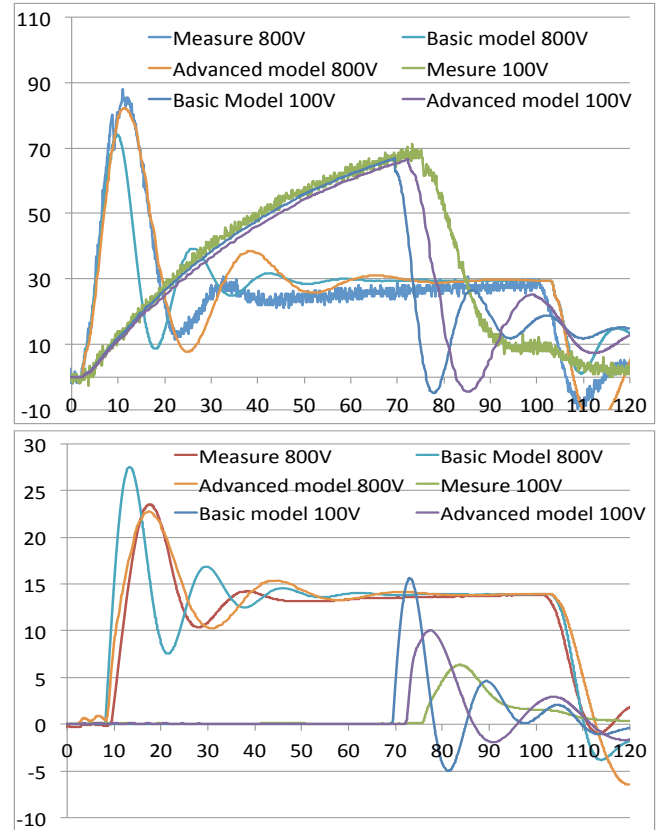


Figure 20: Comparison between simulation and measurement for voltage and current between LIN and GND pins with decoupling capacitance (component A).

In figure 21 the measurements of component C are compared with the models. The triggering voltage of this protection diode is around 40V. In general, the advanced models give better accuracy than basic I(V) ones. The overshoot (70V for 400V injection & 95V for 800V injection) is well reproduced.

If we look into details, on the voltages, for 400V injection, with the advanced models, the simulated waveform is below the measured one, which is the opposite for 800V injection. The overshoot is mainly related to the inductance effect. This means that the L_{dyn} we put into the model is higher than the equivalent one found in the device. We define L_{dyn} for each component by fitting the turn-on speed. A good way to extract this parameter has to be found for better accuracy. Another point is that for 400V TLP injection R_{dyn} extracted using the method proposed in chapter IV.B is 11Ω and 6Ω for 800V. In the simulation we implemented R_{dyn} of 10Ω . If the resistance increases, the overshoot is increased. It means that the model of the dynamic resistance has to be carefully tuned.

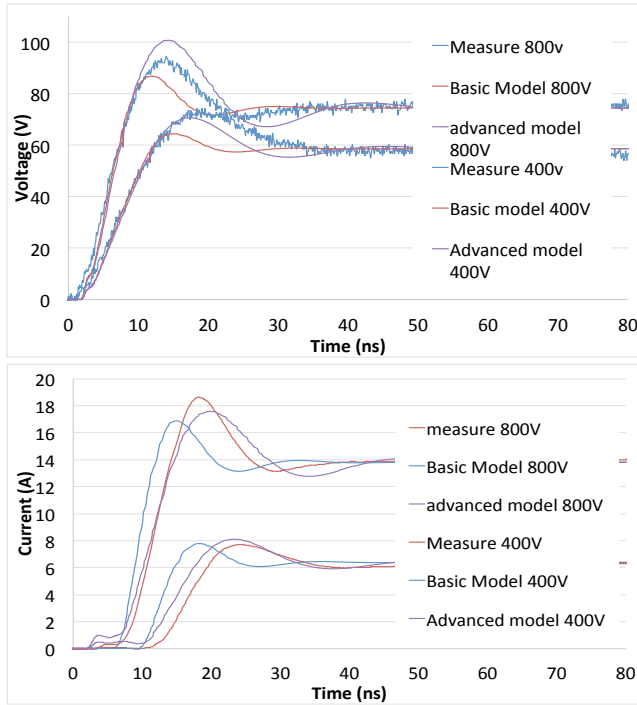


Figure 21: Comparison between simulation and measurement for voltage and current between LIN and GND pins with decoupling capacitance (component C).

Looking at the result, adding a dynamic impedance into the model of the on-chip protections significantly increases the accuracy of the simulations. This is even more important if current is investigated. We demonstrated that for high level of injection the proposed model gives very good result on the three investigated components.

VI. Validation with two boards connected by wires

In this part, we tested two boards based on LIN components connected together with cables, one embedding component A and the other component C.

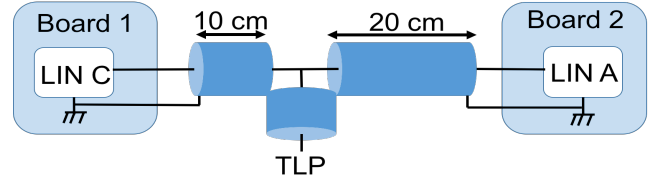


Figure 22: Schematic of equipment under test

Using such configuration, we wanted to validate our transient model. TLP stress is injected at 10cm from one board including component C and at 20cm to the other with component A. The two components are mounted on board alone, with no external elements. The simulation results are compared to the measurements for multiple values of injected voltage (100V, 200V, 800V).

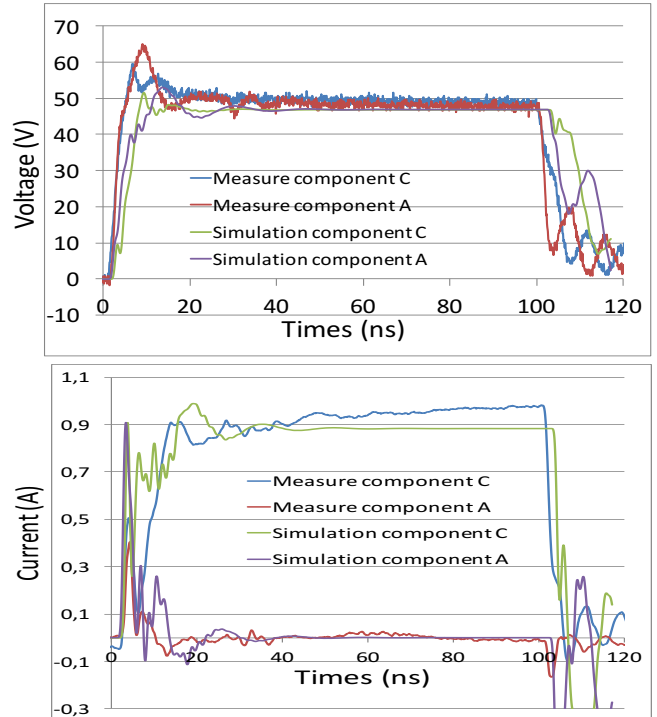


Figure 23: Measure and simulation results for the LIN-GND protection of C and A components, 100V TLP injection

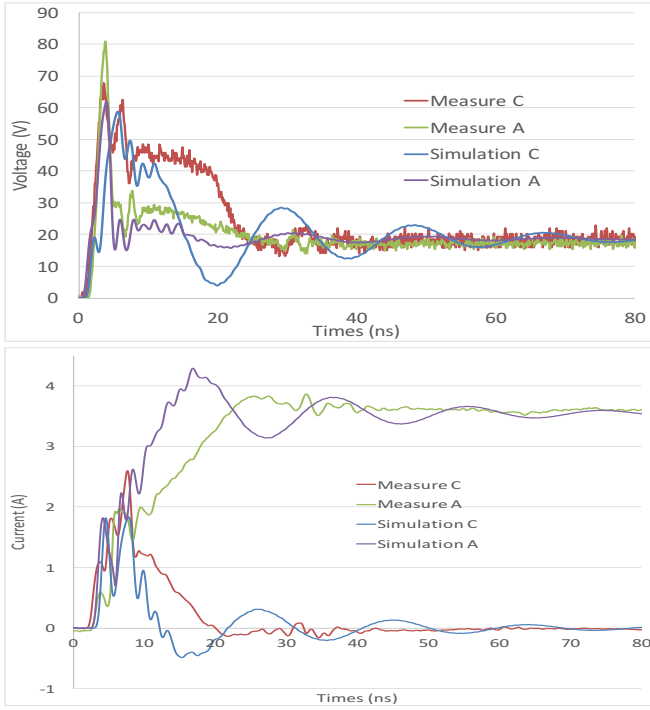


Figure 24: Measure and simulation results for the LIN-GND protection of C and A components, 200V TLP injection.

In figure 23, 100V TLP is injected. Simulation and measurement correlate and all the current goes into the component C. In figure 24, 200V is injected. The behavior is totally different and at this time the component A conducts the current. It takes approximately 20ns for the system to stabilize, and the simulation gave us around 10ns. We can notice that the measured voltage on component C stays more than 10ns around 40-45V, which is its triggering voltage.

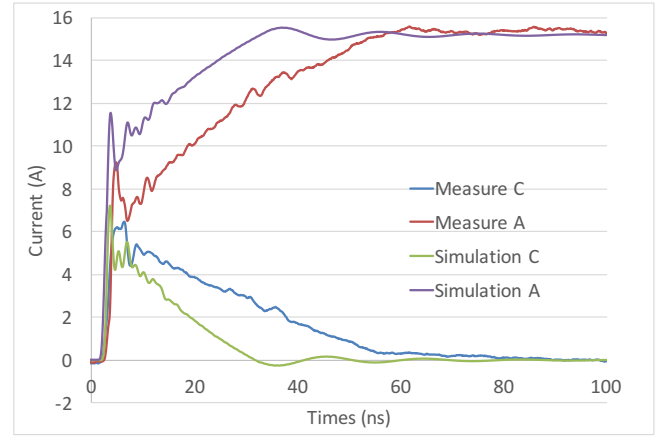
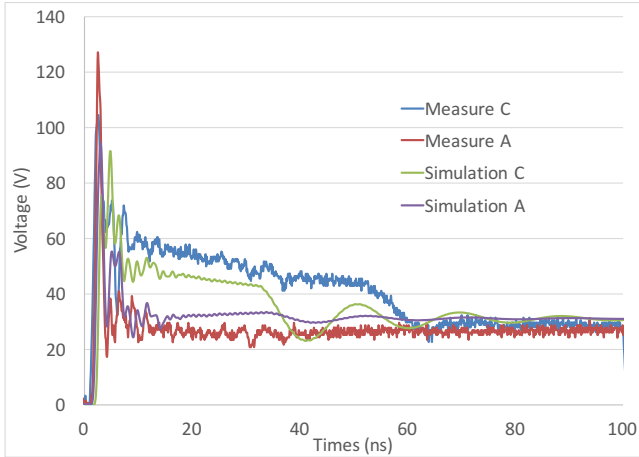


Figure 25: Measure and simulation results for the LIN-GND protection of C and A components, 800V TLP injection.

Figure 25 is obtained for 800V TLP injection. The surprising thing is that even if we have a strong injection, it takes approximately 50-60ns for the system to stabilize. If we look at the current, our simulation is able to predict this long time to distribute the discharge on the two components. The slopes of the measurement and simulation are well reproduced but the started amplitude levels do not match. At this point of study, it is difficult to say if it is due to the triggering conditions of the devices or to a line-modeling problem that drives the stress to on component more quickly then expected.

Conclusion

In this paper we investigated the way to perform transient simulations to predict the impact of system level ESD stress. A dedicated board has been designed around three devices to be sure that the proposed method is applicable for various on-chip protections. Initially, we extracted quasi-static I(V) curves from TLP measurement as done in most of papers addressing SEED. Then the model built from this measurement was compared with simulation. With no external elements, this methodology gives very good results, and the quasi-static voltages and currents can be accurately predicted. When an external decoupling capacitance is added, a lot of mismatches appear showing that transient simulation is required if we want to have accurate prediction. In the measurement and simulation reported, more than 150% of error is observed. To take into account this dynamic behavior into simulation, additional elements that translate dynamic turn-on behavior of the device must be added.

From these observations, we proposed a set of measurement methodologies to extract first an on-chip equivalent capacitance that reproduces the way the voltage increases. Second, we added to the quasi-static model a dynamic impedance made up of a resistance and an inductance in parallel. The dynamic resistance is extracted from a time representation of the I(V) curve, and the inductance is set to fit the time to reach the stable value. This combination of the R_{dyn} and L_{dyn} enables the modeling of the relaxing time of the ESD protections.

The enhanced model is compared with measurement in different configurations with different devices and shows a very good accuracy. We demonstrated that it is possible to get transient parameters from TLP measurements that provide transient system level ESD simulations. This work is under progress and it has to be fully validated with ESD gun stresses.

Acknowledgements

The authors would like to thank the French national agency of research (ANR) for its financial support of EFT-SAFE3A project. The authors would also address their thanks to the ESDA, WG26 (models for system level simulation) working group for their support on the boards and discussions on this topic.

References

- [1] Industry Council on ESD Target Levels, White Paper "System Level ESD, Part I: Common Misconceptions and Recommended Basic Approaches
- [2] N. Monnereau, F. Caignet, D. Trémouilles, "Building-up of system level ESD modeling: Impact of a decoupling capacitance on ESD propagation," Electrical Overstress/ Electrostatic Discharge Symposium (EOS/ESD), 2010 32nd, pp.1-10, 3-8 Oct. 2010
- [3] N. Monnereau, F. Caignet, N. Nohier, D. Trémouilles, M. Bafleur, " Behavioral-Modeling Methodology to Predict Electrostatic-Discharge Susceptibility Failures at System Level: An IBIS improvement," EMC Europe 2011 York, pp.457,463, 26-30 Sept. 2011.
- [4] N. Monnereau, F. Caignet, N. Nohier, et al. « Investigation of Modeling System ESD Failure and Probability Using IBIS ESD Models », IEEE Trans. on Device and Materials Reliability, Volume: 12 Issue: 4 Pages: 599-606, Dec. 2012.
- [5] Tianqi Li; et al., "An application of utilizing the system-efficient-ESD-design (SEED) concept to analyze an LED protection circuit of a cell phone," Electromagnetic Compatibility (EMC), 2012 IEEE International Symposium.
- [6] R. Mertens, E. Rosenbaum, H. Kunz, A. Salman, and G. Boselli, "A flexible simulation model for system level esd stresses with applications to ESD design and troubleshooting," 34rd Electrical Overstress/Electrostatic Discharge Symposium (EOS/ESD), 2012.
- [7] Collin Reiman, Nicholas Thomson, Yang Xiu, Robert Mertens and Elyse Rosenbaum, « Practical Methodology for the Extraction of SEED Models », Electrical Overstress/ Electrostatic Discharge Symposium (EOS/ESD), 2015.
- [8] IEC 61967-3: "Integrated Circuits, Measurement of Electromagnetic Emissions, 150 kHz to 1 GHz – Part 3: Measurement of Radiated Emissions – Surface Scan Method".
- [9] F. Caignet, N. Monnereau, N. Nohier, « Non-invasive system level ESD current measurement using magnetic field probe », International Electrostatic Discharge Workshop 2010, Tutzing (Allemagne), 10-13 May 2010
- [10] Wei Huang et al., "Probe characterization and data process for the current reconstitution by near field scan method," IEEE International Symposium of Electromagnetic Compatibility, June 2010.
- [11] IEEE 1076.1, "VHDL analog and mixed-signal," 1999.
- [12] ANSI/EIA-656B, "IBIS (Input Output Buffer Information Specification), www.eigroup.org/IBIS.
- [13] Y. Cao, et al. "Rise-Time Filter Design for Transmission-Line Pulse Measurement Systems," in *Microwave Conference, 2009 German*, pp.1-5, 16-18 March 2009.
- [14] Kuo-Husuan Meng, E.Rosenbaum, et al. " Piecewise-Linear With Transient Relaxation for Circuit-Level ESD Simulation", IEEE Trans. On Device and Materials Reliability, Volume: 15, 3 Sept. 2015.
- [15] A.P. Godse, U.A. Bakshi. " Semiconductor Devices & Circuits ", Technial publication Pune. Chapter 5.2.2, pp.256,259, Edition 2008.