

Thermal management and electromagnetic analysis for GaN devices packaging on DBC substrate

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Abstract—Printed Circuit Boards (PCBs) are often used to mount gallium nitride transistors, as they offer good electrical performance. However, their thermal conductivity is not as good as with ceramic substrates. In this paper, we compare (experimentally and by simulation) both the electrical and thermal performances of GaN transistor mounted on PCBs and ceramic substrates, and we show that with a proper layout, the ceramic substrates can offer both a very good thermal management (thermal resistance 4 times lower than with PCB) and suitable electrical performance (parasitic inductances of 1–2 nH).

Index Terms—GaN power device, thermal management, DBC substrate, simulation FEM, electromagnetic analysis.

I. INTRODUCTION

GALLIUM NITRIDE (GaN) is a wide-bandgap semiconductor material which offers many advantages, in particular a high electron mobility and a large critical field [1]. With the recent improvements in the GaN technology, power devices are becoming available. Because there is no bulk GaN substrate available, and because an attractive feature is the high mobility 2D-electron gas (which appears at the heterojunction between AlGa_N and GaN), GaN devices have essentially a lateral structure. This means that all electrically-active parts (contact pads, in particular) are concentrated only on one side of the die. This is uncommon in power electronics, as most silicon and silicon-carbide devices have a vertical structure, with electrical contacts on both sides of the die.

This lateral structure, along with their high switching speed capability, have many consequences on the packaging of the GaN devices. In particular, the stray inductances of the interconnects must be reduced as much as possible (lower than 1 nH in [2]). It is also true for the control circuit [3], [4], so the gate driver is placed as close as possible to the power device, with low-inductance connections. Printed Circuit Board (PCB) is well suited to take full advantage of these fast devices, due to its high-density interconnects and low inductance (in the case of multilayer PCBs).

Thermal issues are also a key aspect of packaging. Despite the improvement in conversion efficiency, the active devices dissipate a lot of heat (100 to 300 W/cm²). In this regard, PCB is not as attractive as it is has poor thermal conductivity (< 1 W/mK for FR4 material). Ceramic substrates (especially DBC, for Direct Bonded Copper) are preferred for medium

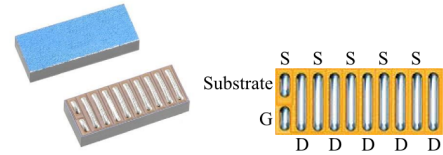


Fig. 1: EPC 2015 GaN transistors, rated at 33A, 40 V and 4 mΩ [10].

to large power packages (from kW to MW). In particular, alumina (Al₂O₃) is commonly used and offers thermal conductivities of 24 to 33 W/mK [5]). The dielectric strength of ceramic is lower (from 10 to 15 kV/mm) [5] than that of typical epoxy-based FR4 PCBs (54 kV/mm) [6]. Therefore PCBs may be thinner than alumina substrates for the same insulation rating. From a thermal point-of-view, however, the possible difference in thickness is not sufficient to make up for the difference in thermal conductivity. Thermal vias are often used to reduce the thermal resistance of PCBs [7], but they are electrically conducting.

While it has better thermal performance than PCB, the DBC substrate is not so attractive from an electrical point of view: its thick (typically 300 μm) copper layers offer low resistance interconnects, but they cannot be patterned with a high resolution (typical pitch is only 1 mm [8]). Furthermore, only one copper layer can be patterned to form a circuit, resulting in a planar layout with longer interconnects [9] and therefore to higher electrical and EMI constraints. A cost comparison between DBC and PCB is difficult, as a wide range of PCBs exist (various number of layers, of copper thicknesses, different qualities of dielectric material...). For small quantity orders, the cost is comparable (≈0.5 \$/cm²).

A first comparison of GaN converters built on PCB and DBC is presented in [14], and shows the interest of DBC (limited increase in inductance, large gain in thermal performance). In this paper, we demonstrate an even higher gain in thermal resistance (75 % reduction), and address stray inductance, resistance and capacitance. The studied GaN transistors are shown in Fig. 1. Provided by EPC, they are eGaN FET (enhancement mode, 40 V, 33 A [10]) with a very small die size (4×1.6×0.7 mm³). They are equipped with solder bumps for flip-chip mounting (Land Grid Array, or LGA package). This is efficient from an electrical point of view, with very short distances between the active area of the GaN transistor and the other components. From a thermal point of view, the bumps have limited thermal conductivity, and cover only a fraction of the die surface area. Section II is

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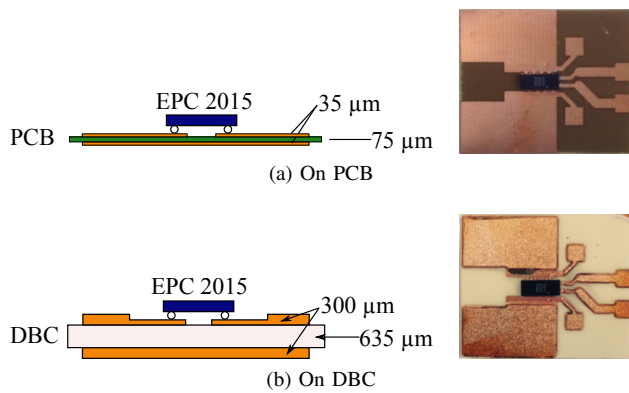


Fig. 2: Cross section of the prototypes.

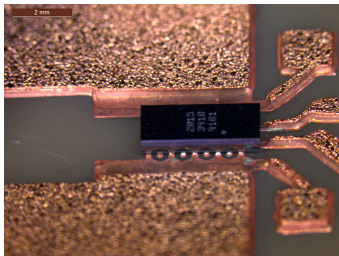


Fig. 3: Photograph of an EPC 2015 mounted on DBC with a two-step etching of the copper layer.

dedicated to comparing the thermal performance of designs made on ceramic and PCB. The electrical performance of both substrates is then analyzed in section III.

II. THERMAL MANAGEMENT

To compare the thermal performance of PCB and DBC substrates, the two structures presented in Fig. 2 are investigated. A very thin PCB structure ($70 \mu\text{m}$ FR4 thickness, Fig. 2a) is considered, to achieve a low thermal resistance. Regarding the DBC (Fig. 2b), a standard thickness is used for the ceramic. Note that both structures have comparable theoretical dielectric strengths (4000 and 6000 V respectively for the thin PCB and the DBC).

A. Fabrication

The “PCB” configuration (Fig. 2a) is made by laminating Isola 370HR prepreg layers and $35 \mu\text{m}$ -thick copper foil. The GaN transistor is mounted using a Zevac Onyx 21 flip-chip bonder, without additional solder (the SAC solder which forms the bumps is reflowed to attach the die to the substrate).

In the “DBC” configuration (Fig. 2b), a special etching technique (dual-step etching) is used. This allows for using thick copper on most of the surface (for low electric resistance) while having thin copper around the GaN die. This thinner copper layer is compatible with the resolution of the EPC 2015 transistors ($200 \mu\text{m}$ -wide bumps with a $400 \mu\text{m}$ pitch).

The first etching step removes approximately $250 \mu\text{m}$ from the $300 \mu\text{m}$ -thick copper layer: the substrate supplied by Curamik is coated by a photosensitive resin (MC Dip Coating) with a “Dip Coating” machine. After this step, the substrate is

TABLE I: Thermal conductivity values used in the simulation.

Material	Thermal Conductivity (W/m.K)
Copper	400
Ceramic	27
GaN Bumps	62
GaN Encapsulation	130
Prepreg	0.4
Silver paste	200
TIM	2
Heatsink	160

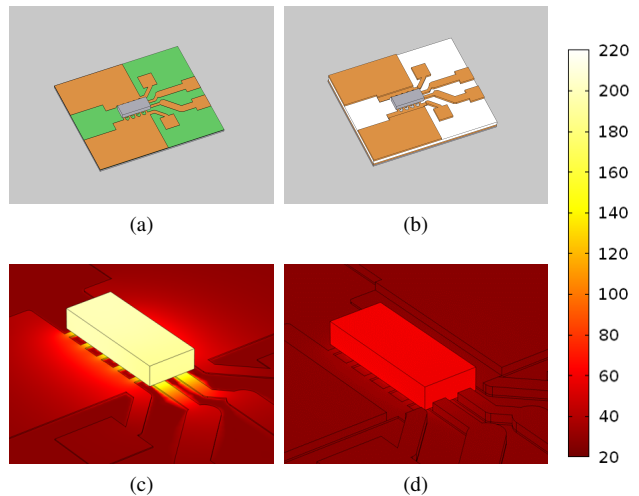


Fig. 4: Geometry of the models used for the thermal simulations on PCB (a) and on DBC (b), and corresponding temperature distributions, (c) and (d), respectively.

exposed to UV light through a first mask and developed. The copper etching is performed in ferric chloride, with a spray system (Bernier Elektronik PR2030). After cleaning, a second etching step removes the remaining $50 \mu\text{m}$ where needed to form the final layout, using the same process from coating to etching. A photograph of the result is visible in figure 3

B. Thermal analysis

3-D models, based on the Finite Element Method (FEM, Comsol) are used to simulate the temperature distribution in the prototypes. For both configurations (PCB and DBC, respectively Figs. 4a and 4b), we consider that the prototypes are attached on a heatsink (Fisher Elektronik SK 58/150 SA) through a layer of thermal interface material (TIM, Bergquist Q3AC). A heat dissipation of 10 W, located at the surface of the die on the bump side is considered in the model. The boundary conditions are an equivalent heat-transfer coefficient of $8 \text{ W}/(\text{m}^2\text{K})$ (corresponding to natural air convection) on all surfaces, and a constant temperature ($27 \text{ }^\circ\text{C}$) at the fins of the heatsink. The thermal conductivities for the different materials are given in Tab. I. The calculated temperature distributions in the two prototypes are shown in Fig. 4c and 4d, and confirm that the DBC offers a much better cooling. 4. We can note the big difference between the two substrates behavior proving that DBC substrates lead to much better thermal performances than PCB substrates (maximum junction temperature of $71 \text{ }^\circ\text{C}$ vs $207 \text{ }^\circ\text{C}$ respectively).

TABLE II: Thermal performance, for PCB and DBC. The measurement method is described in [11].

	I_D (A)	POWER (W)	T_J (°C)	R_{Th}	
				Experimental	Simulation
PCB	25	3.9	125	25 K/W	18 K/W
DBC	40	7.46	73	6.2 K/W	4.4 K/W

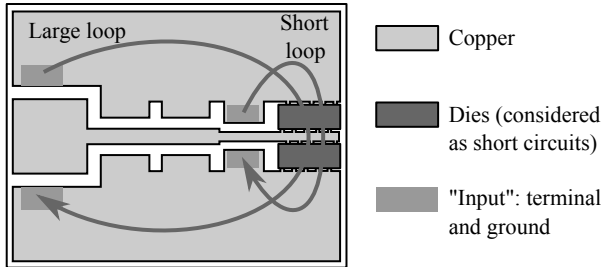


Fig. 5: Layout of the prototype used for the electromagnetic characterization, with the location of the terminal considered for inductance estimation. The upper and lower copper tracks are the + and - DC links, while the middle track is the output of the half-bridge. The three tooth-like patterns on the left of the dies are the locations of the DC decoupling capacitors

Thermal measurements (detailed in [11]) performed on the prototypes confirm the 4-fold reduction in thermal resistance achieved by replacing the PCB substrate by a DBC. The results are presented in Tab. II. For the PCB prototype, the maximum continuous current achievable is 25 A (above this value, the device enters thermal runaway, as its on-state resistance increases with temperature). For the DBC prototype, the 40 A value listed in Tab. II is limited by the test system.

III. ELECTROMAGNETIC ANALYSIS

In this section, we consider a half-bridge structure, with two EPC 2015 transistors and some decoupling capacitors. The power commutation loop is comprised of the input decoupling capacitor, the two transistors of the Half-Bridge and all the interconnections between these devices. With the significant reduction in stray inductance provided by the LGA Package, the substrate layout becomes the major contributor to the commutation loop inductance, and therefore, to the switching losses and EMI generation.

For PCB, an optimal design uses the first inner layer as a power loop return path [7]. As the current return path is located directly underneath the top power layer, this design leads to a lower loop inductance (from 1 nH down to 0.4 nH [7] when using the inner layer). With a DBC substrate, only one copper layer is available to route the signals, so the input capacitors and transistors must be placed on the same plane, and close proximity to minimize the size of the power commutation loop. However, as depicted in Fig. 2b, there is a second copper layer in the DBC structure. Even though this layer is not available for routing (this layer usually remains plain), it may contribute to reduce the stray inductances of the circuit. This effect is studied in this section.

The layout under investigation is presented in Fig. 5. Two loops are considered: a “large” loop, where the current flows

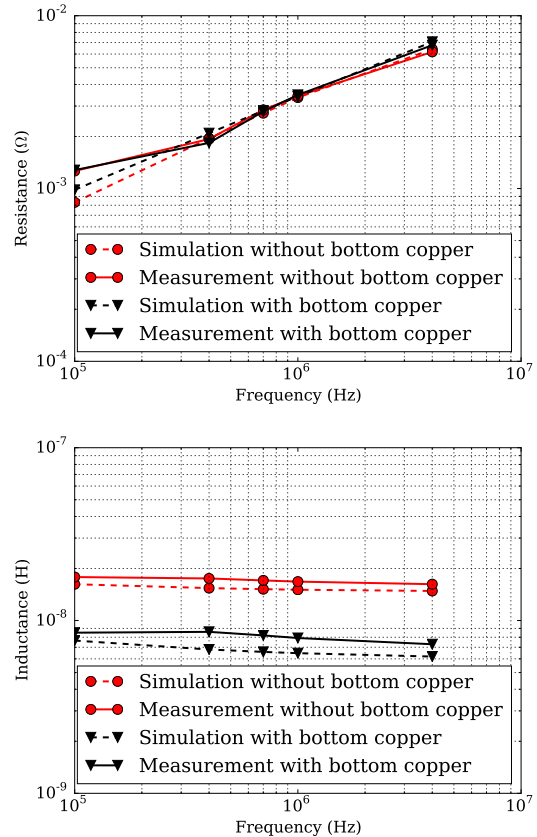


Fig. 6: Resistance and inductance along the “large loop”, obtained by simulation and measurement, for DBCs with and without backside copper.

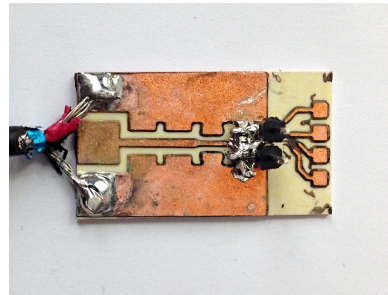


Fig. 7: Test vehicle for inductance measurement

across the full length of the DC link tracks, and a “short” loop, corresponding to the path of the current supplied by the rightmost DC capacitor. The large loop is used to compare simulation and experimental results (as it results in a larger inductance which is easier to measure), while the short loop corresponds to the actual path of the current during switching.

A first study is presented in Fig 6, with two versions of the layout from Fig. 5, both implemented on a DBC substrate: the first version has a plain layer of copper on its backside, while this layer is removed on the second version. The two version are prepared in a similar way to that presented in section II, with short circuits replacing the GaN dies. An inductance measurement is performed using a Keysight 4294A impedance

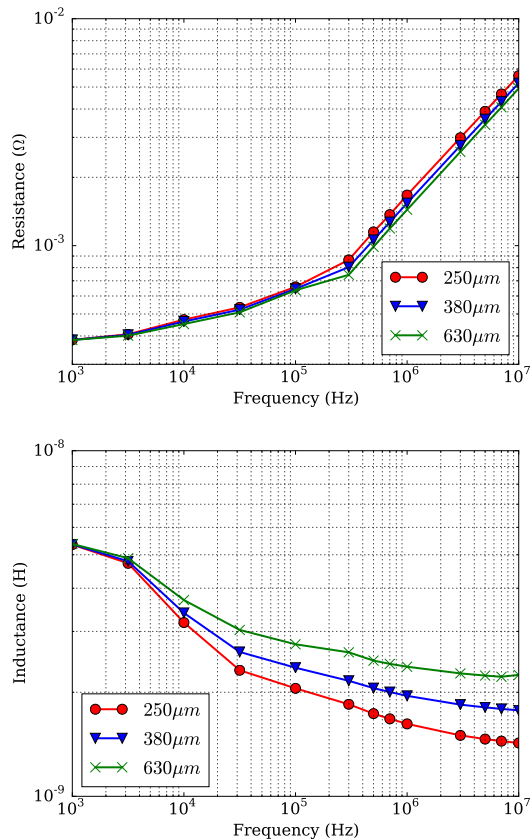


Fig. 8: Simulation and experimental results of different ceramic thickness

analyzer. A photograph of one of the DBC substrates with the connections for inductance measurement is given in Fig. 7. In parallel, a FEM model of the two versions is built using COMSOL. The model geometry is imported from Solidworks. The model is set to calculate the magnetic field over the entire system except on the feed gap located between the input terminals (see Fig. 5) [12]. Only surface currents are allowed around this gap, to close the current loop. The study is performed from 100 kHz to 4 MHz. The comparison between experimental and simulation results presented in Fig. 6 shows that they are in good agreement (15%). The backside copper layer has a strong effect, as it reduces the inductance by a factor of two, with negligible consequence on the resistance.

This screening effect offered by the backside copper is related to the insulated material thickness. A simulation study along the “short loop” is presented in Fig. 8 and shows that the inductance increases with the ceramic thickness. This is because the mutual inductance between the top and bottom copper layers decreases when the ceramic thickness increases. According to the mirror image method [13], the total inductance equals to the difference between self inductance of the top side circuit and the mutual inductance. As a consequence, the total inductance is larger when the ceramic layer is thicker. For a ceramic layer of 250 μm (a value which is still compatible with the manufacturers’ capabilities [8]), inductances of less than 2 nH are achievable. This is much

more than an optimized PCB (0.4 nH, [7]), but might still be acceptable in some cases. For a 30 A current, the energy stored in this additional stray inductance is $\frac{1}{2}LI^2=0.72 \mu\text{J}$, corresponding to an additional power dissipation of 0.72 W in the switches, for a 1 MHz operation. In reality, the power dissipated in the switches should be 2-3 times larger [14], because of slower switching due to the larger inductance.

Common mode performances could also be compared for DBC and PCB substrate. Common mode coupling is mainly induced by the stray capacitances between the copper tracks and the backside copper layer. Alumina has a higher permittivity ($\epsilon_R=10$) but is thicker than the PCB substrate ($\epsilon_R=4$). For the layout in Fig. 5, we obtain the following results on DBC: 51 pF (measured on 630 μm prototype), 85 pF and 129 pF (calculated for 380 and 250 μm respectively); for PCB, the capacitance was calculated at 187 pF. DBC is therefore better than thin PCB regarding common mode perturbations.

DBC offers a final advantage compared to PCB: thick standard copper layers. The 2-step etching process presented in section II-A allows to use 300 μm -thick copper despite the small pitch of the LGA-packaged transistors. As a result, the DC resistance for the large loop in Fig. 5 drops from 2.4 m Ω (the GaN devices have a $R_{DS(on)}$ of 4 m Ω) for a 35 μm -thick copper layer down to 1 m Ω for a 300 μm -thick layer with 2-step etching.

IV. CONCLUSION

This paper assesses the use of a ceramic substrate with GaN transistors. Although these transistors are designed to be mounted on a PCB, it is shown that a ceramic substrate offers a substantial gain regarding thermal management (4-fold reduction), and that parasitic inductances can be largely mitigated by choosing a proper substrate structure. With this solution, it is possible to use the GaN transistors at a much higher current level (more than 40 A vs 25 A using PCB). DBC is therefore an attractive substrate for the high current converters, as the slightly higher switching losses caused by the parasitic inductance will be more than counterbalanced by the dramatic reduction in thermal resistance.

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